High speed 21Mpixel global shutter image sensor

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Introduction

In recent years, many global shutter sensors have been presented with increasing resolution, performance and frame rate [1,2,3,4]. In this paper a 21 Mpixel (4096 rows, 5120 columns) global shutter sensor is presented which can reach 1000 fps at full resolution in 8 bits or 250 fps in 12 bits.

Sensor architecture and design

The pixel is a charge domain global shutter pixel at 4.5 µm pitch with dual gain readout, shown in Figure 1. Thanks to the double, split-column pixel architecture with dual sided readout and analog readout structures at 2.25 µm pitch, 4-pixel rows can be read simultaneously. Due to the double select line per row with alternating connections, all columns can be used when 2x2 pixels are configured in a charge binning mode, resulting in 8 (binned) pixel rows to be read concurrently as indicated in Figure 2. Without this double select line, half of the columns would not be usable in binning mode. From layout perspective, the array control lines were optimized, not only for high-speed readout, but also for short minimum integration times down to 4 µs. To keep minimum integration time small, it is important to have small propagation times especially on GRST and TG1.

The sensor readout chain and architecture are shown in Figure 3 and Figure 4 respectively. The switched capacitor column PGA has 2 input capacitors which allows to readout 2 lines interleaved and therefore blank away the pixel transfer (TG2) time [5] or, alternatively, perform a HDR read of the same pixel charge with 2 different conversion gains as depicted in Figure 5. Both modes rely on the column voltage during Reset ('R') phase being sampled on the input capacitor and the charge being frozen there until the corresponding Signal ('S') phase is available on the column line to perform CDS operation. The pixel readout process including pixel access and sampling at the S/H stage, A-to-D conversion and data readout is fully pipelined to achieve high frame rates.

As the sensor supports various modes with different line times and different noise requirements, a low pass RC filter is added in between the PGA output and the S/H stage before the ADCs. The S/H capacitor serves as the C of the filter. The R is implemented by a set of PMOS rather than poly resistors as shown in Figure 6. This has multiple benefits: a PMOS has a higher resistance per area than a poly resistor and the effective resistance varies with the signal level. In dark, where noise is dominated by the readout, a low bandwidth is desired. For near-saturation scenes, the noise is dominated by the shot noise of the pixel and therefore the readout bandwidth can be left higher such that the larger swing on the PGA output still settles fast.

The readout includes a low power ramp ADC in which 2 clock frequencies are used [6]. The high-speed clock is only active for maximum a period of the low-speed clock around the comparator toggle point while most of the counting is done on that low-speed clock avoiding unnecessary additional counts. Depending on the ADC bit depth a line can be converted in less than 1 µs for 8 bits and 1.9 µs for 12 bits linear by using a 1.8 GHz ramp A/D conversion. As both edges are used, the effective count rate

is 3.6 GHz. Supply IR drops were optimized to ensure that the supply remains sufficient for the ripple counter to work at the 1.8 GHz clock frequency. Figure 7 shows the ADC concept and indicates the hit on the power supply. Sufficient decoupling and low resistance supply routing are obvious design tricks to make this circuit work. Furthermore, it also helps to have sufficient offset in the analog domain to not have all 10240 comparators toggle at once with their corresponding high speed counting.

The sensor furthermore also provides on chip black level correction based on optically black pixels on the sides of the light sensitive array, reducing the row noise more than 10x below the random pixel noise, as well as providing some row fixed pattern correction. The data is being sent out over maximum 160 sub LVDS channels at 1.2 Gbps each, delivering up to 192 Gbps or up to 24 Gpixel per second. The number of channels used can be reduced in certain modes by multiplexing channels.

The large number of channels requires to have 4 bonding decks on the top and bottom side of the ceramic package. The package is a 454 pin µPGA.

Measured Results

A read noise of less than 3 e-, FWC of more than 30 ke- and up to 69.5 dB dynamic range intra frame are measured at 250 frames per second. Alternatively, in 8 bits mode, the frame rate can increase above 1000 for full resolution, which boils down to 245 ns per line. In the 2x2 binning mode, the frame rate almost quadruples. Additionally, a HDR mode is implemented based on dual gain readout at 60 fps providing about 81 dB intra scene dynamic range. Table 1 gives a performance summary of the developed sensor and Figure 8 shows a comparison to earlier reported work with comparable size and pixel pitch in terms of achieved maximum line rate.

The sensor is fabricated using TPSCo 65 nm monolithic 4M FSI CMOS image sensor process. A photograph of the sensor is shown in Figure 9. An image grabbed by the sensor in 12 bits mode is shown in Figure 10.

References

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[5] Y. Li, et al., “A pipeline row operation method of CMOS image sensors”, IEICE Electronics Express, Volume 18 (2021) Issue 6

[6] C. Ma, et al., “A 4M Pixel High Dynamic Range, Low Noise CMOS Image Sensor with Low Power Counting ADC”, IEEE Transactions on Electron Devices, Vol. 64, Issue 8, 2017: 0018-9383

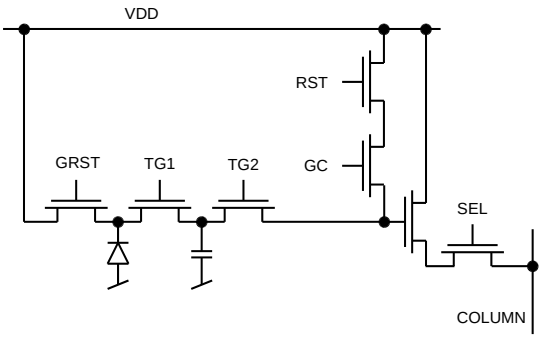

Figure 1 Charge Domain Global Shutter pixel with dual gain readout

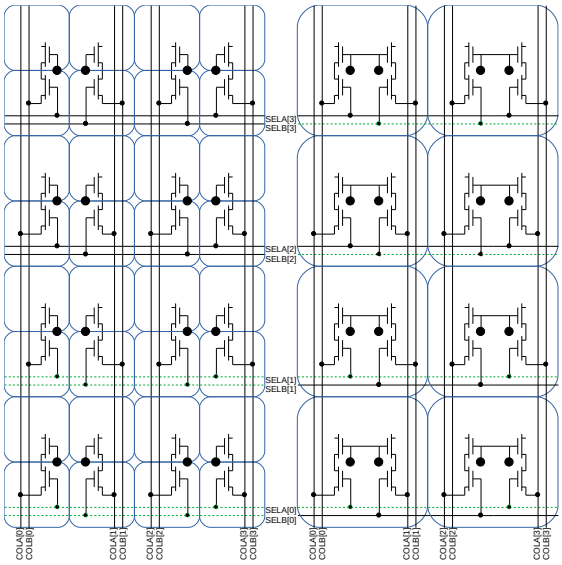

Figure 2 Array selection and readout: normal (left) vs binned (right). Green dashed lines show which select lines are active in a mode and pixel access slot. In normal mode, 2 full lines (per side) are read simultanously. In binned mode, only half of the selects on a line are needed, additional selects are switched on to use otherwise redundant columns (COLx[1] & COLx[3]).

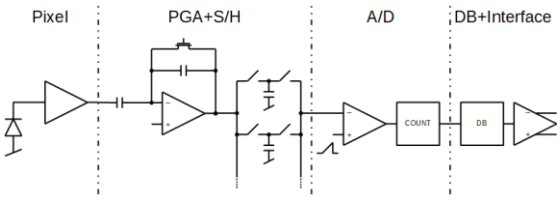

Figure 3 Readout chain. The pixel output column is connected to a column switched capacitor PGA with S/H stage. The latter is read and converted by a column ramp A/D converter and then processed by a data block to be sent over an LVDS interface

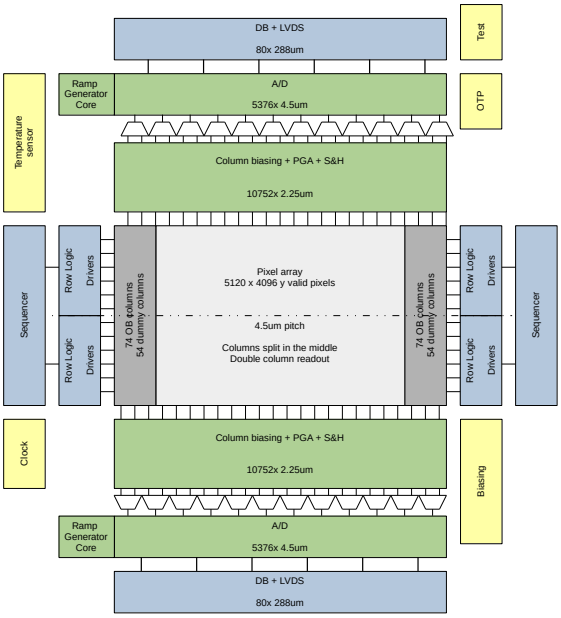

Figure 4 Chip architecture

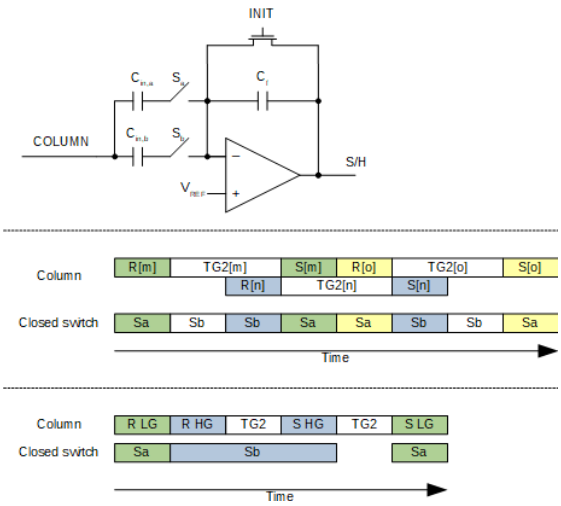

Figure 5 PGA circuit drawing and operation. In interleaved mode (middle) the input capacitors are alternated to make use of the columns during signal transfer. For HDR mode (bottom), the input capacitors serve as a sample-and-hold for the low gain reset while reading the high gain pixel values.

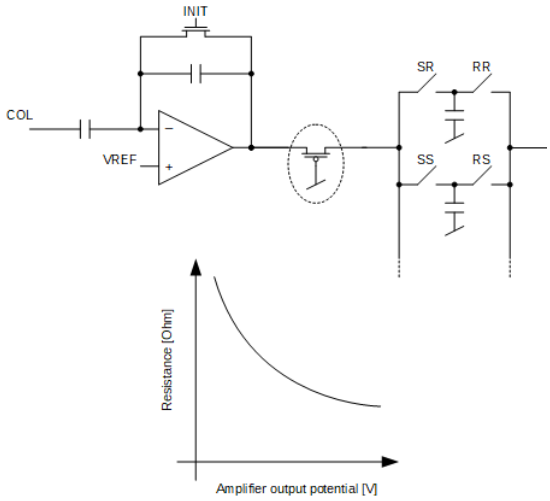

Figure 6 PGA Bandwith reduction by using PMOS device

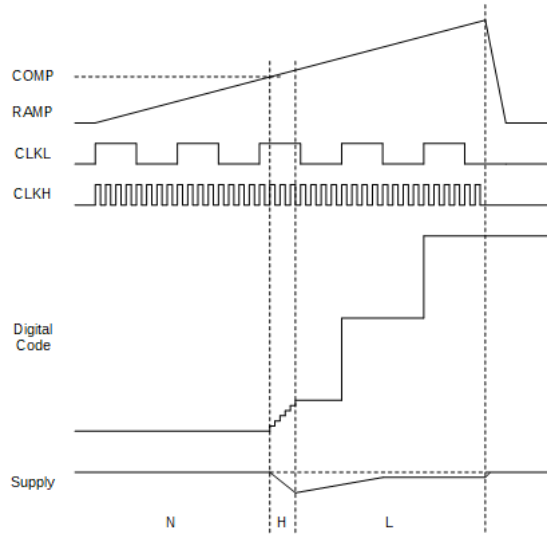

Figure 7 Dual clock ADC concept and supply impact when not counting (N), during high speed counting (H) and low speed counting (L)

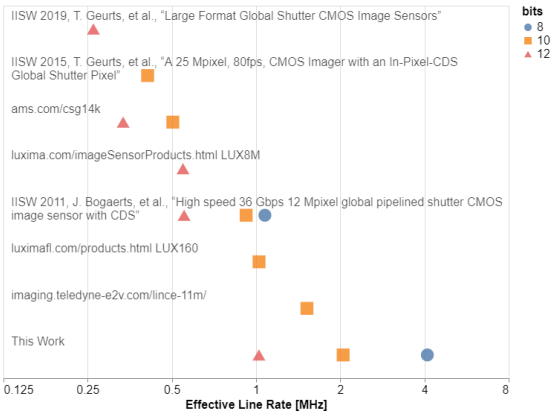

Figure 8 Line rate comparison for competitive sensors with similar size and pixel pitch 3.2 to 6 µm

Table 1 Image sensor performance

Parameter	Value	
Valid pixel resolution	5120x 4096y	
PLS	< -86 dB	
Dark current	< 60 e-/s @ 60C	
Peak QE	~ 63 % (530 nm)	
Full well	> 30 ke-, > 120 ke- (2x2 binned)	
ADC depth	8 bits	12 bits
Frame rate	> 1000 fps, > 3750 fps (2x2 binned)	> 250 fps, > 980 fps (2x2 binned)
Max DR	~ 52 dB	~ 69.5 dB
Read noise (max gain)	< 10 e-	< 3 e-
Row noise (max gain)	< 1 e-	< 0.3 e-
FPN (max gain)	< 10 e-	< 2 e-
Power	~ 6.1 W	~ 5.8 W
Dual gain HDR		< 3 e- noise > 30 ke- FWC > 81 dB DR > 60 fps

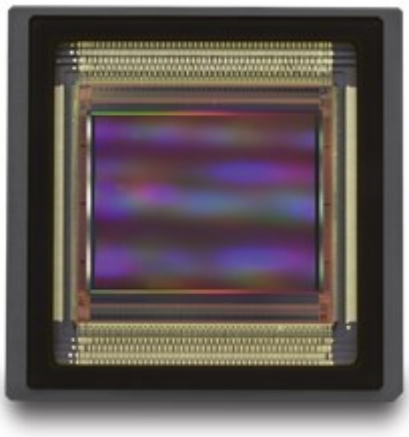

Figure 9 Fabricated and Packaged sensor. Top and bottom side showing 4 bonding decks.

Figure 10 Image taken with the developed image sensor in 12 bits mode