A 2.5µm 9.5Mpixel charge domain global shutter imager with dual columns and 7.1Gbps per channel outputs for high framerate applications

Jeroen Rotte, Rik Visser, Ruud van Ree, Frank van der Weegen,
Juul van den Heijkant, KlaasJan Damstra
Grass Valley, Breda, the Netherlands
Jeroen.Rotte@grassvalley.com, Bergschot 69, 4817 PA Breda, the Netherlands
Phone: +31 (0)76 303 2167

Abstract: **This paper presents a charge domain storage global shutter CMOS imager for broadcast applications. The image sensor requires an output framerate of minimal 180fps after digital CDS. The pixel pitch is 2.5µm, with a total array size of 4224x2248 resulting in a 9.5Mpix resolution and an 11mm effective diagonal. The 65nm process enables a higher speed serializer outputs. This design uses a serializer with 7.1Gbps per lane. The image sensor is manufactured in a 65nm 1Al/3Cu/1P 65nm CIS process.**

The imager is symmetrically build around the pixel array (figure 1). Left and right of the image array, shift registers for row addressing with level shifters are placed. On north and south of the image array, 16 bit column ADCs are placed. Hybrid output multiplexers generate a serial pixel stream. The pixel stream is serialized to max 7.1Gbps data rate at the serializer outputs.

The pixel used in the array is a two diagonally shared, select-less charge domain global shutter type [1] [2].

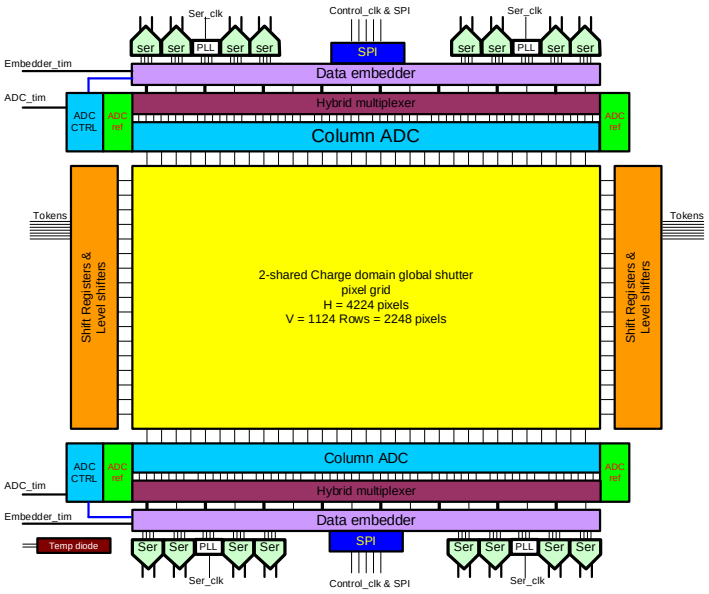

Figure1: Architectural blockdiagram

The pixel is operated in global shutter mode by activating TG_A (See figure 2) to transport for all pixels in parallel the collected charge in PD to the storage node (SN). Alternatively the pixel can be read in rolling shutter mode by activating TG_A row by row.
The storage node is read per row. By bringing the VDDC and the RST to high level, the pixel source follower for a certain row can be activated to drive the column. The column voltage is sampled as ‘resetlevel’. Charge is now transported from the Storage Node (SN) to the floating diffusion by activating the TG_B, and the ‘signal level’ can be read. All these actions take place in series and each requires its own settling and transfer time, limiting the readout speed. For high framerate readout, a second column has been added. Figure 2 shows the pixel diagram with dual column. A timing diagram for a select-less pixel with a single column and a dual column readout comparison is shown in Figure 3. In case of conventional pixel timing next to the

signal level sampling time, a wait state for transfer and column activation is needed. With a dual column architecture two rows are operated in parallel to alternate the processes of column sampling, and pixel resetting and charge transfer from storage node (SN) to floating diffusion (C_{fd}). This way the throughput of reset- and signal levels is maximized out of the pixel array.

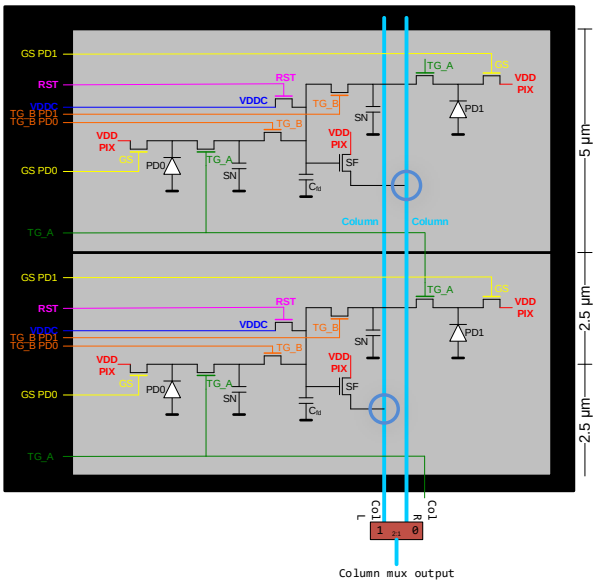

Figure 2: Circuit diagram pixel with dual columns

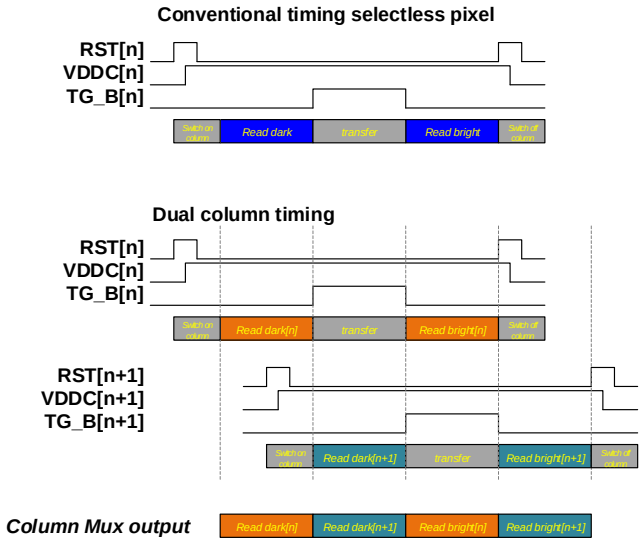

Figure 3: Timing diagram single vs dual columns

The signal levels from the column are sampled on the digital sub-ranging, charge based column ADC built on the concept of [3]. The ADC converts the high input range signal to a 16bit output value. This way the pixel low-noise values and the high full-well values are preserved and the full dynamic range is maintained.

The 8448 column wires are multiplexed to 2112 column ADCs with a 4:1 analog input multiplexer. The digital output data from the A/D converters is serialized by a hybrid output multiplexer [4].
In the data embedder the ADC data is processed. A CRC inserter is introduced to enable monitoring the integrity of the serializer links between the imager and the receiving FPGA. The CRC inserter uses a 16-bit parallel implementation of the CRC-16/MODBUS polynomial for 16 and 14-bit data modes. The polynomial used is $x^{16} + x^{15} + x^2 + 1$. [5]

The imager is designed for use in source synchronous applications. A training pattern is inserted to enable the data receiver to dynamically lock to the data stream. A sawtooth pattern and an all zeros / all ones pattern in inserted at the start of each new frame. The receiving FPGA can phase, bit and byte align on these patterns. The source synchronous system avoids the need for length matching of the multiple signal output lanes, reducing system complexity. The imager serializer outputs are AC-coupled to the FPGA multi-gigabit receivers. A scrambler is used to ensure enough data transitions are offered to the receiving CDR. Furthermore, it assures a statistical DC balanced data stream to allow the AC-coupling of the link. The scrambler is a parallel multiplicative (self-synchronizing) scrambler with the polynomial: $G(x) = x^{58} + x^{39} + 1$ [6]. The scrambler is implemented MSB first.

The data embedder also offers the option of daisy chaining to reduce the number of active outputs at lower framerates and takes care of mapping the data correctly to the serializer in case of 16/14 bit output modes. Additionally a PRBS-7 and PRBS-31 generator are implemented in the data embedder.

After processing, the data is delivered to the serializer blocks [7]. The serializer has programmable serialization widths of 28 or 32 bit. The output is compatible with JESD8-13 (SLVS-400) and runs up to 7.1 Gbps per channel. The imager has 16 of such lanes resulting in a total maximum output data rate of 114Gbps. Measurement results are shown in figure 4 and 5, using a PRBS-7 signal.

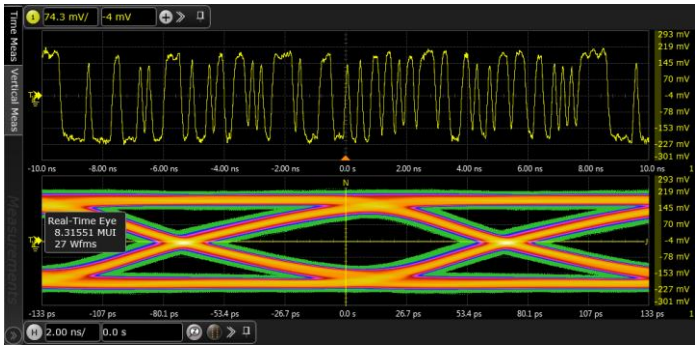

Figure 4: Eye diagram SLVS output at 7.1 Gbps

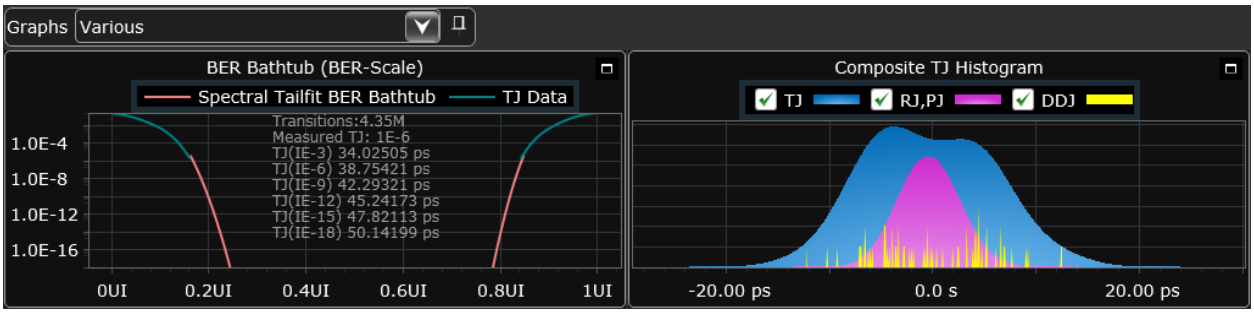

Figure 5: Serializer BER bathtub and total jitter histogram

The high output data rate enables digital CDS off-chip at high framerate. For the target output framerate of 180fps eight lanes are needed at 7.1Gbps each.

The prototype imager has been successfully manufactured. A die micrograph is shown in figure 6. An exemplary output image demonstrating global shutter is shown in figure 7. The serializer outputs run at 7.1 Gbps including the custom ceramic package. Performance measurements show a system noise level of 1.9e- read noise with 7ke- linear full well. The imager shows no lag and the 1/PLS is measured at >80dB in green. A list of parameters is given in figure 8.

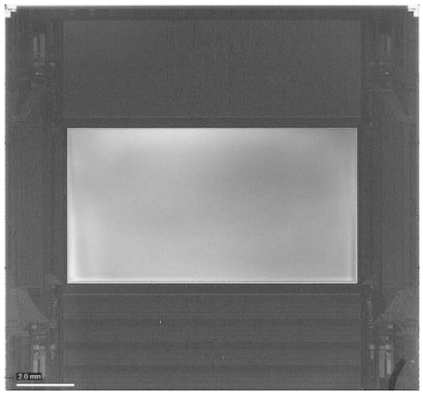

Figure 6: Chip micrograph

Figure 7: Sample UHD image at 60fps with integration time of 1ms

Parameter	Unit	Value	Note
Resolution	[#]	4224 (H) x 2248 (V)	9.5 Mpix
pixel size	[µm]	2.5	
shuttertype		global	charge domain storage
noise	[e-]	1.9	
full well [e-]	[e-]	7000	
PLS	[dB]	-80	typ @ F11
MTF @ 800 TVL	[%]	40	
Framerate after CDS	[fps]	240	
ADC type		column wise	charge based digital multi-slope
ADC count	[#]	2112	(sum of North and South)
ADC noise	[µV]	120	
ADC resolution	[#]	14..16 bit	240 .. 60 Hz framerate
ADC conv time	[ns]	<450	
Output interface			
# of channels	[#]	16	
Output interface		SLVS	
datarate per channel	[Gbps]	7.2	
Package		Custom ceramic 215 pin PGA	
Technology node		65 nm, 1P4M	
Die area	[mm2]	210	
Control		SPI	
Power	[W]	1.9 .. 3.5	60..240 Hz output framerate

Figure 8: Parameter list

Acknowledgements

The development of this imager has been performed in the framework of the European Penta project SENSATION.

References

[1] T. Yokoyama, et al. "High Performance 2.5µm Global Shutter Pixel with New Designed Light-Pipe Structure" *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2018, pp. 10.5.1-10.5.4, doi: 10.1109/IEDM.2018.8614569.
[2] I. Mizuno et al, “A High Performance 2.5µm Charge Domain Global Shutter Pixel“, R51, IISW, June 2019.
[3] S. Louwsma et al. “A scalable 12b-16b charge-domain multi-slope column ADC for HDR imagers with 86dB DR and 1µs conversion time”, R33, IISW, June 2019.
[4] J. Rotte et al. “A 2.5µm 9.5 Mpixel high framerate CMOS imager with hybrid output multiplexer and 58Gb/s datarate”, P30, IISW, June 2019.
[5] CRC-16/MODBUS (https://reveng.sourceforge.io/crc-catalogue/all.htm)
[6] SERIAL INTERFACE FOR DATA CONVERTERS, JEDEC standard, JESD204C, Dec 2017
[7] J. Galloway, https://www.siliconcr.com/newsroom/detail/128/why-do-we-need-serdes, May 2020.