

# Crystalline Selenium Layer Stacked CMOS Image Sensors with Pixel-Wise 1-bit A/D Converters using Avalanche Multiplication Suitable for Photon Counting

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## Abstract

We report crystalline-selenium (c-Se) photoconversion layer stacked CMOS image sensors with pixel-wise 1-bit A/D converters (ADCs) using avalanche multiplication suitable for photon counting. The c-Se layer is introduced to separate photomultiplication function from circuits to achieve high sensitivity and high spatial resolution. The 1-bit ADCs with pulse output realize pixel-wise digital imaging. The prototype sensor confirmed video images including avalanche multiplication operation for the first time, demonstrating feasibility of photon counting. The soft-X-ray imaging was also demonstrated as an invisible-light sensing application by exploiting the X-ray sensitivity of c-Se.

## Introduction

Photon counting is a superior, high-sensitivity imaging process, which detects incident photons discretely. Recently, single-photon avalanche diode (SPAD) imagers [1] have attracted much attention with high photon detection efficiency. Although size reduction of SPAD pixel has been studied [2], there are still challenges for high spatial resolution owing to their large diodes. To solve these problems, we have been studying c-Se stacked image sensors with 1-bit ADCs [3]. The sensor separates photomultiplication function from circuits, which realizes highly integrated pixels. In this paper, we demonstrate the first video imaging with avalanche multiplication and soft-X-ray imaging.

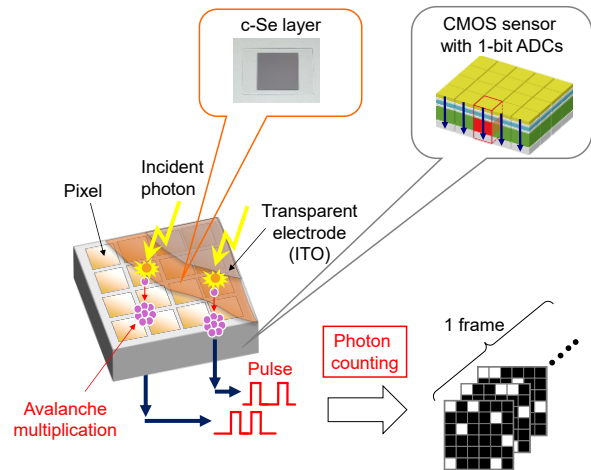
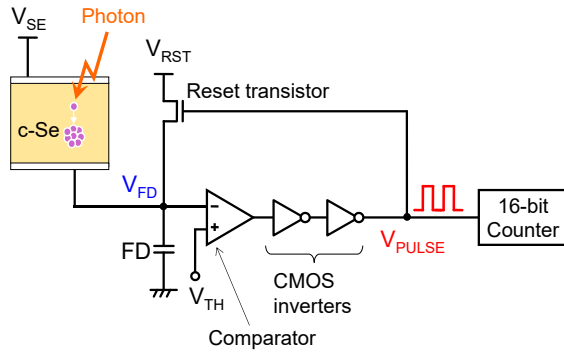


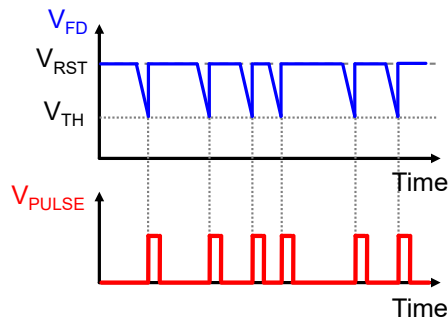
Figure 1: Schematic diagram of the proposed c-Se layer stacked CMOS image sensor.

## Design and Implementation

Figure 1 shows a schematic of the proposed sensor. The c-Se layer is overlaid on the CMOS sensor. A photogenerated charge in the c-Se layer can be multiplied by avalanche multiplication [4]. A set of multiplied charges generates a pulse to be counted by 1-bit ADCs [5–7]. The circuit diagram is shown in Fig. 2. Whenever the floating diffusion potential reaches the threshold of the comparator, pulses are output and detected by the counter. Figure 3 shows the fabrication process flow, where Au electrodes are formed by electroplating and chemical–mechanical polishing (CMP). The p-type c-Se and the n-type  $\text{Ga}_2\text{O}_3$  comprise a p–n photodiode. The cross-section of the pixel in Fig. 4 confirmed a 300-nm-thick c-Se film covered the entire pixel.



(a)



(b)

Figure 2: (a) Circuit diagram and (b) operation-timing chart for 1-bit ADC pixel. The circuit consists of a floating diffusion (FD), a comparator, CMOS inverters, a reset transistor, and a 16-bit counter.

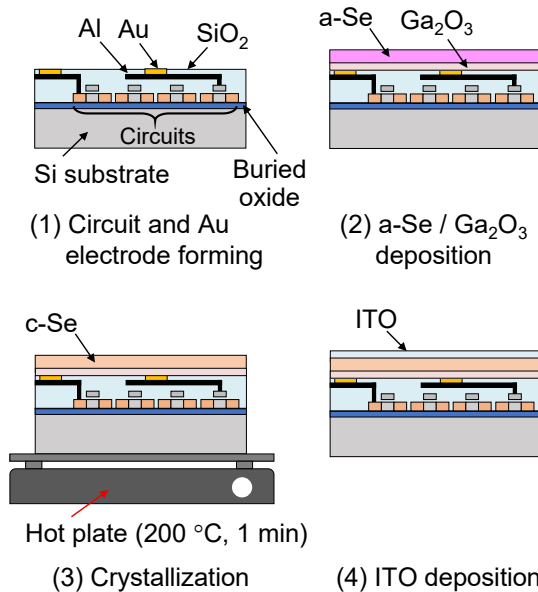


Figure 3: Fabrication process flow for the sensor. The p-type c-Se and the n-type Ga<sub>2</sub>O<sub>3</sub> comprise a p-n photodiode.

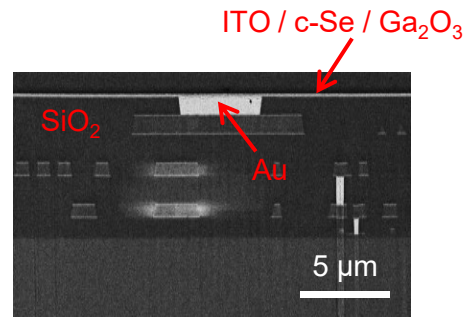


Figure 4: Cross-sectional scanning electron microscopy image of stacked sensor pixel. A 300-nm-thick c-Se film covers the entire pixel.

### Measurement Results

Figure 5 shows the measured output versus supply voltage of c-Se ( $V_{SE}$ ). The photogenerated signal rises in  $V_{SE}$  from 0 to 5 V and exhibits a further increase of more than 10 V with avalanche multiplication. Figures 6 shows the captured video images for different  $V_{SE}$ . Figure 6 (c) shows the first highly sensitive image achieved by avalanche multiplication.

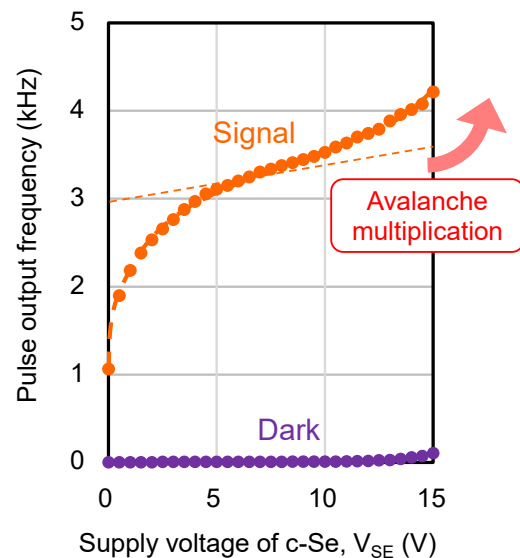


Figure 5: Measured output as a function of the supply voltage of c-Se ( $V_{SE}$ ), where input illuminance is 1,200 lx. The output exhibits avalanche multiplication for the voltage of more than 10 V.



(a)



(b)



(c)

Figure 6: An example of captured images for different  $V_{SE}$ : (a) 1 V, (b) 5 V, and (c) 11 V, where the frame rate is 30 fps, and the lower 8-bit signal is used to produce a 256-gradation image. The sensor has  $128 \times 96$  pixels. Figure 6 (c) confirmed a highly sensitive image achieved by avalanche multiplication.

We also demonstrated soft-X-ray imaging, which is suitable for observing light element materials and biological specimens, as an invisible-light sensing application. A soft X-ray tube and the sensor were set closely, and objects were put directly onto the sensor (Fig. 7). Figure 8 (a) shows X-ray absorption rates for different c-Se film thicknesses. We used 1- $\mu\text{m}$  thickness this time, and thicker film would increase photoconversion efficiency. The images were successfully captured owing to the X-ray sensitivity of c-Se (Fig. 8 (b)), indicating feasibility of an invisible-light photon-counting application.

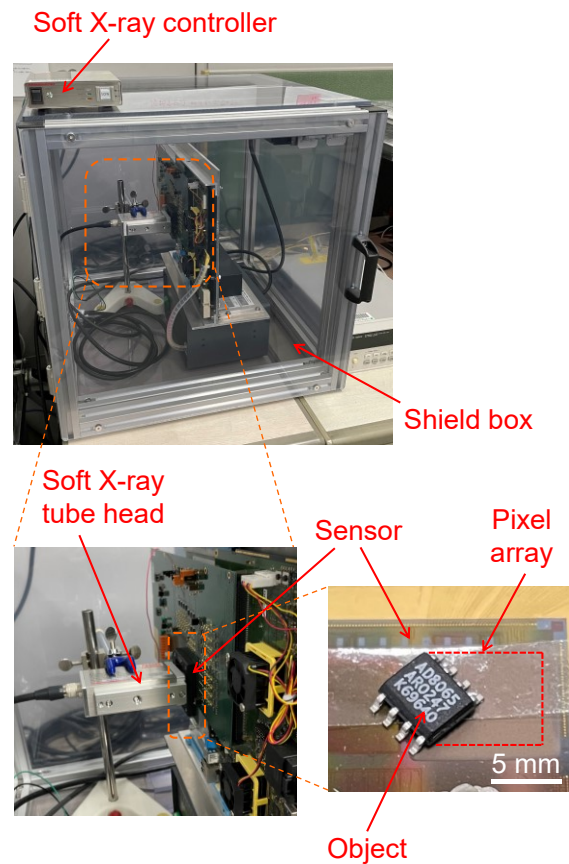
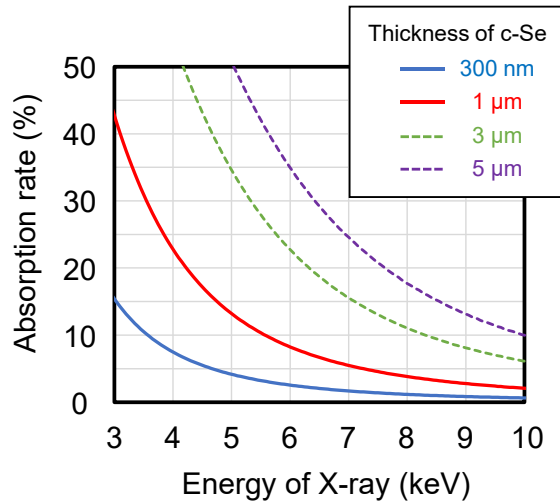
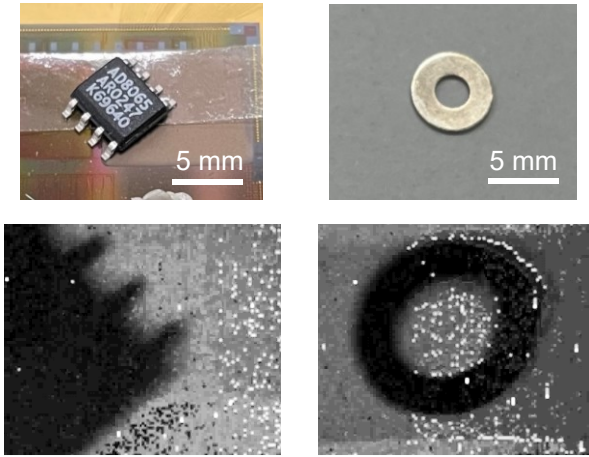


Figure 7: Experimental setup for soft-X-ray imaging, where the soft X-ray energy ranges from 3 to 9.5 keV.



(a)



(b)

Figure 8: (a) X-ray absorption rates for different c-Se film thicknesses. The plots are calculated using the measured absorption rate of 80-nm-thick c-Se film. The experiment used 1- $\mu\text{m}$  thickness. (b) Captured images of objects by soft X-ray irradiation, where  $V_{\text{SE}} = 3 \text{ V}$  under visible light shielding.

### Conclusion

We developed c-Se stacked CMOS image sensors with pixel-wise 1-bit ADCs. Measurement results showed functions of video imaging with avalanche multiplication and soft-X-ray imaging. As the next step, we will increase the multiplication factor of c-Se to realize a single-photon counting as well as enhance applications, including visible and nonvisible imaging.

### References

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