High-precision CMOS Proximity Capacitance Image Sensors with Large-format 12 µm and High-resolution 2.8 µm Pixels

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ABSTRACT

This paper presents newly developed two high-precision CMOS proximity capacitance image sensors: Chip A with 12 µm pitch pixels with a large detection area of 168 mm^2; Chip B with 2.8 µm pitch 1.8 M pixels for a higher resolution. Both fabricated chips achieved a capacitance detection precision of less than 100 zF (10^{-19} F) at an input voltage of 20 V and less than 10 zF (10^{-20} F) at 300 V due to the noise cancelling technique. Furthermore, by using multiple input pulse amplitudes, a capacitance detection dynamic range of 120 dB was achieved. The examples of capacitance imaging using the fabricated chips are also demonstrated.

INTRODUCTION

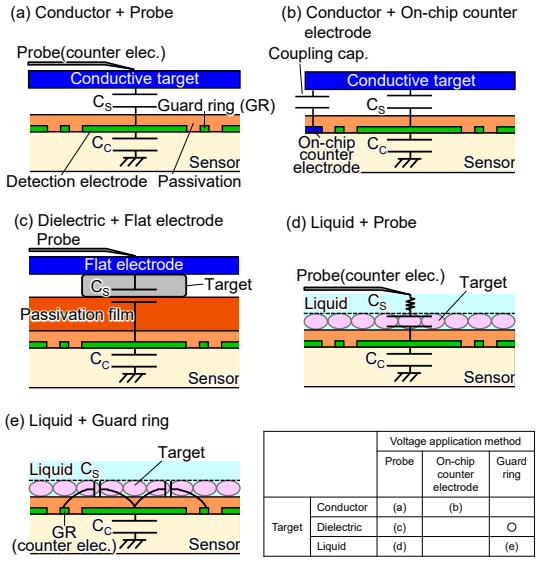
Image sensors can capture two-dimensional information from the real world and are used in various fields such as autonomous driving and factory automation for improving safety, security as well as productivity. Among the many types of image sensors, proximity capacitance image sensors can detect and visualize two-dimensional distributions of capacitance between the sensors and targets. Unlike optical image sensors, these sensors can detect electrical connections as well as microroughness and minute irregularities on the surface of objects and distribution of substances inside organic, solid, and liquid materials. They are used in various applications such as wiring inspection for flat panel displays and printed circuit boards, fingerprint authentication, material surface observation, and so on.[1-5] These applications require not only a high precision to detect minute capacitance, but also a large detection area to improve the inspection efficiency of a large area targets. In addition, a high spatial resolution is required to capture small targets such as biological cells.

So far, discrete sensors with aF-order detection precision[6] and an array sensor with a detection area of 8.73 cm^2 with 11.4 µm pitch pixels[4] have been reported. However, a simultaneous achievement of a detection precision of less than aF and a detection area of more than 1 cm^2 or, a pixel pitch of less than 10 µm toward a higher resolution has not been reported yet. Recently, we have presented a prototype CMOS proximity capacitance image sensor with 256^H×256^V 16 µm pitch pixels achieving 100 zF detection precision due to the advanced noise cancelling technique.[7-8] In this paper, we describe the newly developed two chips to increase imaging area and spatial resolution: the Chip A with large format 12 µm pixels for practical inspection applications and the Chip B with high-resolution 2.8 µm pitch pixels. The operating principle, circuit and layout design, and chip measurement results are described as follow.

DESIGN AND STRUCTURE OF DEVELOPED CHIPS

Fig. 1 shows the cross-sectional diagrams illustrating the proximity capacitance imaging setups. For the proposed proximity capacitance sensors, a counter electrode is introduced to which the input pulse signal is supplied. For a conductor target, the input pulse signal is supplied by a probe and the target itself is used as the counter electrode, as in (a). It is also possible to measure proximity capacitance without a probe by supplying the input pulse signal through a coupling capacitance between the target and the counter electrode in the chip, as in (b). For a dielectric target, the measurement is performed by placing a flat counter electrode and supplying an input pulse signal to it, as in (c). For a target in a liquid, the measurement is carried out by placing a probe or using the guard ring in the sensor as a counter electrode and supplying the input pulse signal to it, as in (d) or (e). By using an appropriate measurement method, various objects can be measured.

Fig. 2 shows the circuit block diagram of the developed chips. Each pixel is comprised of a detection electrode and a readout circuit. First, the vertical scanning circuit selects a row and acquires the signal, then the column S/H circuit holds the signal, and the horizontal scanning circuit selects a column and reads the signal out of the chip in sequence.



		Voltage application method		
		Probe	On-chip counter electrode	Guard ring
Target	Conductor	(a)	(b)	
	Dielectric	(c)		○
	Liquid	(d)		(e)

Fig. 1 Typical measurement configurations. Chip B has an on-chip counter electrode outside the pixel array, allowing imaging without a probe as in (b).

Fig. 3 shows the simplified sensor circuit and operational timing diagrams of the normal and the high dynamic range (HDR) modes. Each pixel contains a detection electrode capacitance (C_C) which is connected to the measurement capacitance (C_S) in series. The voltage of floating detection electrode node between C_C and C_S is readout twice; first after the reset operation, and second after the voltage level is changed at the counter electrode. By taking the difference of the two signals, thermal noise remained at the floating node, low frequency noise of in-pixel SF and fixed pattern noise are cancelled. The output is obtained by the following equation.

$$V_{OUT} = V_{OUTN} - V_{OUTS} = \frac{C_S}{C_C + C_S} \cdot V_{IN} \cdot G_{SF} \quad (1)$$

Here, the proximity capacitance signal (V_{OUT}) is proportional to the voltage amplitude (V_{IN}) applied to the counter electrode. The larger the V_{IN} applied, the smaller the capacitance can be detected, but if the capacitance is large, the signal output will saturate beyond the signal readout range of the chips. In the HDR mode, two or more voltage amplitudes are applied to measure a wide range of capacitance within a signal readout range of the chips.

Fig. 4 shows the layout diagrams and circuit schematics of the developed pixels, respectively. The pixel in Chip A uses an isolated P-well in the deep N-well for the SF to improve the gain and it also forms a protection diode to protect the floating node from high voltage. In the pixel of Chip B, the SF is formed in a normal P-well, and one side of the protection diodes was removed to reduce the pixel size. As a result, the pixel size of Chip B becomes 1/18th of that of Chip A.

CHIP FABRICATION AND MEASUREMENT RESULTS

Fig. 5 shows the micrographs of the fabricated chips. A 0.18 µm 1-poly-Si 5-metal CIS technology was employed. The chip size, number of pixels and pixel pitch were 14.4×14.4 mm^2, 1080^H×1080^V and 12 µm for Chip A, and 4.8×4.8 mm^2, 1408^H×1280^V and 2.8 µm for Chip B, respectively.

Fig. 6 shows the cross-sectional pixel TEM image of Chip B. The first through fourth metal layers were used for wiring, and the fifth metal on the top layer is used as the detection electrode and the guard ring.

Fig. 7 shows the measurement system. It consists of a headboard with the fabricated sensor chip mounted face up, an analog front-end (AFE) circuit board with voltage regulators and a 14 bit differential ADC directly connected to V_{OUTN} and V_{OUTS}, a FPGA board to supply operation pulse to the sensor chip, and a PC.

Fig. 8 shows the measured noise characteristics without any measurement targets obtained without and with the noise cancelling. Without the noise cancelling, the input referred FPN and temporal random noise arises mainly due to the threshold voltage variation of SF and column fixed pattern noise, and the kTC noise at the detection electrode node. They were 19.3 mV_{rms} and 1.29 mV_{rms}, respectively for Chip A, and 16.4 mV_{rms}, 1.71 mV_{rms}, respectively for Chip B. These noise components were significantly reduced by the noise cancelling to 37.8 μV_{rms} and 267 μV_{rms},

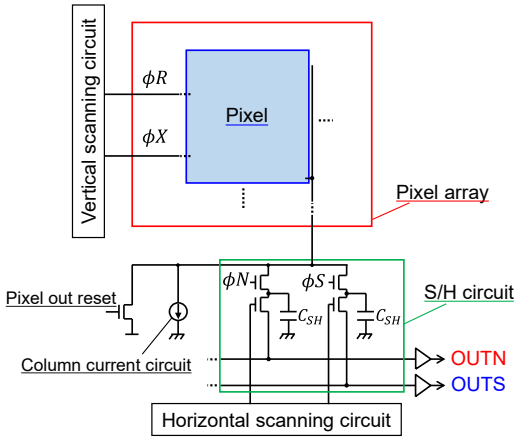


Fig. 2 Circuit block diagram of the two chips.

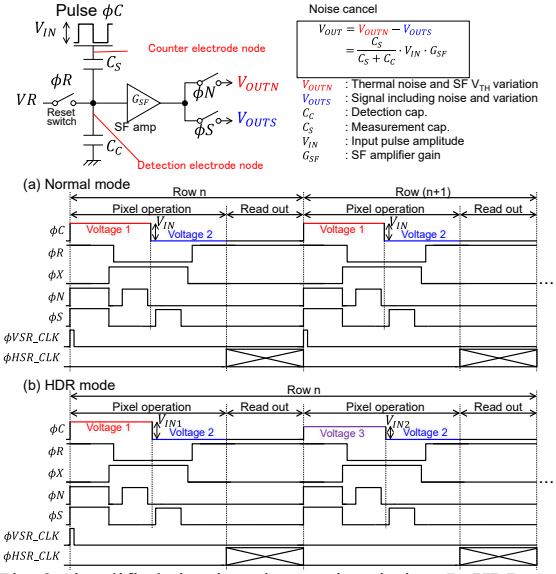
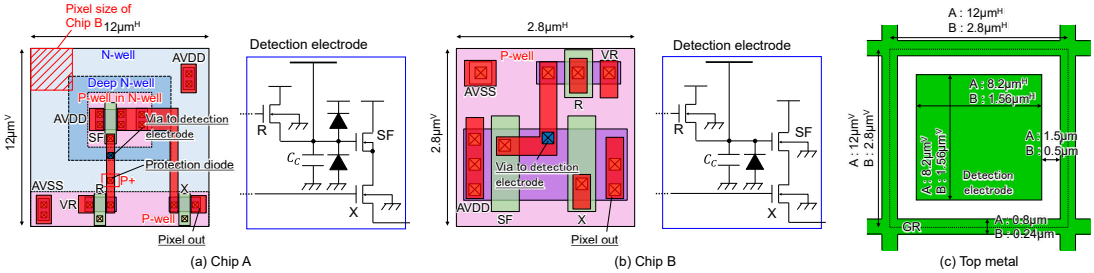


Fig. 3 Simplified circuit and operation timing. In HDR mode, signals are readout multiple times for each row while varying V_{IN}.



(a) Chip A (b) Chip B (c) Top metal

Fig. 4 (a-b) layout diagrams of pixels up to the 1st metal layer and circuit schematics and (c) the top metal layer layout.

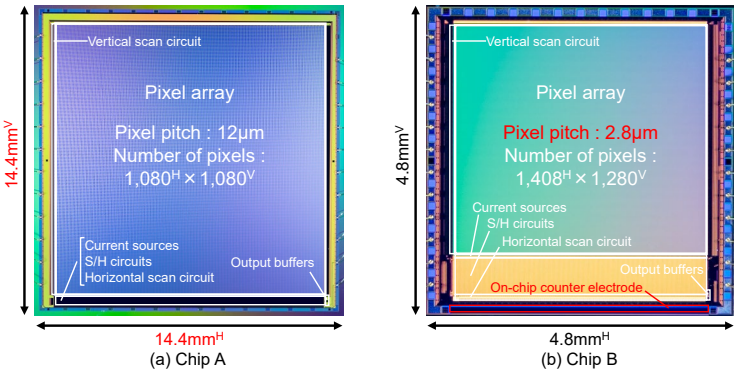


Fig. 5 The micrograph of the fabricated CMOS proximity capacitance image sensor Chips A and B.

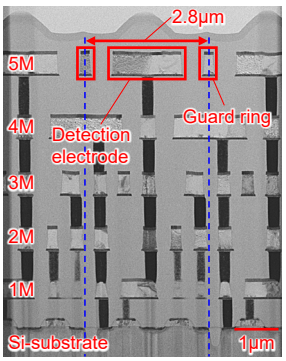


Fig. 6 The cross-sectional pixel TEM image of Chip B.

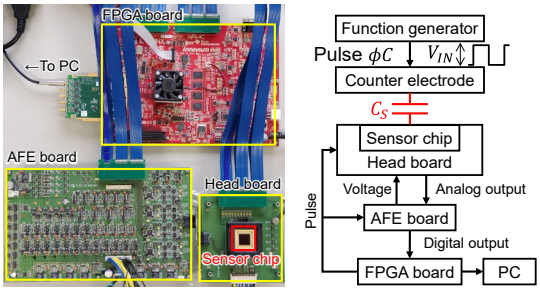
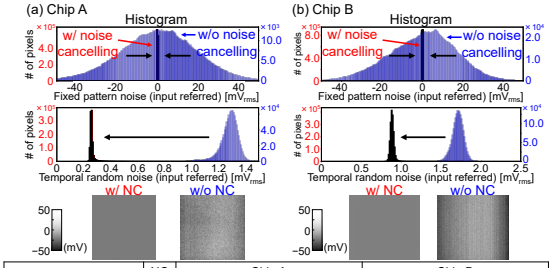


Fig. 7 The measurement system for characterizing the performance of fabricated sensor chips.



	NC	Chip A	Chip B
Fixed pattern noise (input referred)	w/o	19.3mV$_{rms}$	16.4mV$_{rms}$
	w/	37.8μV$_{rms}$	137μV$_{rms}$
Temporal random noise (input referred)	w/o	1.29mV$_{rms}$	1.71mV$_{rms}$
	w/	267μV$_{rms}$ (w/o averaging) 25.2μV$_{rms}$ (100 frames average)	887μV$_{rms}$ (w/o averaging) 85.5μV$_{rms}$ (100 frames average)

Fig. 8 Noise characteristics without and with the noise cancelling (NC).

respectively for Chip A and 137 μV_{rms} and 887 μV_{rms}, respectively for Chip B, without averaging. Furthermore, temporal random noise can be reduced by multiple frames averaging; 25.2 μV_{rms} was achieved for Chip A and 85.5 μV_{rms} for Chip B, respectively by 100 frames averaging.

C_C in equation (1) was calculated to be 5.4 fF for Chip A and 2.5 fF for Chip B from the parasitic capacitance extraction, and 2.8 fF was obtained for the fabricated Chip B from the measured photon transfer curve using the protection diode as a photodiode.

Fig. 9 shows the measured transfer characteristic of the two chips with various measurement capacitance conditions. Here signal output is plotted as a function of the voltage amplitude of input pulse. The colored dots show the measured values, and the black lines are the calculated characteristics at each capacitance value, using equation (1) and the C_C obtained from the simulation and the measurement for the Chip A and B, respectively. The results indicate that 1 fF to less than 10 zF of proximity capacitance was successfully measured in the range of input pulse amplitude below 300 V. In addition, the input referred signal range was confirmed to be over 1.0 V with a good linearity.

Fig. 10 shows a fingerprint image captured by Chip A. Owing to its large pixel area, the entire fingerprint was captured. In addition, sweat gland pores of several tens of μm in diameter were clearly captured.

Fig. 11 shows capacitance images of a logic IC (TC74HC02) captured by the two chips. For the Chip B, the resolution was greatly improved, and the shape of the wiring and transistors could be clearly captured. Furthermore, by shooting in HDR mode, it was possible to capture both small and large capacitance regions simultaneously.

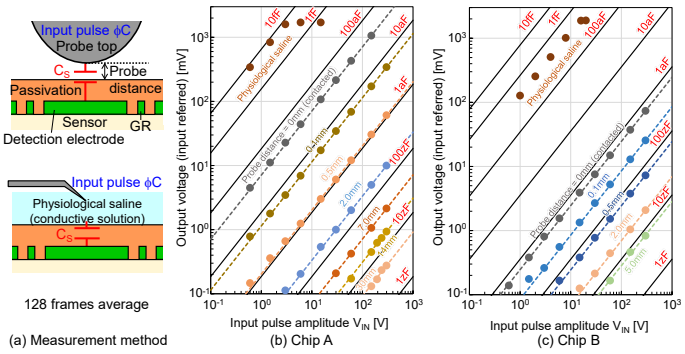
Fig. 12 shows the images of a drop of saline solution on the sensor surface captured by Chip B with the setup in Fig. 1(e) without external counter electrode. The water evaporates over time, and the final salt crystal precipitation was clearly captured.

Table I shows the performance of the developed chips. Compared to our previous work, Chip A achieved 10 times larger imaging area and a higher precision, and Chip B achieved 18 times higher resolution while maintaining the precision.

Fig. 13 shows the benchmarking of the developed proximity capacitance CMOS image sensors with other array and discreate capacitance sensors.[1-12] The developed sensors have a large pixel area or a higher resolution while achieving higher detection accuracy than other sensors.

CONCLUSION

Two high-precision CMOS proximity capacitance image sensors were presented in this paper. Both chips successfully achieved real-time proximity capacitance imaging with high precision. Using the Chip A with a large pixel area, the measurement efficiency will be improved especially for large measurement targets like flat panel displays. It is production ready for wiring inspection applications. For the Chip B with high-resolution pixels, it is expected to be useful for the visualization of microscopic objects such as living cells. The developed sensors can be utilized for high efficiency measurement tools in the manufacturing, biomedical, life scientific fields and more.



(a) Measurement method (b) Chip A (c) Chip B

Fig. 9 Measured transfer characteristics of the Chips A and B with various capacitance conditions.

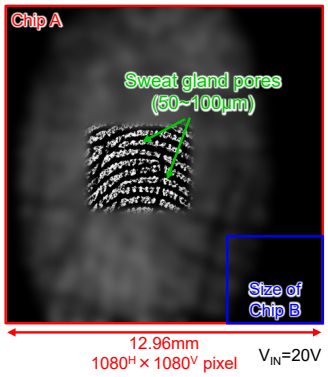
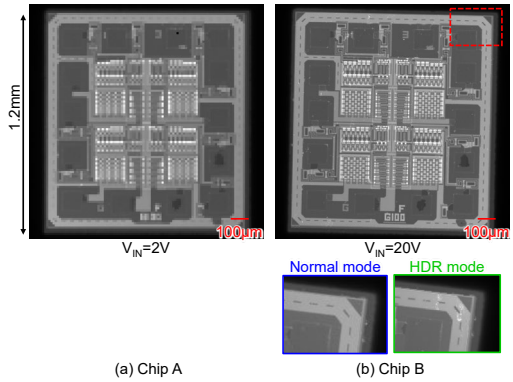
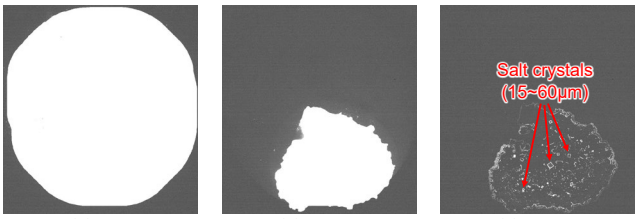


Fig. 10 Captured image of fingerprint by the large format Chip A. (Blurred for privacy)



(a) Chip A (b) Chip B

Fig. 11 Captured images of a general-purpose logic IC (TC74HC02) for resolution comparison between the Chip A and B.



(a) t=0s (b) t=500s (c) t=600s

Fig. 12 Captured images of a drop of saline solution on the sensor surface drying out as time advances captured by the Chip B.

Table I Performance summary of the developed sensors.

	Previous work[7-8]	Chip A	Chip B
Process	1-Poly 5-Metal 0.18μm CMOS		
Die Size	4,800μm^{H}×4,800μm^{V}	14,400μm^{H}×14,400μm^{V}	4,800μm^{H}×4,800μm^{V}
Pixel Area	4,096μm^{H}×4,096μm^{V}	12,960μm^{H}×12,960μm^{V}	3,942.4μm^{H}×3,584μm^{V}
# of Pixels	256^{H} ×256^{V}	1,080^{H} ×1,080^{V}	1,408^{H} ×1,280^{V}
Pixel Size	16μm^{H}×16μm^{V}	12μm^{H}×12μm^{V}	2.8μm^{H}×2.8μm^{V}
Detection Electrode Size	12μm^{H}×12μm^{V}	8.2μm^{H}×8.2μm^{V}	1.56μm^{H}×1.56μm^{V}
Frame Rate	60fps	7fps	8fps
Sampling Frequency	20MHz	20MHz	20MHz
Saturation Signal	1.03V (input referred)	1.70V (input referred)	1.89V (input referred)
Temporal Random Noise (input referred)	321μV$_{rms}$ (w/o averaging), 55.1μV$_{rms}$ (100 frames average)	267μV$_{rms}$ (w/o averaging), 25.2μV$_{rms}$ (100 frames average)	887μV$_{rms}$ (w/o averaging), 85.5μV$_{rms}$ (100 frames average)
Detection Precision	1×10^{-19}F (V$_{IN}$=20V)	7×10^{-20}F (V$_{IN}$=20V) 5×10^{-21}F (V$_{IN}$=300V)	1×10^{-19}F (V$_{IN}$=20V) 8×10^{-21}F (V$_{IN}$=300V)

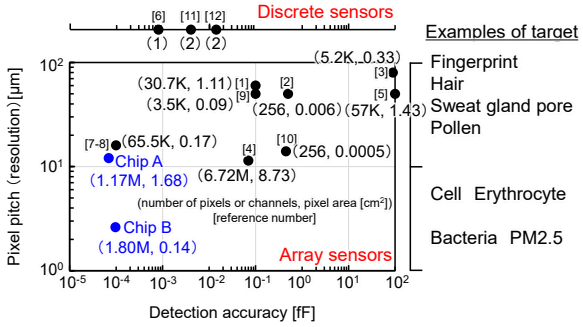


Fig. 13 Pixel pitch and detection accuracy for benchmarking with other sensors and examples of target.

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