

A 500×500 Dual-Gate SPAD Imager with 100% Temporal Aperture and 1 ns Minimum Gate Width for FLIM and Phasor Imaging Applications

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Time-gated SPAD image sensors are increasingly common in time-resolved imaging thanks to a simpler pixel and system architecture [1, 2, 3, 4, 5]. However, the gating architectures of most large-format SPAD imagers employ a single gate, thus limiting temporal aperture.

In this work, we present a 500×500 SPAD image sensor that achieves 100% temporal aperture with two contiguous gates [6]. It can generate dual-gated binary images in rolling shutter at up to 49.8 kfps. The imager, which was designed in 0.18 μm FSI CMOS technology, employs pixels with 16.38 μm pitch and 10.5% native fill factor (Figure 1). The 14-transistor pixel, whose schematic is shown in Figure 2, comprises two output bits (Out_1, Out_2), passive quenching (T2), and a 1-bit dynamic memory with reset for each output (T3, T9, T10). The boundary between contiguous gates is controlled by an asynchronous signal acting on T4 – T8, while two pull-down networks for the two output bits (T11 – T14) sharing a single output channel are used to read the corresponding bits. A cascode transistor (T1) is used, along with T2, as a resistive divider to reduce the voltage applied to the other transistors in the pixel when high excess bias voltages up to 6 V are used [7].

The timing diagram of the pixel is illustrated in Figure 3. Out_1 records the single-bit photon count of a frame while Out_2 records only those photons that have impinged outside the gate window, provided no photon was detected earlier in the same frame. The output values of 00, 10 and 11 represent the states “no photon”, “photon in gate 1” and “photon in gate 2”, respectively. Since the pixel can detect up to only one photon in a single frame, the total count of the two gates in a frame cannot exceed 1. As the pixel output values are held constant after the detection of the first photon, the SPAD recharge is not required, thus eliminating the slower recharge-based gate edge and reducing the difference between rise and fall times of the gate. This mechanism also enables short gate windows.

The imager, as shown in Figure 4, consists of two independently operating symmetrical 500×250 arrays with uniform pixel pitch. The circuit blocks outside the pixel area include column-level gate signal trees, row selection circuit, column-level readout circuit and 4:1 multiplexers. The number of I/Os per half array was set to 125 due to the I/O pin limitations of commercially available FPGAs, power constraints, and the readout speed limitations by the output wire pull-up and pull-down networks.

A 16-bit image captured with the full array, shown in Figure 5, demonstrates the operation of both sides of the array with no visible spatial non-uniformity. The imager achieves as low as 1 ns gate width at 40 MHz laser PRF (Figure 6), with a skew dominated by the signal propagation in the wire across each column. The phasor-FLIM results obtained using the dual-gated operation based on the methodology described in [8] are presented in Figure 7. A comparison of the visible patterns in the intensity and the relative lifetime images shows the independence of the measured lifetime on signal intensity, as expected. The reduced dispersion in the dual-gated phasor plot compared to the single-gated version at a constant frame rate demonstrates the advantages of 100% temporal aperture in terms of photon sensitivity. The lifetime dispersion is expected to exhibit shot-noise-limited behavior with an inverse proportionality between the lifetime variance and the number of recorded photons.

The performance comparison of this work with state-of-the-art medium and large-format SPAD imagers is shown in Table 1. To the best of the authors’ knowledge, it is the large-format SPAD imager with the highest number of gate channels and the shortest gate width. In addition, its spatial resolution and the DCR are among the best in the literature. The image sensor will be equipped with an array of microlenses corrected for vignetting to improve the native fill factor [9].

References

- [1] K. Morimoto et al., "Megapixel time-gated SPAD image sensor for 2D and 3D imaging applications," *Optica*, vol. 7, no. 4, pp. 346-354, 2020.
- [2] T. Okino et al., "A 1200×900 6μm 450fps Geiger-Mode Vertical Avalanche Photodiodes CMOS Image Sensor for a 250m Time-of-Flight Ranging System Using Direct-Indirect-Mixed Frame Synthesis with Configurable-Depth-Resolution Down to 10cm," in *ISSCC*, San Francisco, 2020.
- [3] A. C. Ulku et al., "A 512 × 512 SPAD Image Sensor With Integrated Gating for Widefield FLIM," *IEEE J. Sel. Top. Quantum Electron.*, vol. 25, no. 1, p. 6801212, 2019.
- [4] I. Gyongy et al., "A 256×256, 100-kfps, 61% Fill-Factor SPAD Image Sensor for Time-Resolved Microscopy Applications," *IEEE Trans. on Electron Devices*, vol. 65, no. 2, pp. 547-554, 2018.
- [5] C. Bruschini et al., "Single-photon avalanche diode imagers in biophotonics: review and outlook," *Light Sci. Appl.*, vol. 8, p. 87, 2019.
- [6] A. C. Ulku, "Large-format time-gated SPAD cameras for real-time phasor-based FLIM," EPFL, Lausanne, Switzerland, 2021. PhD Thesis.
- [7] S. Lindner et al., "A High-PDE, Backside-Illuminated SPAD in 65/40-nm 3D IC CMOS Pixel With Cascoded Passive Quenching and Active Recharge," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1547-1550, 2017.
- [8] A. Ulku et al., "Wide-field time-gated SPAD imager for phasor-based FLIM applications," *Methods Appl. Fluoresc.*, vol. 8, no. 2, p. 024002, 2020.
- [9] I. M. Antolovic et al., "Optical-stack optimization for improved SPAD photon detection efficiency," *Proc. SPIE*, vol. 10926, p. 109262T, 2019.
- [10] N. A. W. Dutton et al., "A SPAD-Based QVGA Image Sensor for Single-Photon Counting and Quanta Imaging," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 189-196, 2016.
- [11] L. Parmesan et al., "A 256 x 256 SPAD array with in-pixel Time to Amplitude Conversion for Fluorescence Lifetime Imaging Microscopy," in *IISW*, Vaals, Netherlands, 2015.
- [12] S. Burri et al., "Architecture and applications of a high resolution gated SPAD image sensor," *Opt. Express*, vol. 22, no. 14, pp. 17573-17589, 2014.

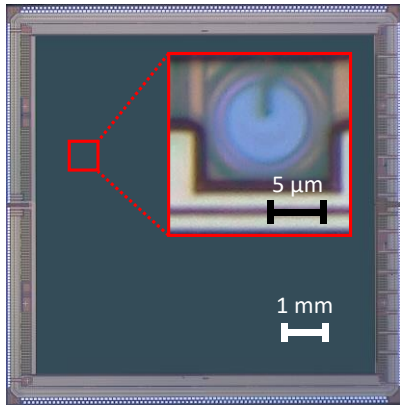


Figure 1: Chip and pixel micrograph.

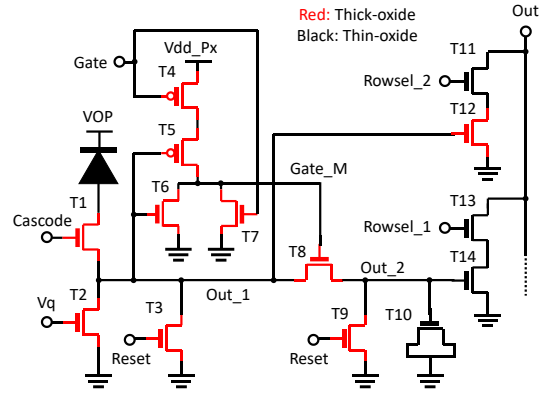


Figure 2: Pixel schematic.

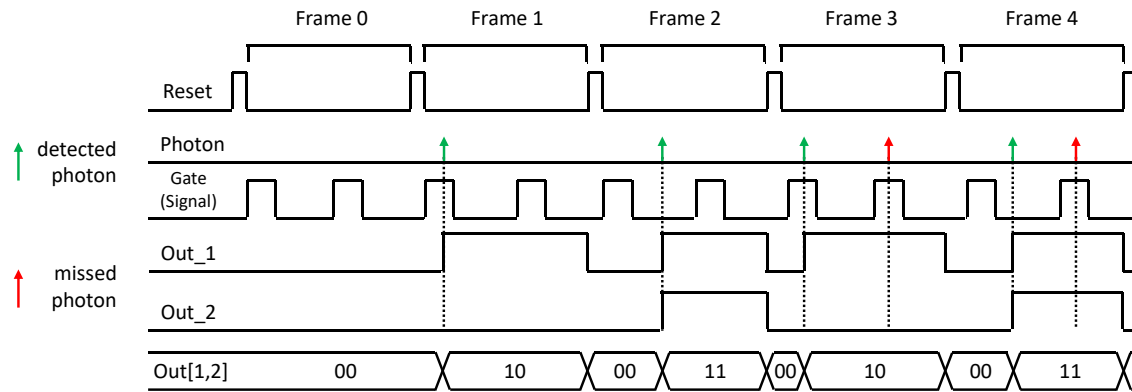


Figure 3: Pixel timing diagram. The frames represent examples of different photon arrival sequences. The pixel output of a frame is not influenced by the outputs of the previous frames.

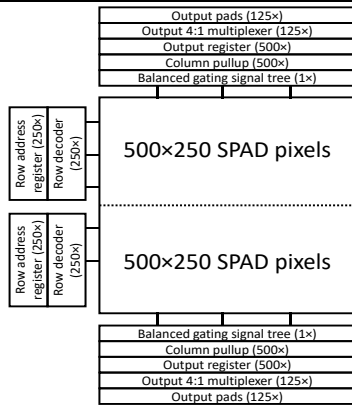


Figure 4: Sensor block diagram.

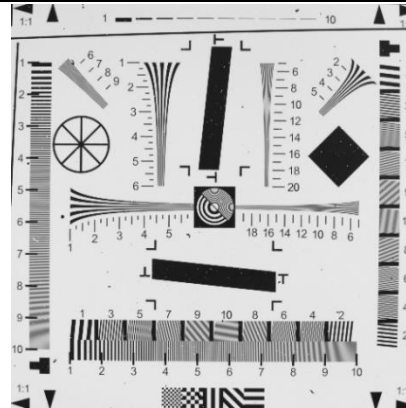


Figure 5: 16-bit intensity image of a USAF test chart.

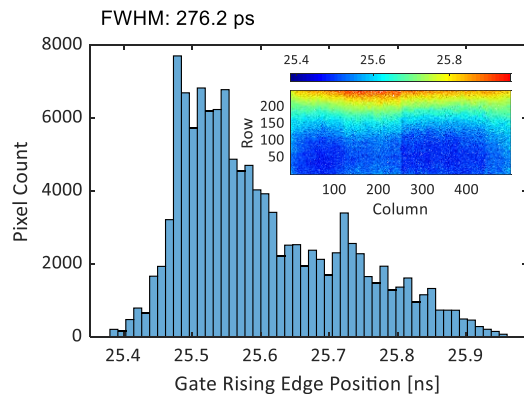
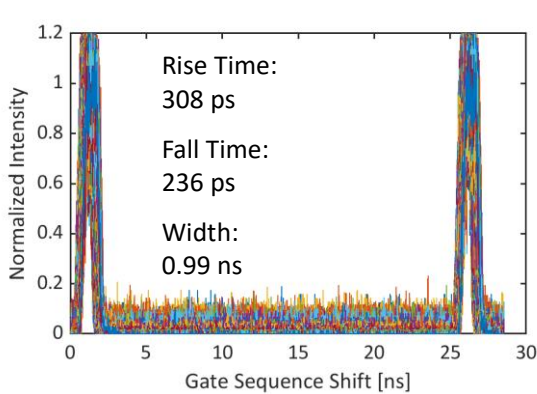


Figure 6: Left: profile of a 1 ns-wide gate at 40 MHz laser PRF. Right: gate rising edge position spatial distribution.

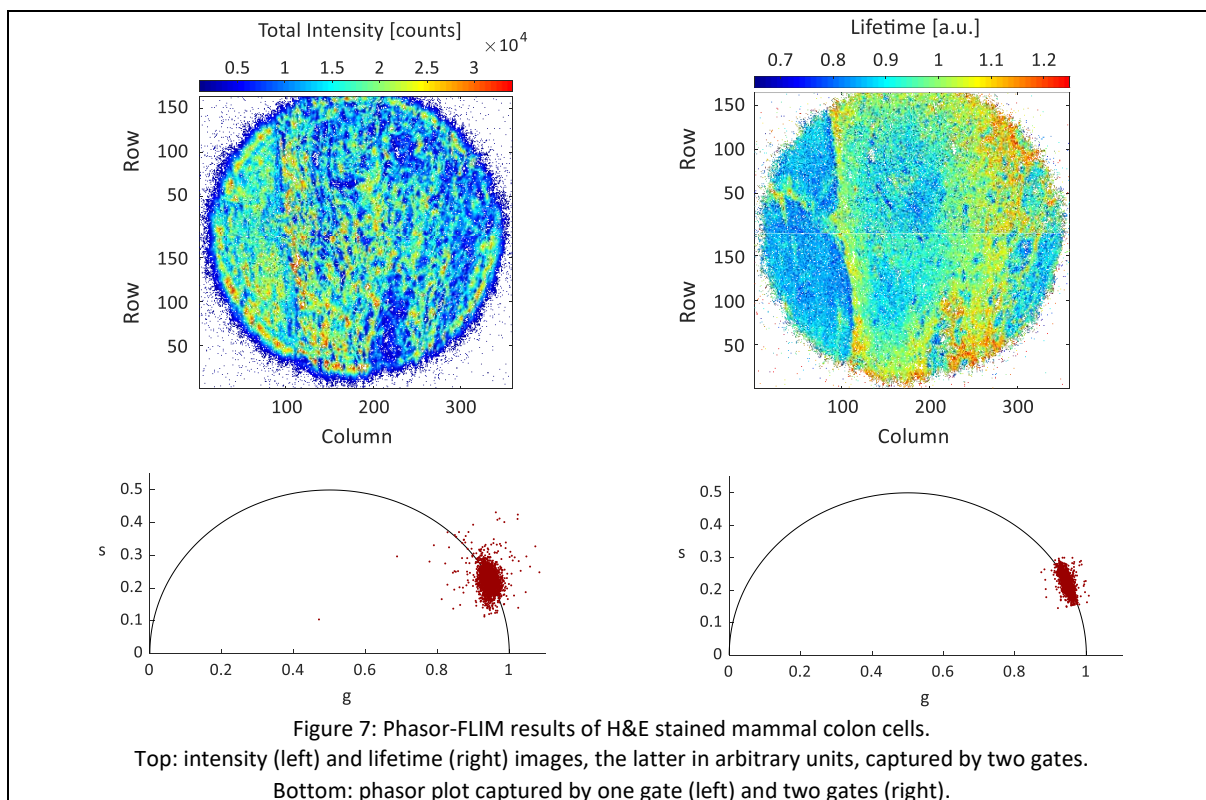


Table 1: State-of-the-art comparison between this work and other prominent medium and large-format SPAD imagers.

	This work	SwissSPAD2 [3]	MegaX [1]	[2]	[10]	[11]	[4]	[12]
Process Technology	180 nm CMOS	180 nm CMOS	180 nm CMOS	65 nm CMOS	130 nm CIS	130 nm CIS	130 nm CIS	350 nm HV CMOS
Array Format	500×500	512×512	1024×1000	1200×900	320×240	256×256	256×256	512×128
Pixel Pitch	16.38 μm	16.38 μm	9.4 μm	6 μm	8 μm	8 μm	16 μm	24 μm
Fill Factor (Native)	10.5%	10.5%	A: 7.0% B: 13.4%	-	26.8%	19.6%	61%	5%
Fill Factor (with Microlenses)	*	28%-47%	-	-	50%	-	-	60%
Chip Size	9.6×9.7 mm ²	9.5×9.6 mm ²	11×11 mm ²	-	3.4×3.1 mm ²	3.5×3.1 mm ²	5×5 mm ²	13.5×3.5 mm ²
Maximum PDP	-	~50% @ 520 nm (V _{ex} = 6.5 V)	A: 10.5% @ 520 nm B: 26.7% @ 520 nm (V _{ex} = 3.3 V)	-	39.5% @480 nm (V _{ex} = 1.5 V)	-	39.5% @480 nm (V _{ex} = 3 V)	46% @490 nm (V _{ex} = 4 V)
Median DCR	10.2 cps/px 0.36 cps/μm ² (V _{ex} = 6 V)	7.5 cps/px 0.26 cps/μm ² (V _{ex} = 6.5 V)	A: 0.4 cps/px 0.06 cps/μm ² B: 2.0 cps/px 0.17 cps/μm ² (V _{ex} = 3.3 V)	-	47 cps/px 2.7 cps/μm ² (V _{ex} = 1.5 V)	50 cps/px 4.0 cps/μm ² (V _{ex} = 2 V)	6.2 kcps/px 40 cps/μm ² (V _{ex} = 1.5 V)	366 cps/px 12.7 cps/μm ² (V _{ex} = 4.5 V)
Readout Noise	0	0	0	-	0.168 e ⁻	-	Negligible	0
Maximum Frame Rate**	49.8 kfps (1 bit)	97.7 kfps (1 bit)	24 kfps (1 bit)	450 fps	16 kfps (1 bit)	4 kfps (3-bin histogram)	100 kfps (1 bit)	156 kfps (1 bit)
Number of Gate Channels	2	1	1	1	1	1	1	1

* At least similar performance to SwissSPAD2 is expected.

** For cameras with multiple gates, a frame includes the images of all gates.