A 4.0μm Stacked Digital Pixel Sensor Operating in A Dual Quantization Mode for High Dynamic Range

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Introduction

The digital pixel sensor (DPS) architecture [1-2] has been studied with high expectation to achieve low-noise, high-speed, low-power and high dynamic range [3] in a global shutter (GS) operation employing the state-of-the-art image sensor technology. Recently, a stacked DPS pixel approach, where the CIS pixel and the pixel-level ADC and in-pixel memories are fabricated on separate, stacked wafers, has been introduced to obtain smaller pixel sizes with higher image quality [4-6]. Also, some large pixel size DPSs with time domain ADC for expanding dynamic range (DR) only in high light level were reported [3,7]. However, in a conventional DPS structure, it is quite difficult to enhance the DR by increasing the in-pixel memory size due to area limitation within a small pixel. Furthermore, readout speed and power consumption are degraded as in-pixel memory size increases.

Overlapped triple quantization DPS

To resolve the tread-offs among pixel size, power, DR and frame rate, a stacked DPS with a triple quantization (3Q) scheme was developed and reported by the authors [8]. The 3Q scheme enables an adaptive pixel wise ADC operation among the time domain quantization (TTS mode) and the linear mode ADCs with high conversion gain (PD ADC) and low conversion gain (FD ADC) for various light conditions in a single exposure. As a result, DR extends toward both bright and dark conditions and 127dB DR has been achieved. This DPS can operate in a GS mode and features high dynamic range (HDR), low power consumption and small form factor aiming for mobile computer vision applications. Prior to the development of this DPS, a proof-of-concept device was designed, fabricated and characterized to verify the basic operation of the combined quantization scheme with a time domain quantization and a linear ADC. The simplified scheme of dual quantization (2Q) enables further pixel size reduction for the DPS-HDR feature. This paper reports its operating principle, pixel structure and characterization results.

Pixel structure and 2Q scheme design concept

The sensor operates in a time domain quantization mode and a single CG linear ADC mode for extending DR. By adopting the time domain and the linear ADC modes for bright and dark conditions, respectively, high saturation level and low dark noise can be achieved by the pixel simultaneously. A schematic diagram of the stacked pixel structure is shown in Fig. 1. The pixel circuit is formed on a two-wafer stack consisting of a CIS layer (top) and an ADC layer (Bottom). This stacked DPS structure has the advantages of small pixel size, low parasitic light sensitivity (PLS) and large PD fill factor, despite of the large number of pixel transistors. The CIS layer circuit consists of a conventional 4T pixel and an in-pixel bias transistor (V_{BIAS}) to achieve pixel-parallel GS operation. The ADC layer consists of a comparator, 9-bit SRAMs and a single-bit state latch which controls the write state of SRAM bit-cells for adaptive mode control and includes a flag bit. This architecture enables individual pixel to select the correspondent quantization mode based on its own light level. As a result, data storage SRAM bits can be minimized for pixel size reduction.

Operation timing

Fig. 2(a) shows the timing diagram where the FD referred ramp signal V_{REF} is represented as red dotted line and the FD voltage is represented as solid lines., Fig2(b) shows the estimated photo charge (Q_{eq}) (dotted

circles) and signal charge (Q_{REF}) (solid circles) at the flipping points in FD node and Fig2(c) shows the corresponding potential diagrams at different time and under different lighting conditions. Just after the pixel reset, the comparator reset is released. During exposure, the FD potential and V_{REF} are continuously compared, and when the FD voltage reaches V_{REF}, the comparator flips, which sets the flag bit to "H" and a digital code DN (Note that DN is 8bit and goes downward over time from 255 to 0) that corresponds to the flip timing is stored in the SRAM. This time domain quantization is referred to as "time stamp" (TS) quantization. To enable the TS operation, a buried overflow path is implemented under the transfer gate TG [9] to allow signal charge to start overflowing to the FD when PD well is filled. On the other hand, if the FD voltage does not reach V_{REF} during the exposure period, the flag bit is kept at "L" and the conventional linear mode ADC takes place after the charge is transferred from PD to FD at the end of exposure, and the resulting digital code is stored in the SRAM. Throughout this operation, total static bias current of the top and bottom pixel circuits is below 100nA.

The time it takes for the comparator to flip during the exposure period is inversely proportional to the input light intensity. The equivalent signal charge obtained by the TS quantization mode can be expressed approximately by the following:

$$(N_{PD\_FWC} + N_{FD}(DN/255)) \times 256/(256\text{-}DN) \quad (1)$$

where DN is the stored TS digital code during counting down, N_{PD_FWC} and N_{FD} denote the PD FWC and the equivalent FD FWC, respectively. Therefore, the nonlinear data code in this scheme can be linearized easily by off chip data processing.

Sensor Characterization

The prototype sensor based on the proposed DPS architecture was fabricated in a 45nm CIS and 65nm logic stacked sensor process. The sensor block diagram and chip micrograph are shown in Fig. 3. For this prototype device, sensor control signals and the ramp voltage for quantization are generated off-chip using FPGA, and post digital signal processing is performed off-chip as well. Photo response characteristics are shown in Fig. 4 (left: Linear ADC mode only, center: 2Q HDR operation, right: TS mode only). Linear photo response has been obtained up to the full code (offsets are subtracted) in the linear ADC mode, while TS quantization exhibits non-linear photo response. A theoretical model of the TS quantization agrees well with the measurement data. The pixel equivalent maximum detectable signal is estimated to be $2.0\times10^{6}e^{-}$ from (1) and the measured read noise is $8.2e^{-}$. This results in 107dB DR. The latest test chip result shows that DR in this 2Q scheme can be extended to over 120dB with further ADC noise reduction and pixel gain optimization. HDR demo images are shown in Fig. 5, where the light bulb filament as well as the name card next to the light bulb can be clearly seen in the 2Q image (top left) in a single exposure. The "flag bit" mapping image is shown as well to demonstrate the per-pixel operation mode selection. Table 1 summarizes the pixel performance of this prototype device together with those of recent stacked DPSs and a voltage-mode GS CIS. Dark noise in the liner mode is dominated by noise sources in the in-pixel ADC, while the signal to noise ratio (SNR) at the middle level of two quantization modes exceeds 30dB.

Summary

This paper presents a novel two-layer stacked DPS pixel based on an advanced wafer-to-wafer hybrid bonding technology. The DPS features a 2Q scheme, which is a combination of TS and conventional linear mode ADC operations. Low power operation and single exposure 107dB intra-scene DR have been achieved with the 4.0μm pixel.

Acknowledgement

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References

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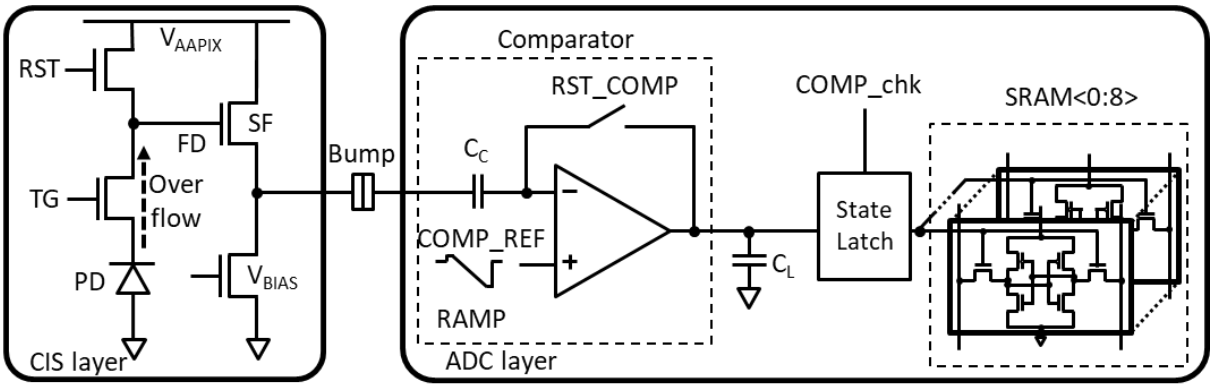

Fig. 1. A schematic diagram of the stacked pixel structure

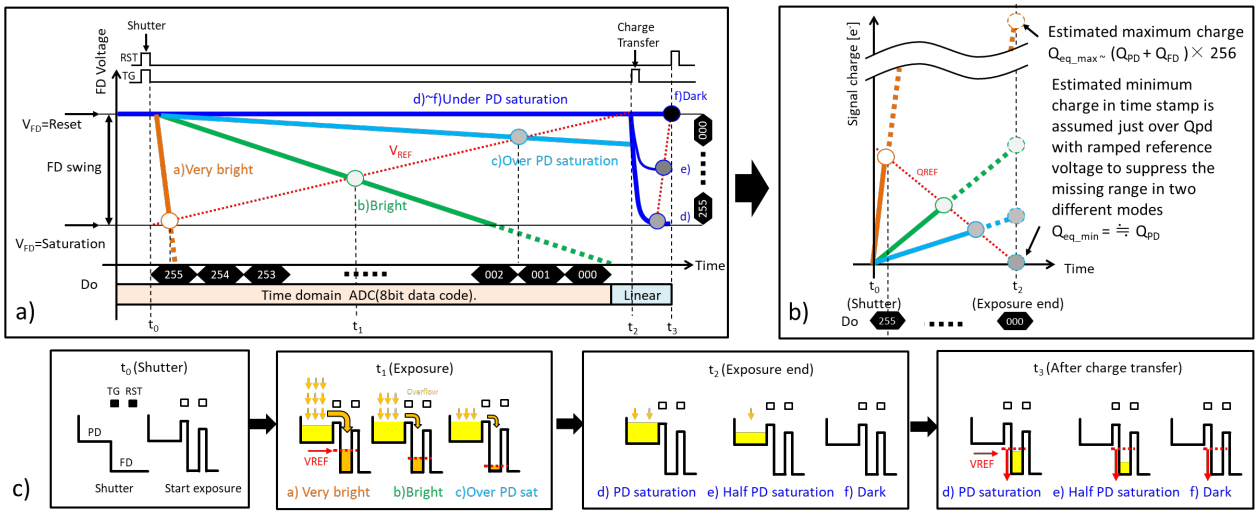

Fig. 2 (a) timing diagram with an FD referred ramp signal (red dotted line: VREF) and FD voltages (solid lines) under various light conditions, (b) estimated photo charge (Qeq) (dotted circles) and signal charge (QREF) (solid circles) at the flipping points in FD node and (c) corresponding potential diagrams at different time and under various light intensity. The FD referenced ramp voltage is compared to FD node voltage during the entire exposure period to monitor the amount of overflow charge that corresponds to photo signal. and the FD referred ramp is also used for single slope ADC operation after the exposure to quantize the photon charge stored in PD.

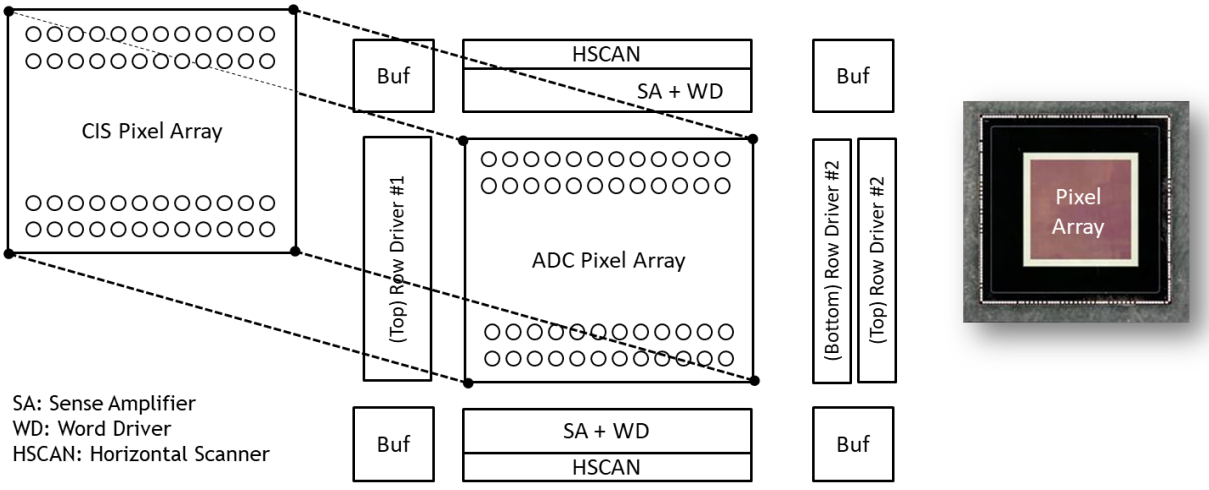

Fig. 3. Stacked sensor block diagram (left) and a packaged chip photograph (right)

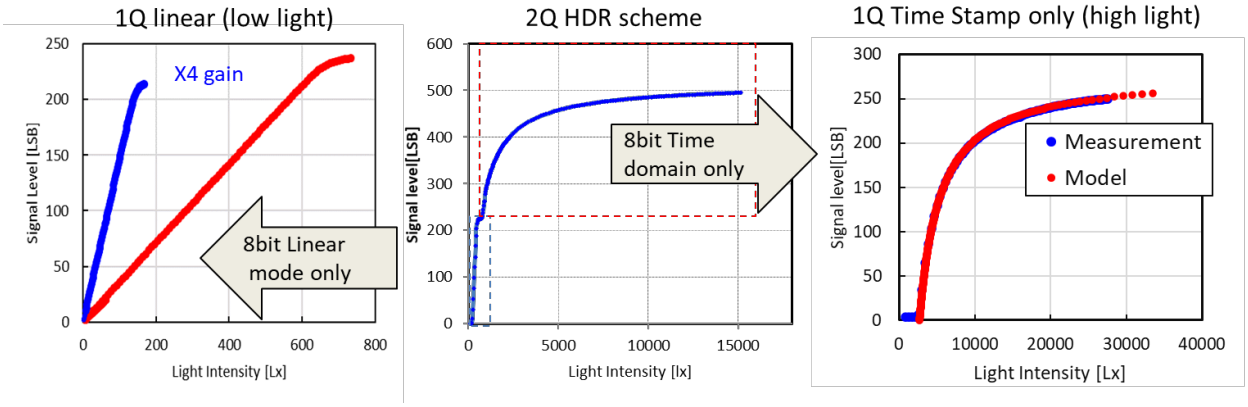

Fig. 4 Photo response plot for linear mode ADC only at gain x1 and x4 (left), 2Q scheme HDR operation (center) and time stamp ADC only and its non-linear theoretical model(right).

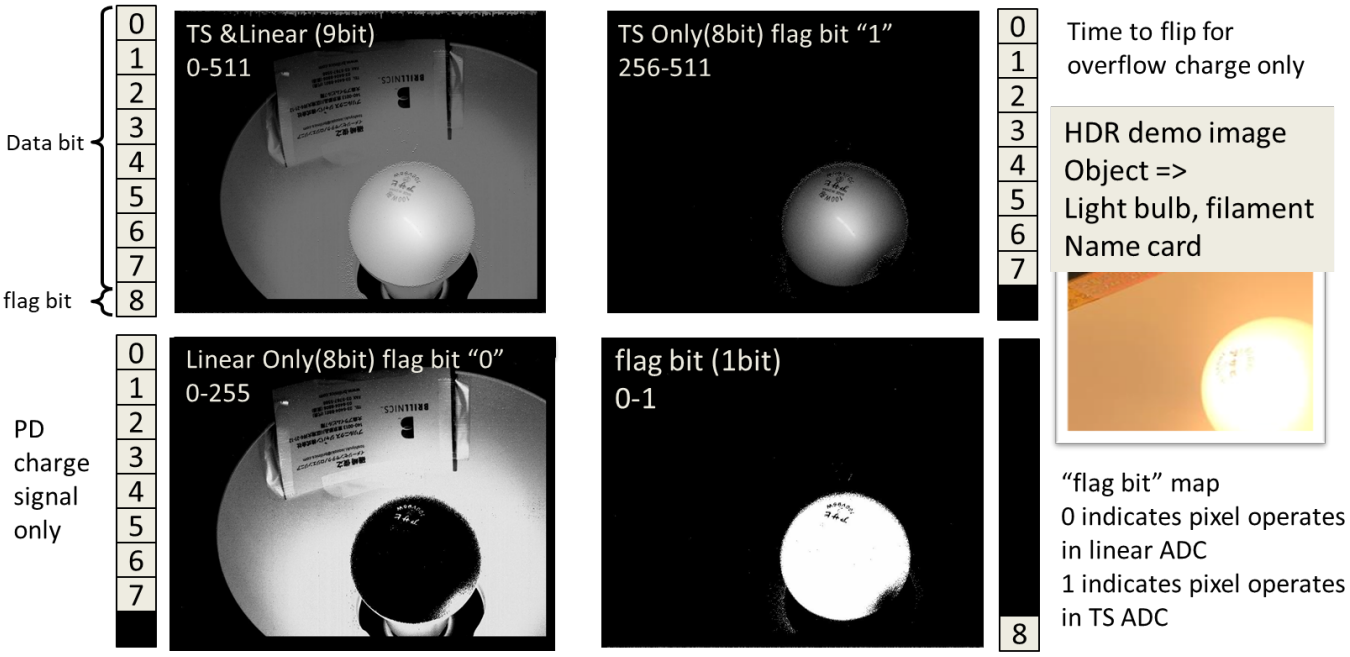

Fig. 5. HDR sample images. Allocation of the data [0:7] bits and a flag bit [8] in each image is shown.

Table 1. Sensor performance comparison for recent stacked DPS's and a VM-GS sensor.

Specification	This work	IEDM2020 [8]	VLSI2021 [6]	IISW2019 [10]	ISSCC 2018 [4]	VLSI2016 [5]
Pixel architecture	DPS (pixel parallel)	DPS (pixel parallel)	DPS (Shared)	VM-GS	DPS (pixel parallel)	DPS (Shared)
Quantization scheme	2Q (PD-Time Stamp)	3Q (PD-FD-TTS)	1Q	HCG & LCG	1Q	1Q (In-pixel LOFIC & ADC)
Pixel size [um]	4.0	4.6	4.95	4.0	6.9	6.6
In pixel Memory bit # (state bit #)	9b(1)	10b(2)	22b	NA (Off chip ADC)	15b	12b (Shared ADC)
QE (@530nm) max [%]	90 (Mono)	90(Mono)	NA	74 (G)	NA	NA
Dynamic range [dB]	107	127	74 *	77 (85)	70.2	NA
Conversion Gain [uV/e$^-$]	150	170/7	132	170/21	NA	NA
Linear full well [ke$^-$]	4/2000**	3.8/51/9000**	14	8 /35	16.6	120
Noise floor [e$^-$]	8.2	4.2	2.6	5/30	5.15	NA
Dark FPN [e$^-$]	63.9	47	1.94/0.45	4.2/16	NA	NA

*:Estimation / **:Equivalent FWC estimated with photo response plot