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4.0μm Stacked Voltage Mode Global Shutter Pixels with A BSI LOFIC and A PDAF Capability

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ABSTRACT

In this paper, two types of 4.0μm backside illuminated stacked voltage mode global shutter pixels implemented in a prototype CMOS image sensor are reported. One is a pixel with a lateral overflow integration capacitor (LOFIC) to extend the sensor dynamic range. The other is a pixel having two photodiodes and dual conversion gain which enables the phase detection auto focus capability and single exposure high dynamic range (SEHDR).

Thanks to the LOFIC and the dual conversion gain technologies, 90dB and 77dB SEHDR have been achieved in the global shutter mode.

INTRODUCTION

In recent years, demands for global shutter (GS) CMOS image sensors (CISs)[1]-[2] are increasing, especially for machine vision and IoT fields. In these fields, not only GS function, but also single exposure high dynamic range (SEHDR), high responsivity and low parasitic light sensitivity (PLS) are highly required.

At IISW2019, a stacked voltage mode (VM) GS CIS which achieved these required performances was reported by our team [3]. Fig. 1(a) shows pixel block diagrams of this CIS, which has 2 key structures.

- A 4.0μm size pixel with the pixel-level stacking technology
- On the bottom layer, 2 sets of sample and hold capacitors (SHCs) are implemented

With this structure, a GS operation with multiple signals[4], such as a high conversion gain (HCG) low noise signal and a low conversion gain (LCG) high full well capacity (FWC) signal, are realized. Additionally, low PLS is achieved with the stacked VMGS scheme.

Fig. 1(b) shows a top layer pixel circuit schematic. An additional capacitor C_S and a switch DCG for switching the conversion gain (CG) are added in the conventional 4T pixel to achieve SEHDR. In addition, a high charge density photodiode (PD)[5] is adapted. As a result, 77dB SEHDR performance was achieved in the dual CG GS mode[6].

CONCEPT

Owing to the stacked structure, changing the top layer pixel design is now possible, it is almost independent of the bottom layer process or design. Two new types of top layer pixels have been designed and combined with the previously reported bottom layer pixel as shown in Figs. 2 and 3.

a. Type1: A LOFIC-GS pixel for further DR extension

The LOFIC[7] technology is known to have potential of achieving higher DR than the dual CG pixel. While both GS and further extension of SEHDR are highly required, to achieve the GS function with the LOFIC pixel, both HCG and LCG signals must be stored in the pixel memories[8]-[9]. In other words, at least 2 sets of in-pixel memories are needed. This time, 2 sets of SHCs in the bottom pixel are used for this purpose. Fig. 4 shows the operation timing and a potential diagram of the LOFIC-GS pixel. During exposure, in case PD well is filled, overflow electrons from PD are accumulated in the floating diffusion (FD) node and C_S. Then, an HCG signal with the only electrons accumulated in PD and LCG signal with electrons accumulated in PD, FD and Cs are read out sequentially. With this operation, all the photo generated electrons that even exceed the PD FWC are detected in a single frame. Fig. 2(a) and Fig. 3(a) show a pixel cross sectional view and a schematic of this LOFIC-GS pixel, respectively. This top layer pixel has below key structures which we reported at IISW2019[10]-[11].

1. A large deep-PD expanding under C_S with BSI technology for high optical performance
2. A buried overflow path under TG and DCG for high overflow efficiency

b. Type2: A PDAF-GS pixel with dual PDs and dual CGs

The phase detection auto focus (PDAF) technology is widely known as one of important technologies for CISs. Recently, some all-pixel PDAF CISs with the dual PD type pixel[12]-[17] were reported. However, they are all rolling shutter (RS) CISs and thus less accurate auto-focusing capability is expected for vertically moving objects. To improve the auto focus accuracy, all-pixel PDAF with GS function pixel has been developed. Here, to achieve the GS function with the dual PD PDAF pixel at the auto focus phase, both the left and the right PD signals need to be stored in the

pixel memories. In this pixel, we use the 2 sets of SHCs for this purpose at the auto focus phase. In addition, they are also used for HCG and LCG signals at the image capture phase to achieve dual CG SEHDR. Fig. 5 shows the dual PD type PDAF pixel operation timings for the auto focus phase and the image capture phase, respectively. During the auto focus phase, the left and the right PD signals are read out. Then, in the image capture phase, sum of the left and the right PD signals is read out through charge binning at FD. Fig. 2(b) shows the cross-sectional view and the top view of this PDAF pixel. Fig. 3(b) shows the pixel schematic and Fig. 5(a) shows the operation timing of the auto focus phase. At first, RST and SIG levels of the left PD are stored in the SHCs. Then, these 2 levels of the right PD are stored in the other SHCs. Because these PDs are designed to obtain high FWC[5], the dual CG operation is readily available for SEHDR at the image capture phase by using the 2 sets of SHCs for HCG and LCG signal sampling as shown in Fig. 5(b).

Additionally, a near infrared (NIR) enhancement technology[18] was employed for these top layer pixels.

EVALUATION RESULTS

A prototype VMGS CIS with these pixels has been fabricated. Fig. 6 shows the chip micrograph and it was fabricated by a 45nm/65nm stacked process. It has several pixel layout pattern variations with 116×90 pixel blocks.

Fig. 7 shows photo-response and signal-to-noise ratio (SNR) of the LOFIC-GS pixel. FWC of 7ke$^-$ and 130ke$^-$ have been obtained in the HCG and LCG modes, respectively, with good linearity. Owing to the HCG operation for low illuminance, dark noise of 4e$^-$ has been obtained, which realizes 90dB SEHDR with 31dB LCG-SNR at the signal conjunction point.

Quantum efficiency (QE) of LOFIC-GS pixel and PDAF-GS pixel are shown in Fig. 8 (a) and (b), respectively. Thanks to the NIR enhancement technology, 80% peak QE and 40% QE at 940nm with a glass lid, which has 93% transmittance were realized. Also, no degradation of QE performance was observed in PDAF-GS pixel despite of the split PD structure.

Fig. 9 shows photo-response and SNR plot of PDAF-GS pixel. When both signals of the left and the right PDs are read out in the image capture phase, linear FWC was 35ke$^-$ and dark noise was 5e$^-$. As a result, 77dB SEHDR-GS has been achieved with this dual CG operation. On the other hand, when only the left or the right PDs are read in the auto focus phase, both PDs have identical FWC and responsivity, which are half of total binning FWC. It suggests that good PD separation is realized with this structure.

Fig. 10 shows angular response (AR) of the PDAF-GS pixel. Owing to the BSI PD, the broaden angle dependence has been obtained. Symmetrical characteristics with the signal cross point at 0° have been obtained, though the μlens and optical structure are not optimized yet.

Table I shows performance summary. Owing to the stacked VMGS structure, extremely small PLS has been achieved. With the BSI LOFIC pixel for the top layer, DR was extended to 90dB with GS operation. With the dual PD PDAF and dual CG pixel for the top layer, PDAF function and 77dB SEHDR with GS have been achieved.

CONCLUSION

Utilizing the 4.0μm VMGS pixel which has 2 sets of SHCs at the bottom layer pixel, a new prototype chip with below 2 types of top layer pixel has been developed.

- Type1: A LOFIC-GS pixel for SEHDR
- Type2: A PDAF-GS pixel with dual PDs and dual CGs for SEHDR and PDAF function

Thanks to the BSI LOFIC technology, both 90dB SEHDR and GS operation have been achieved in LOFIC-GS type pixel with no degradation of optical performances. Also, all-pixel PDAF function in the GS mode has been confirmed in PDAF-GS type pixel. Additionally, it has achieved 77dB SEHDR with dual CG readout at the image capture phase.

ACKNOWLEGMENT

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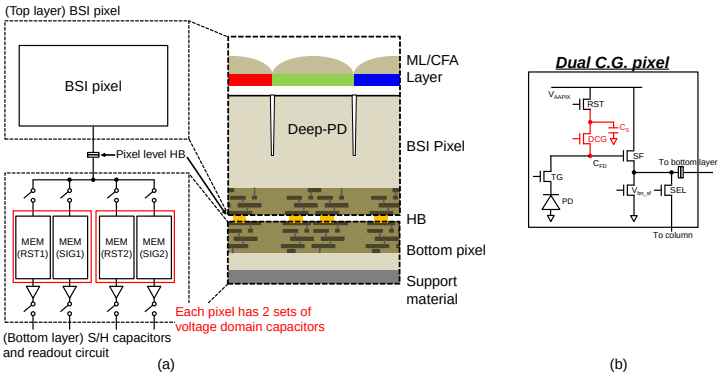


Fig. 1 Schematic diagrams of the stacked VMGS pixel

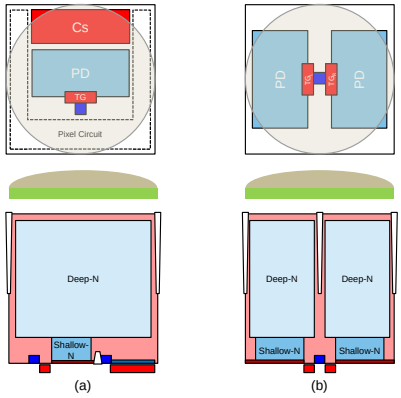


Fig. 2 Top layer pixel of (a)LOFIC-GS (b)PDAF-GS

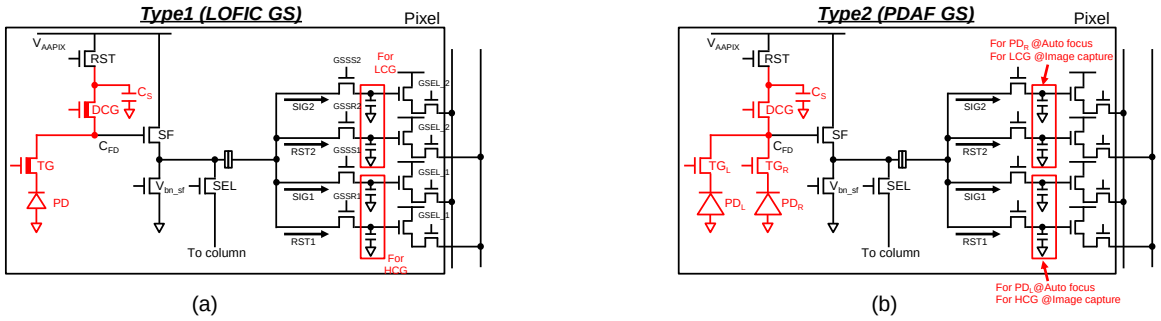


Fig. 3 Two types of pixel circuits (a) LOFIC-GS (b)PDAF-GS

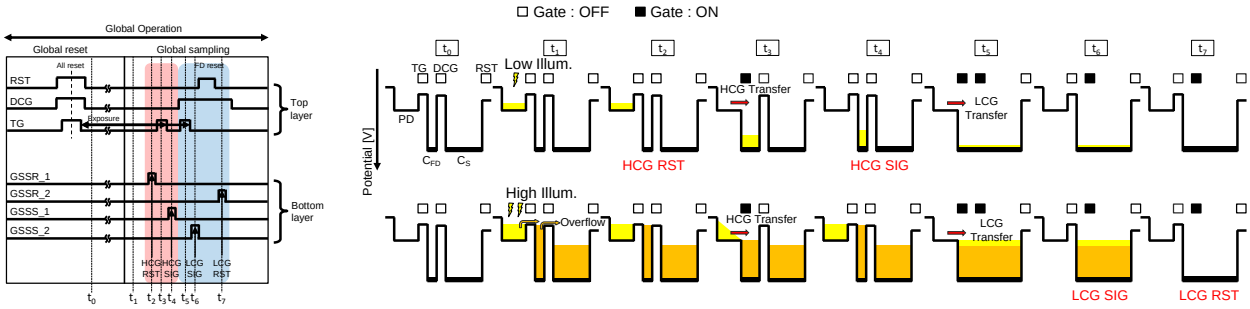


Fig. 4 (a)Operation timing and (b)potential diagram of LOFIC-GS

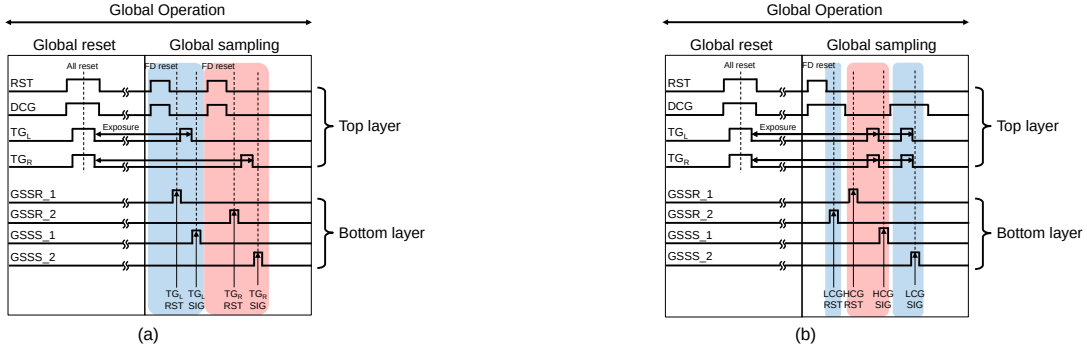
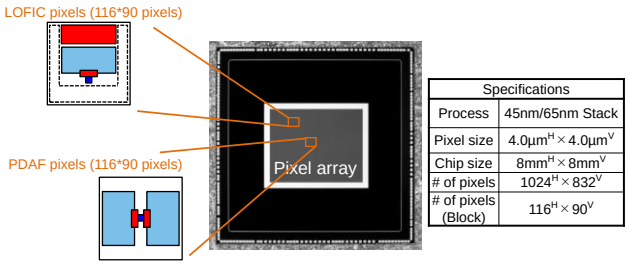


Fig. 5 Operation timings for PDAF-GS (a)Auto fucus (b)Dual CG SEHDR image capture



Specifications	
Process	45nm/65nm Stack
Pixel size	$4.0\mu m^{H} \times 4.0\mu m^{V}$
Chip size	$8mm^{H} \times 8mm^{V}$
# of pixels	$1024^{H} \times 832^{V}$
# of pixels (Block)	$116^{H} \times 90^{V}$

Fig. 6 Chip micrograph

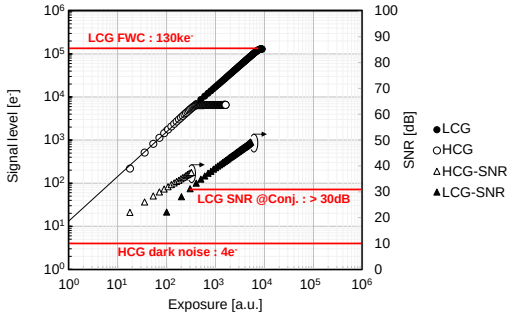


Fig. 7 Photo-response curve and SNR plot of LOFIC-GS

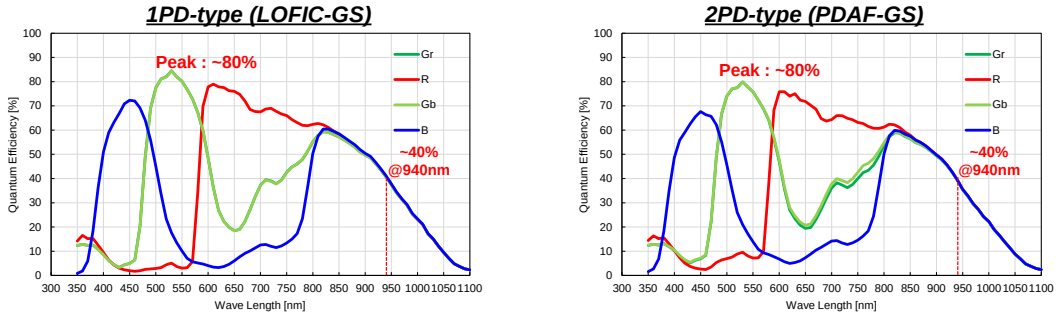


Fig. 8 Quantum efficiency (a)LOFIC-GS (b)PDAF-GS

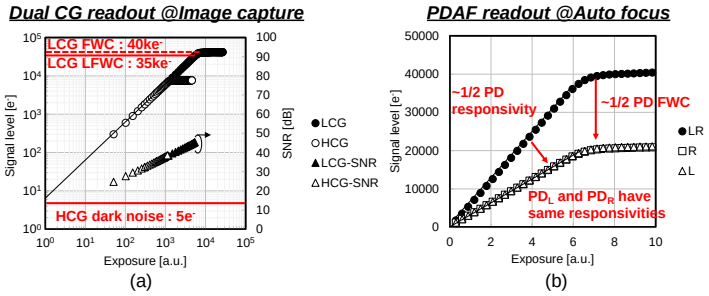


Fig. 9 Photo-response curves of PDAF-GS pixel

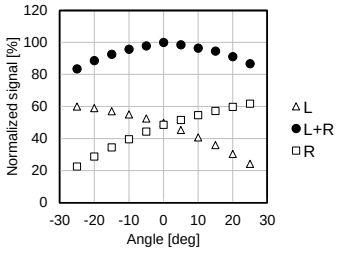


Fig. 10 Angular response of PDAF-GS pixel

Table I. Performance summary (a)This work (b)Comparison with other LOFIC-GS pixels

(a)

Pixel type	BSI LOFIC	PDAF DCG	Dual CG[3]
Process	45nm/65nm stack		
GS / RS	Voltage mode global shutter		
Pixel size	4.0μm × 4.0μm		
PLS	<-140dB		
LFWC (LCG)	130ke- @C_{FD}+C_S	35ke- @PD	
FWC (HCG)	7ke-		
Dark temporal noise	4e-	5e- (FD shared)	5e-
Dark FPN	4e-	5e- (FD shared)	4e-
Dynamic range	90dB	77dB	
Peak Q.E.	~80% (NIR enhancement)		74%
Q.E. @940nm	~40% (NIR enhancement)		~10%
PDAF function	No	Yes	No

(b)

LOFIC-GS comparison	This work (BSI LOFIC)	IEDM2020 [9]	VLSI symp.2017 [19]	VLSI symp.2016 [8]
Process	45nm/65nm stack	0.18μm BSI	180 nm CMOS (FEOL) /90 nm CMOS (BEOL)	45nm/65nm stack
GS / RS	Voltage mode GS		Charge mode GS	Digital pixel sensor
Pixel size	4.0μm × 4.0μm	22.4μm × 22.4μm	3.875μm × 3.875μm	6.6μm × 6.6μm
PLS	<-140dB	N/A	-83/-79dB (F10/F1.8)	N/A
LFWC (LCG)	130ke-	21.9Me-	224ke-	220ke-
FWC (HCG)	7ke-	10.3ke-	5.0ke-	N/A
Dark temporal noise	4e-	8.1e-	N/A	N/A
Dark FPN	4e-	N/A	N/A	N/A
Dynamic range	90dB	129dB	88.3dB	N/A
Peak Q.E.	~80%	N/A	N/A	N/A
Q.E. @940nm	~40%	N/A	N/A	N/A