A 12Mpixel 1.3" optical format CMOS HDR image sensor achieving single-exposure flicker-free 90dB Dynamic range in GS shutter mode and over 110dB Dynamic Range in 2-exposure ERS mode

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This paper presents a 12Mpixel 1.3" optical format global Shutter CMOS image sensor with a 4.2um pixel using lateral overflow to achieve 90dB dynamic range in single exposure pipelined GS mode and 110dB dynamic range in two-exposure ERS mode. The single exposure GS operation avoids motion artefacts seen in other HDR sensors, while the ERS mode extends DR to cover most practical situations. The Sensor is an ASIL-B compliant two-chip solution, includes Cyber Security, 2.1Gbps MIPI TX and consumes 2W at 30fps.

Automotive and machine vision applications have driven the need for High dynamic range (HDR) CMOS image sensors without motion artefacts. While global shutter (GS) image sensors have been available for quite some time, and several HDR sensors have been developed in recent years [1-7], the combination of HDR, high Global shutter efficiency (GSE) and single-exposure GS using pipeline operation remains a challenge.

In this paper, we present a CMOS Image Sensor using the LOFIC scheme to obtain flicker-free 90dB DR in GS mode with pipelined operation at 30 frames/sec and having global shutter efficiency of -86dB. The device also achieves 90dB flicker-free, 110dB DR in Electronic Rolling Shutter (ERS) mode and dynamic switching between ERS and GS mode with only two-frame loss. The device is a two-chip package level stacking device with sensor die containing a pixel array, analog readout circuit, digital data processing and an ASIC die containing further data processing and a MIPI Transmitter.

The pixel architecture in this sensor uses two integrating and two storage nodes (see Figure1). The photodiode (PD) integrates the low-light signal (Linear Exposure - LE) and the excess charge overflows (Extended exposure - EE) to the integrating node Clg. After integration, the LE signal is transferred from the photodiode to SG and the EE signal is transferred to the storage node Clgst. The LE signal path works in the charge domain with complete charge transfer, allowing Correlated Double Sampling (CDS) and thus low read noise, while the EE signal path is based on charge sharing across circuit nodes in the voltage domain which allows higher FWC. The EE signal uses Delta Double Sampling (DDS) for fixed pattern noise (FPN) correction but it does not suppress KTC noise.

Figure 2 shows the behavior of both LE and EE versus illumination. The pixel timing is such that, EE is not responsive to light until LE is saturated. Once LE and EE are read out, EE is gained-up to match the LE slope and the result added to LE to get a single linear response (HDR in Figure 3). In the combined HDR response, noise increases abruptly around the point where EE starts dominating, causing a drop in the SNR curve (see e.g. Figure 4a), since EE has both higher temporal and spatial noise than LE. This drop called transition SNR (SNR_T) is an important specification for HDR sensors and will be discussed in detail later.

Figure 2 shows the pixel fluid diagram. Due to the pixel complexity, a circular representation is used, where the left and right end are the same point. The pixel operation is as follows: 1) The integration nodes are reset and integration starts. 2) The integration is completed. 3) Charge is transferred to the respective

storage nodes. 4) The transfer of charge is completed and the shutter for the new frame can start for pipeline operation. Note that while all the charge integrated in LE is transferred to the SG (charge transfer), EE charge is only partially transferred to the CLGST (voltage transfer). This fact allows CDS for LE, but only DDS for EE is possible. Note that at this point, both PD and Clg (the integration nodes) are available to start the integration of the next frame, while the current frame data is stored in SG and Clgst (storage node) and the readout operation can start in parallel with the integration with the next frame, allowing pipeline operation. 5) EE signal is read out 6) EE reset is read out 7) The FD node is reset and LE reset signal readout. 8) The charge in SG transferred to the FD. 9) The LE signal is read-out.

Figure 3 shows the column parallel read-out chain and row circuits. A column amplifier samples and amplifies the charge from each pixel row. To enable fast readout, the column amplifier pipelines the sample and hold operation and data conversion by sampling the next pixel data while the ADC converts the current pixel data. The column parallel ADC is a low noise 13-bit SAR ADC with a voltage reference of 2V to support the large pixel swing. This large voltage reference range also helps in cancelling dark current at high temperature and high integration time without limiting FWC. A combination of internal charge pump and LDO's provide optimum voltage to maximize the pixel performance. Row Driver is placed on both sides of the pixel array to enable fast settling of pixel voltages. The digital processing pipe is optimally spread across separate ASIC and sensor stacked die to save area and power. The digital pipe includes global shutter linearization algorithm to linearize the GS LE and EE signals. Similarly, for ERS, a multiple exposure correction module linearizes the 2-exposure ERS data producing 110dB DR ERS image. Further noise cancellation, dynamic and static defect correction modules are added to improve image quality.

Figure 4a shows the SNR curves for total noise (temporal plus spatial, SNR_{Total}) in GS mode. As mentioned before, when transitioning from low-light to high-light regime, a drop is SNR is observed. The lowest point of this drop, called transition SNR (SNR_T), needs to be maximized to avoid noticeable image quality degradation. This necessitated tweaking both pixel process and design so that SNR_T is maximum. Pixel design specifications such as LE Full Well, DSNU in EE region, size of storage capacitors affect SNR_T as well as DR and read noise. As shown in Figure 4a, SNR_T @ 60C is >27dB with a DR of 90 dB.

A modified pixel timing allows for capture of two-exposure ERS image. In Figure 4b, three regions can be observed: Low-light and mid-light use the same integration time, while the high-light use a shorter integration time. In both transitions SNR_T @ 60C is >25dB. The linearized signal produces 90dB flicker-free, 110dB total DR image.

Table 1 summarizes chip performance with other sensors. The sensor can read 30 frames per second for a 12Mpixel resolution. The sensor achieves a minimum linear FWC of 105ke- and 3.5e- read noise resulting in flicker free 90dB DR in GS pipeline mode. A responsivity of 105 ke-/(lux·s) and -86dB GSE is achieved. Additionally the sensor supports ERS mode achieving 90dB-flicker-free, 110dB DR image. Figure 5 captures fan rotation in GS mode. Figure 6a, b and c shows HDR image in GS, ERS mode and LED flicker free image in GS mode respectively. The sensor die size is 23mm x 19mm, ASIC die size is 6.5mm x 6.5mm and combined package size is 25mm x 22mm. The typical power consumption is 2W.

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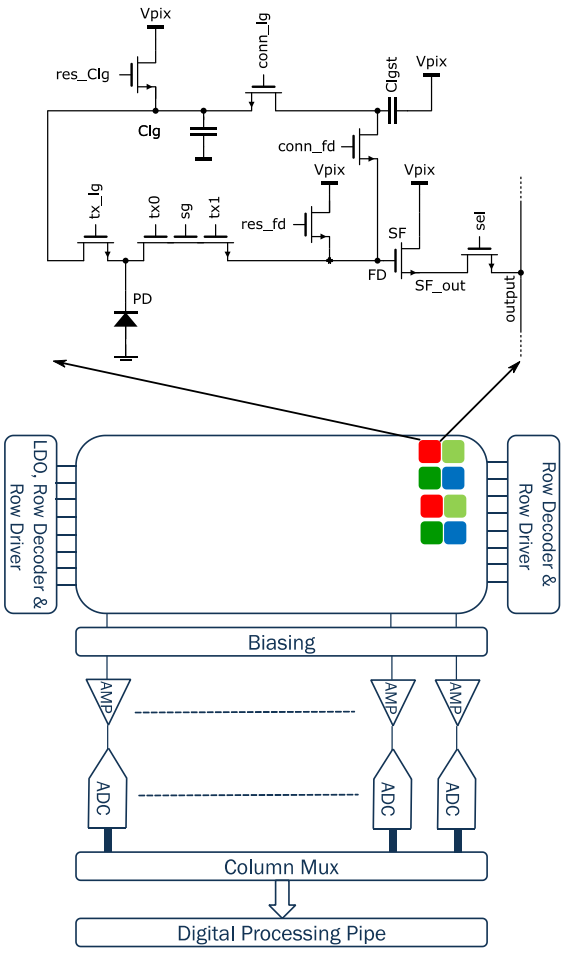

Figure 1. Sensor die block diagram.

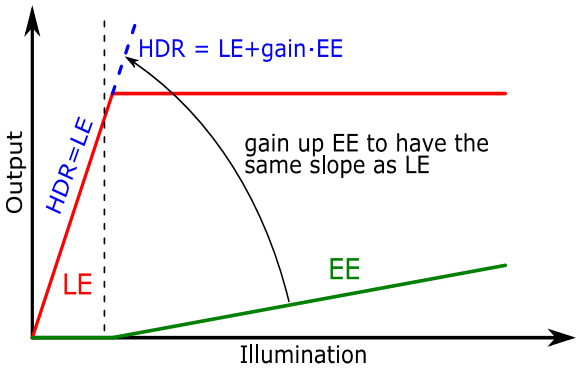

Figure 2. Linear exposure (LE), extended exposure (EE) and reconstructed (HDR) signals.

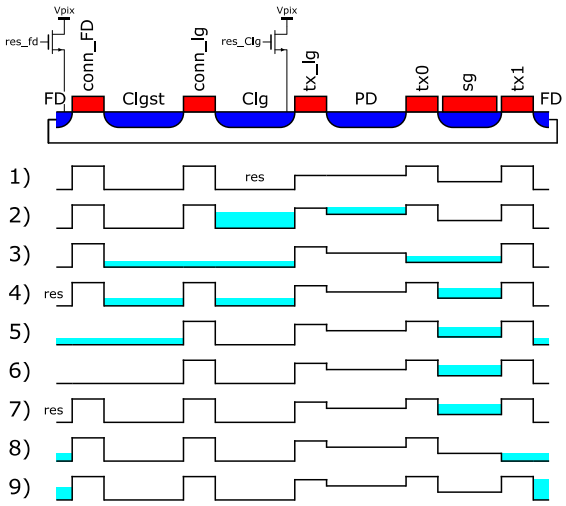

Figure 3. Pixel fluid diagram

Characteristics	This paper	[2]	[3]	[4]
GS Dynamic Range (dB)	90	83	82	93.8
ERS Dynamic Range (dB)	110	-	-	-
Pipeline GS mode	Yes	No	No	Yes
Pixel size (um)	4.2 x 4.2	5.86 x 5.86	2.8 x 2.8	15 x 15
FWC (ke-)	105	67.7	55	320
Array Size	3600 x 4096 (12M)	5M	1328 x 1029	1920 x 1080 (2M)
Read noise (e- rms)	3.5	4.8++	4.4	6.5
FPS	30fps @ 12M	30fps @ 5M	20fps @1.3M	30fps @ 2M
GSE (dB)	-86	-100	-47	-54

+ SD GSE taken for reference

++ At 18dB Analog Gain

Table 1. Comparison of single exposure GS HDR sensors

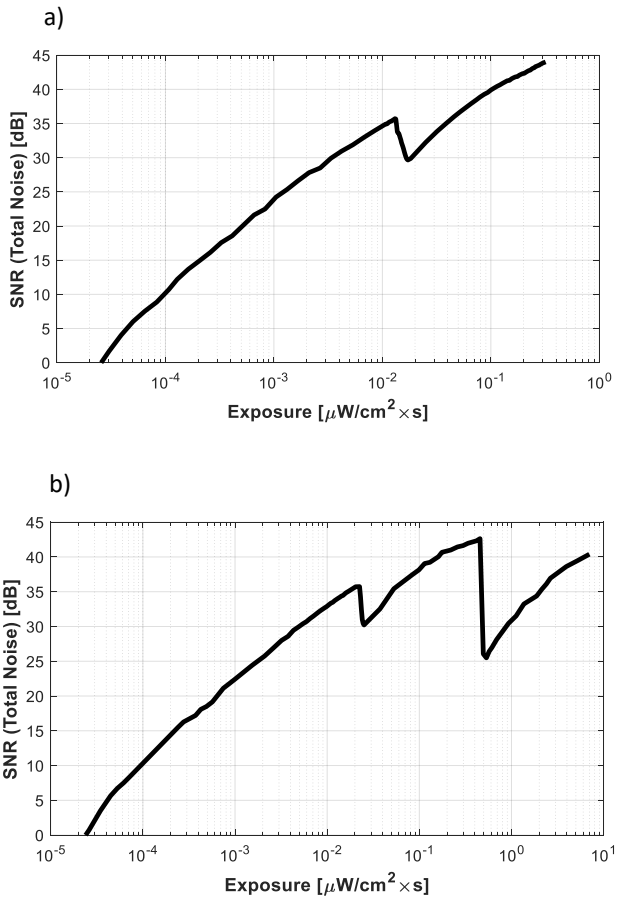

Figure 4. a) Global Shutter SNR_{Total} at 60C, b) ERS mode SNR_{Total} at 60C

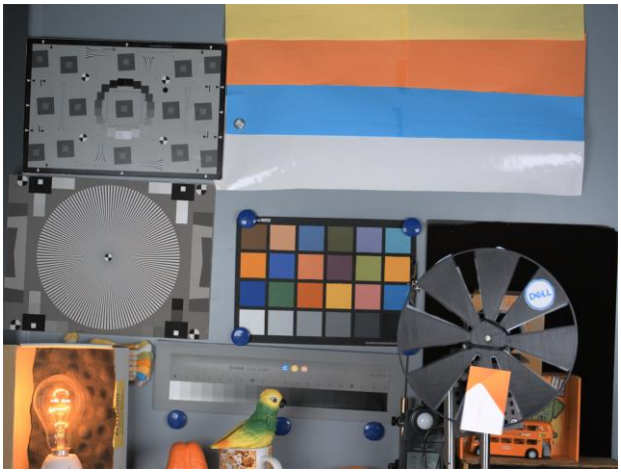

Figure 5. GS image with fan rotation

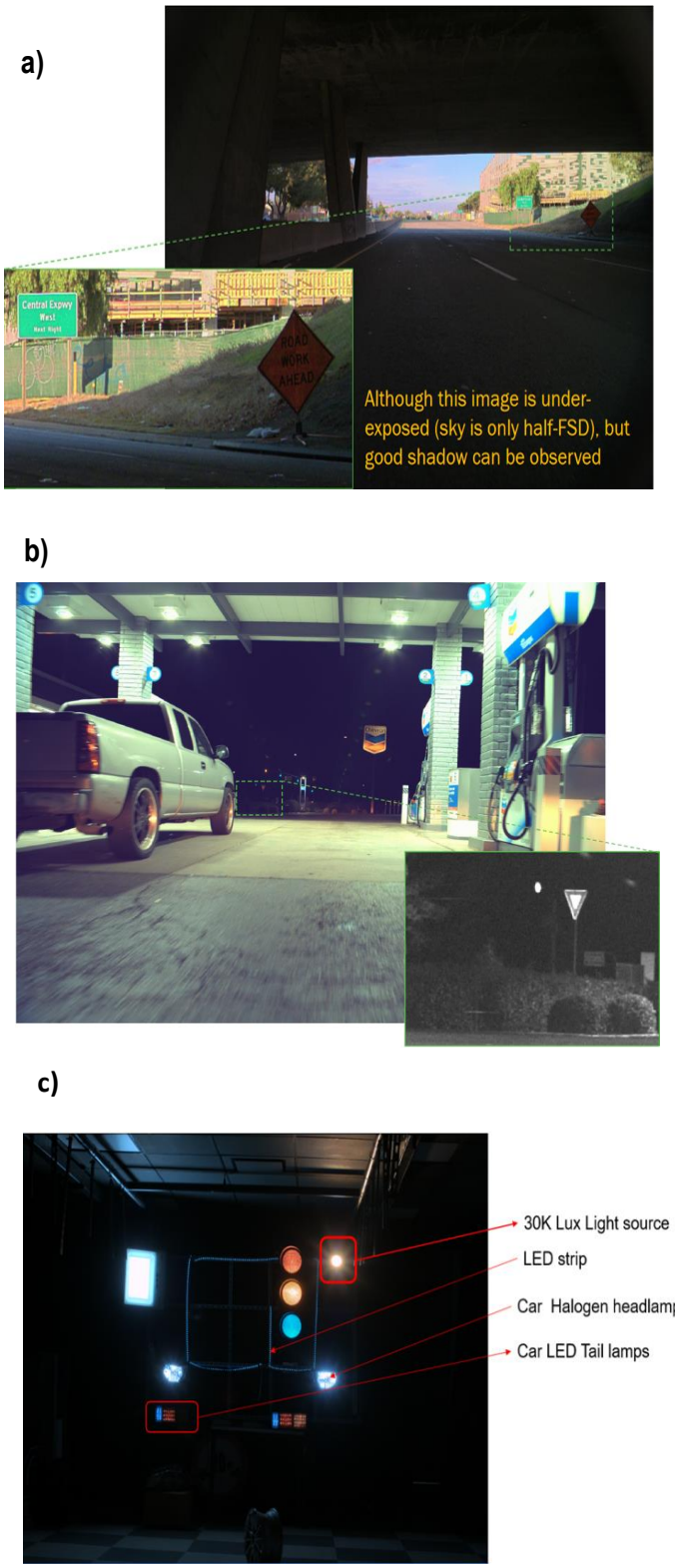

Figure 6. a) Global Shutter HDR image, b) ERS HDR Image, c) Global Shutter flicker free image