A 5.6μm Stacked Voltage Domain Global Shutter Pixel with 88ke$^-$ Linear Full Well Capacity and 85dB Single Exposure High Dynamic Range

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ABSTRACT

In this paper, design and characterization of a 5.6μm stacked voltage mode (VM) global shutter (GS) pixel with a multiple conversion gain (CG) switching function and a high charge density photodiode (PD) is reported. Through study and analysis on several types of pixel structures, an optimum PD structure has been identified to obtain high full well capacity without image lag, where 2 PDs are formed in a pixel, and in each PD, a p-type separation layer and an n-type gradient profile are formed. In conclusion, a high linear full well capacity (LFWC) of 88ke$^-$ with good charge transfer performance was obtained with a 5.6μm stacked GS pixel. With a dual CG and the split PD structure, the pixel provides 85dB single exposure high dynamic range (SEHDR) and the phase detection auto focus (PDAF) capability.

INTRODUCTION

In recent years, demand for high sensitivity GS CMOS image sensor (CIS)[1]–[6] is increased in the fields of consumer large format image sensors, machine vision, and IoT. In these fields, not only GS function but also SEHDR capability, high responsivity and low parasitic light sensitivity (PLS) are highly required. At the IISW2019, we reported a 4.0μm stacked VMGS dual CG pixel with 40ke$^-$ LFWC and 5e$^-_{rms}$ noise floor, demonstrating 77dB SEHDR[1]. Fig. 1 shows a circuit diagram and a timing diagram of the VMGS sensor. To achieve SEHDR, the photo charges in a PD is sampled and stored twice with a low-noise high CG (HCG) and high-LFWC low CG (LCG). This VMGS sensor has a dual CG pixel in the top layer and two sets of S/H capacitors in the bottom layer to sample HCG and LCG signals. By combining high LFWC PD with the SEHDR and GS function, the pixel scheme is suitable for high dynamic range GS CIS with relatively large pixel size as explained below. This time, a GS sensor with an increased pixel size of 5.6μm without changing the circuit configuration of the bottom layer is designed and verified, where a new PD structure is introduced to increase PD FWC further.

PHOTODIODE DESIGN AND SIMULATION

If an attention is not paid in designing a large pixel of a backside illumination (BSI) image sensor, the charge transfer performance would not be good enough, since the position of the maximum PD potential; V_{max}; becomes deep and far from TG. From this reason, potential profile design of a large BSI PD to obtain high FWC without degrading the charge transfer efficiency, is challenging, because high FWC and the charge transfer efficiency (i.e., image lag) are usually in a trade-off relationship. To achieve high FWC without degrading low light image quality with a low operating voltage of 2.5V in this case, advantages of the vertical p-n junction structure in the pinned PD that was demonstrated by the authors with a 3.0μm BSI pixel are utilized for larger size pixels[4]. Fig. 2 shows the examined pixel structures. Structure 1 is a conventional structure. In Structure 2, a P-type separation layer is formed in the center of the pixel to reduce V_{max} and to make the position of V_{max} shallower. In Structure 3 the photo-conversion area is divided into 2 areas, resulting in 2 PDs having a shared FD with 2 TGs in order to bring the position of V_{max} closer to TG. Structure 4 is a combination of Structures 2 and 3. The impurity profile of the PD N-layer is further tuned to secure the charge transfer performance. Fig. 3 shows potential simulation results with

TG and FD voltages of 2.5V. In Structures 1 and 3, the pinning potential was large, and the position of V_{max} is too deep. In Structure 2, although the position of V_{max} is located in a shallow region, the distance to TG is far. On the other hand, simulation results of Structure 4 exhibit low V_{max} and the position of V_{max} is shallow and the distance to TG is shortened.

CHARACTERIZATION RESULTS

A micrograph of the prototype chip and a pixel circuit schematic of the stacked pixel, which consists of a triple gain pixel on the top and the voltage sampling and readout circuit on the bottom, are shown in Fig. 4. The two sets of pixel gain can be selected by configuring the binning transistors (BIN1 and BIN2). Since it was expected from the simulation results that the charge transfer performance of Structures 1 - 3 was not good enough, Structures 4 and 3 (for a comparison purpose with the Structure 4) were implemented in a test chip. A photo-response characteristics and linearity plots in HCG operation mode of Structure 3 and Structure 4 are shown in Figure5(a) and (b), respectively. A poor charge transfer and linearity at low light levels are observed in Structure 3, while those of Structure 4 exhibit good performance. These measurement results reproduce well with the simulation result of Fig. 3. The shot noise characteristic in the LCG operation is shown Fig. 6, which shows LFWC of 88ke$^-$ and FWC of 100ke$^-$;, where LFWC and FWC are defined from a photon shot noise peak and from the maximum output signal, respectively. A log-scaled photo response and signal to noise ratio (SNR) characteristics in various gain conditions are shown in Fig. 7. As a result of high LFWC and good charge transfer performance, it has been confirmed that a linear photo response and high SNR were achieved from very lowlight to highlight with multiple conversion gains. The angular response (AR) of 85% at ± 20° was achieved as shown in Fig. 8 (upper plot; L+R signal). In addition, because of the split PD structure, the PDAF operation can be realized as was shown in Fig. 8 (lower plot; L/R signal) as well. Sample images of the GS and the rolling shutter (RS) operation are shown in Fig. 9 that demonstrate no image distortion in the GS mode, while distortion is observed in the RS mode. Characterization results are summarized in Table.1

CONCLUSION

We have designed a prototype stacked VMGS CIS with a pixel gain switching function, high saturation PD, and two sets of S/H capacitors. The pixel structure of a 5.6μm stacked VMGS CIS has achieved LFWC of 88ke$^-$ without lag by forming 2 PDs in a pixel with P-type separator and a vertical electric field in the N-type layer of the PD. Furthermore, dark random noise of 5e$^-_{rms}$ and dynamic range of 85dB are realized utilizing the SEHDR. Good optical characteristics and a PDAF function with the divided PD have been realized.

ACKNOWLEDGMENT

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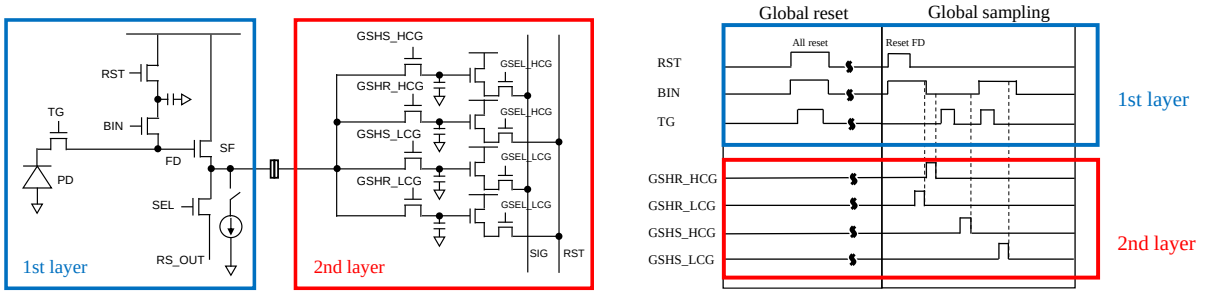


Fig. 1 A circuit diagram and a timing diagram of the voltage domain global shutter image sensor of IISW2019

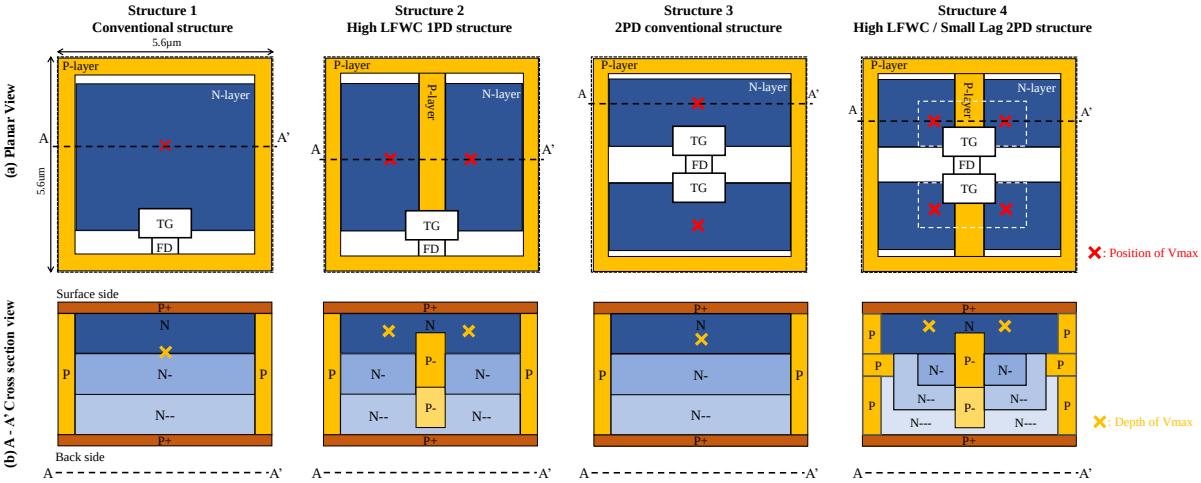


Fig. 2 Studied structures for high LFWC and low image lag

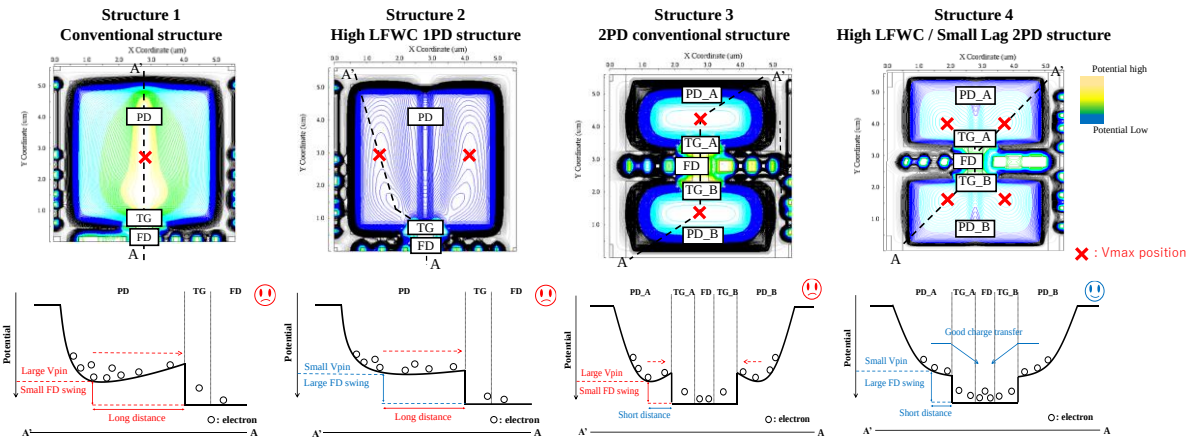
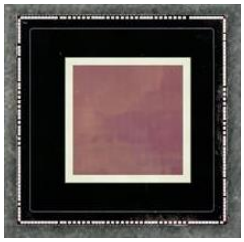


Fig. 3 Simulation results. Planer views with potential profiles (upper plots) and corresponding potential plots (lower plots)



Specifications	
Process	45nm/65nm Stack
Pixel size	5.6μm(H) x 5.6μm(V)
Chip size	8mm(H) x 8mm(V)
# of pixels	736(H) x 736(V)

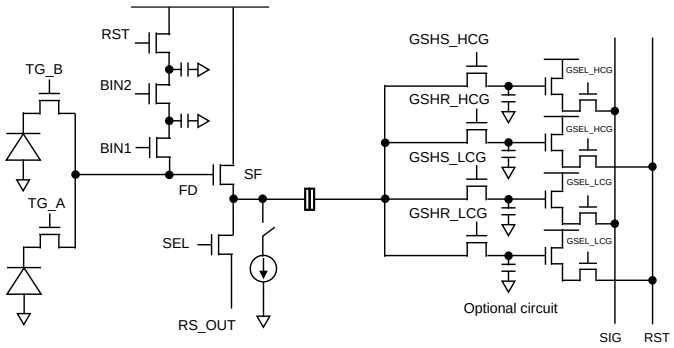


Fig. 4 Chip micrograph and circuit diagram of a triple gain pixel

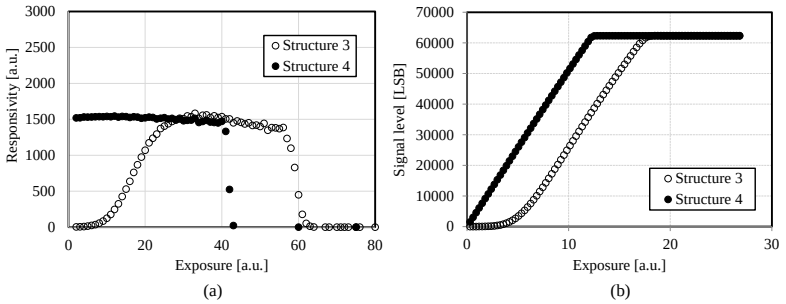


Fig. 5 (a) Photo response and (b) Signal linearity of HCG

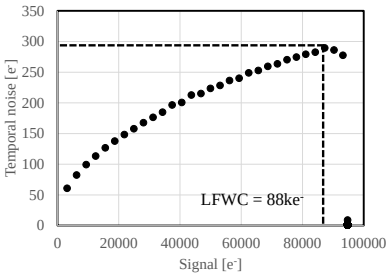


Fig. 6 Shot noise characteristics of LCG in Structure 4

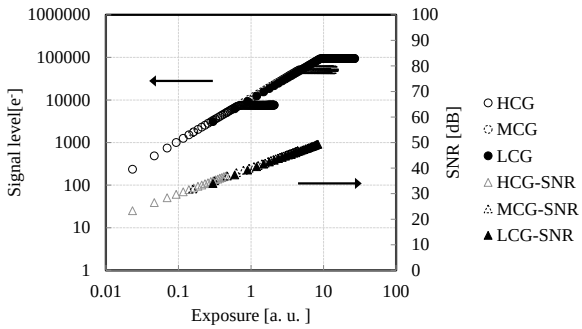


Fig. 7 Photo response and SNR characteristics in Structure 4

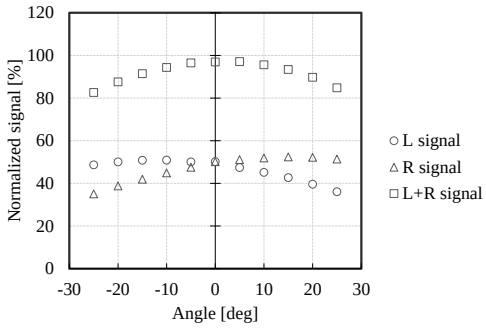


Fig. 8 Vertical angular response in Structure 4

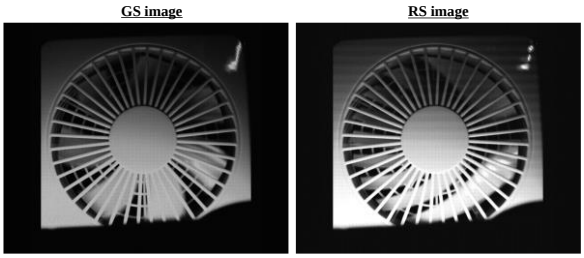


Fig. 9 Sample images of GS (left) / RS (right)

Table. 1 Performance summary

Specification	Low gain	Mid gain	High gain
Pixel size	5.6μm × 5.6μm		
Pixel operation voltage	2.5V		
QE (G) max	74%		
Angular response@+-20°	>85%		
Parasitic light Sensitivity	<-140dB		
PRNU	0.4%		
Dynamic range	85dB @ SEHDR		
Conversion Gain	11.5μV/e-	24.5μV/e-	152μV/e-
Linear full well	88ke-	50ke-	7ke-
FWC	100ke-		
Lag	< 1e-		
Noise floor	30e-	-	5e-
Dark pixel FPN	16e-	-	4.2e-