A Double Transfer 8.0μm Pixel with High Conversion Gain and Pixel Binning

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***Abstract*—**This paper presents a newly developed 8μm pixel for night vision sensor. In order to have HDR capability with both the dual conversion gain and the pixel binning, this pixel implements double transfer scheme with capacitors which temporarily stores electron charges read out from photodiode. Thanks to this new structure, parasitic capacitance to FD was successfully reduced even though FD was shared by 4 pixels. 130μV/e^- high CG and 2 × 2 pixel binning were realized and 0.96e^- rms temporal noise was achieved.

INTRODUCTION

Night vision camera requires high dynamic range (HDR) and high photo response to the image sensor. Hence comparatively large pixel size such as 8μm or greater is desirable. Furthermore multiple conversion gain (CG) and pixel binning operation are the key components for the requirements. However such large pixel namely photodiode (PD) needs relatively large transfer gate (TG) in order to transfer charge from PD to floating diffusion (FD) compared with small pixel. Furthermore as many TGs as the number of pixel binning must be connected to FD. These factors will result increased capacitance to FD which does not allow the high CG. In this work, we will report a newly developed 8.0μm pixel which has a unique double transfer scheme to realize both high CG and pixel binning.

PIXEL ARCHITECTURE

The circuit schematic of the developed 8.0μm pixel is shown in Figure 1. For pixel binning, 2 × 2 pixel sharing is adopted. Each pixel shares FD and a pixel circuit consisting of a reset transistor (RST), a select transistor (SEL), and a source-follower amplifier transistor (SF). FD can be divided into FD1 and FD2 by a gain control transistor (GC) to realize dual CG.

In order to achieve high CG even in 2 × 2 pixel sharing, a unique double transfer scheme was newly developed. Charge in the PD is read out to FD through two TGs connected serially. Top view schematic of the pixel is shown in Figure2. The 1st TG (TG1) works to read charge from PD and stores charge temporally before transferring charge to FD. Two TG1s on a same row are connected to each other and charge is stored under the shared two TG1s. The 2nd TG (TG2) is connected to the two TG1s, which transfers charge from TG1s to FD. FD is shared by two TG2s on a same column. The transistor size of TG2 was minimized to reduce capacitance to FD in order to achieve high CG, which was allowed by adopting the double transfer scheme.

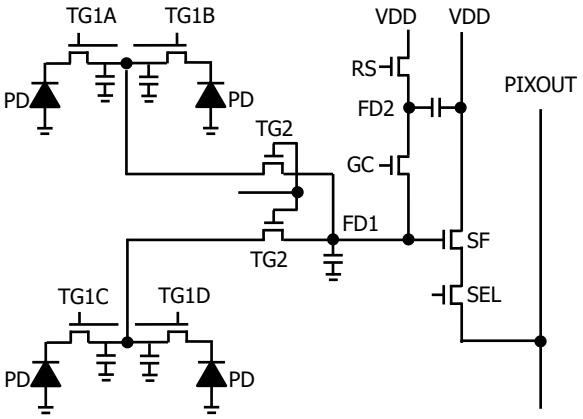

Figure 1: Schematic of the 2 × 2 Pixel Circuit.

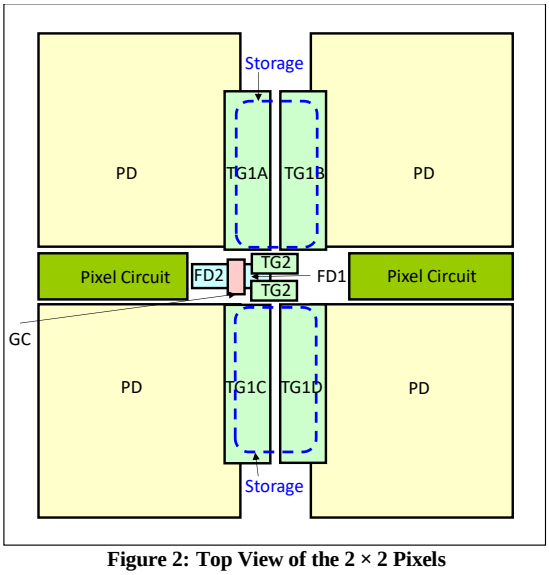

Figure 2: Top View of the 2 × 2 Pixels

PIXEL OPERATION

Figure 3 shows the pixel driving sequence for (A) the high CG mode and (B) the low CG mode. The difference between the two modes is just the gain control (GC) transistor operation. When GC is turned on during pixel activated, the low CG mode is enabled.

In the case of single pixel read out mode, this operation is carried out for each pixel sequentially. While for 2 × 2 binning pixel read out mode, the operation is performed for binned 2 × 2 pixels, thus four TG1s are driven simultaneously.

The pixel potential diagram at the high CG mode is shown in the Figure 4. (1) PD is reset before an exposure is started. After the exposure, (2) TG1 as a storage is reset again keeping TG1 low level to remove any noise like dark current and parasitic light, then (3) the reset level is sampled. After that, (4) charge in PD is transferred to TG1 and temporally stored in TG1, then (5) charge is transferred from TG1 to FD by turning on TG2. Finally (6) the signal level is sampled.

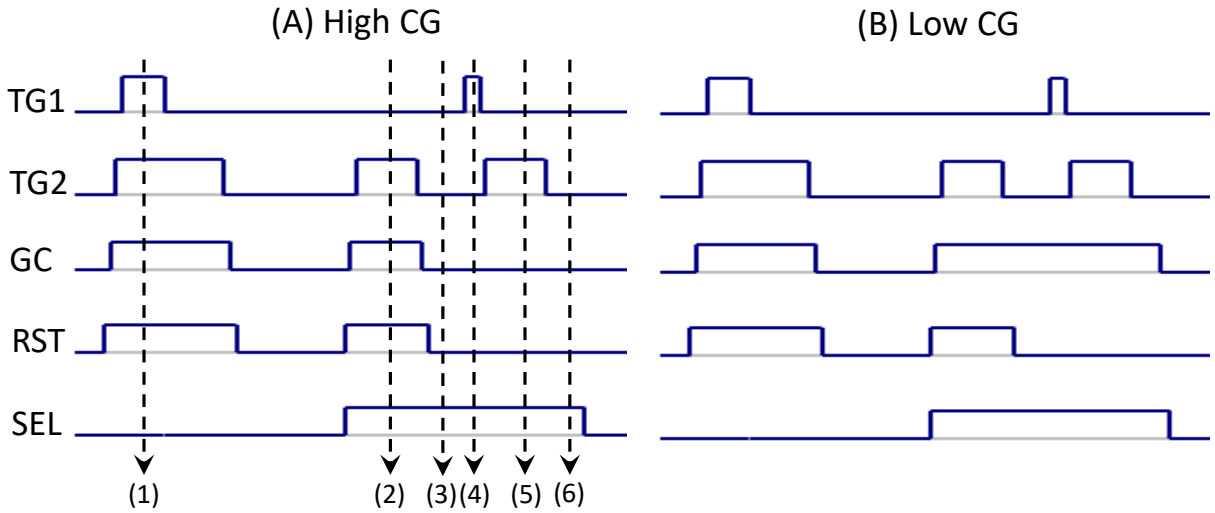

Figure 3: Pixel Driving Sequence. (A) High CG mode (B) Low CG mode.

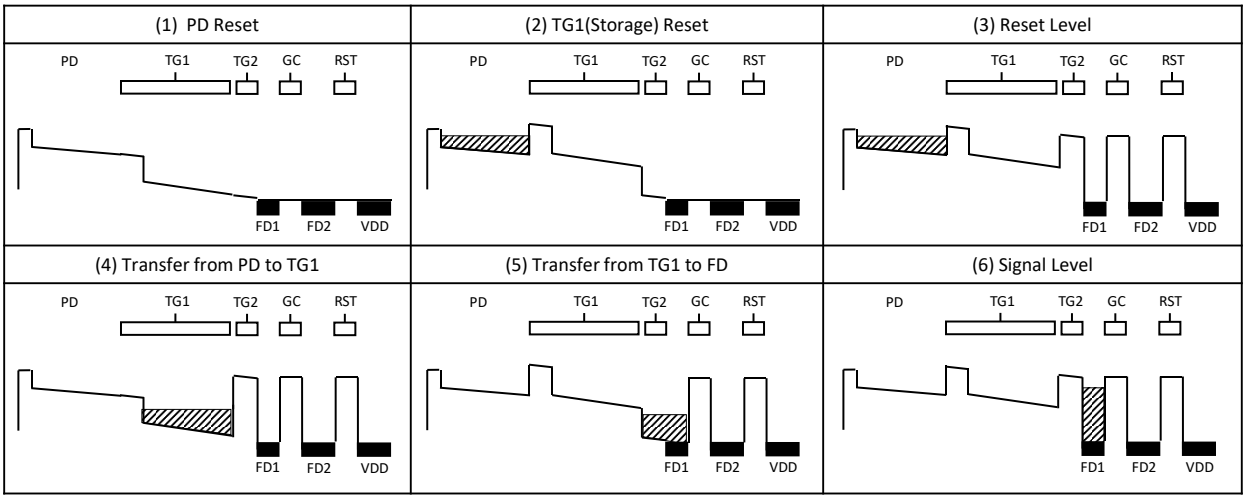

Figure 4: Potential Diagram. [(1) – (6) in Figure 3 (A)]

PIXEL DESIGN

TG1 has a near pixel size long transfer path toward FD in order to keep the channel width to transfer charge from PD to TG1 and also to store charge under TG1. Hence the complete transfer from TG1 to FD is a challenge to realize the double transfer scheme. In order to overcome the challenge, TG1 was designed based on our sophisticated fully pinned memory node for global shutter pixel as we already reported [1-3].

Figure 5 shows the top view of the electrostatic potential distribution under TG1 and TG2 during the charge transfer from TG1 to FD. Regardless of the near pixel size long transfer path, the electrostatic potential with the continuous gentle slope was successfully designed.

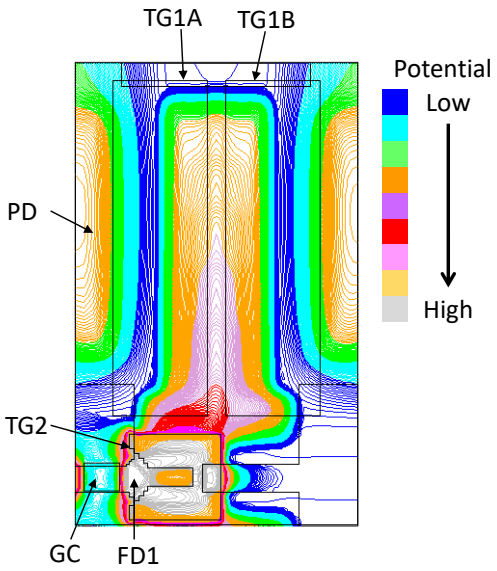

Figure 5: Top View of Electrostatic Potential Distribution. [(5) in Figure 4].

EXPERIMENTAL RESULTS

The 8.0μm pixel in this work was fabricated using our 65nm CIS process for FSI. In order to enhance QE maintaining good MTF, the Stacked Deep Photodiode (SDP) technology with N-type wafer was adopted [4].

The key pixel performances are summarized in Table 1.

Table 1: Pixel Performance.

Process Technology	65nm CIS FSI Stacked Deep Photodiode
Power Supply Voltage	3.6 V
Pixel Size	8.0 μm × 8.0 μm
High Conversion Gain @SF out	130 μV/e$^-$
Low Conversion Gain @SF out	45 μV/e$^-$
Linear FWC @single read-out (max SNR, 25C)	27700 e$^-$
Maximum Output Voltage Swing	1.6 V
Temporal Noise	0.96 e$^-$ rms

Figure 6 shows the Photon Transfer Curve (PTC) of 2 × 2 pixels with single read-out at (A) High CG mode and (B) Low CG mode. From these curves, the high CG was 130 μV/e$^-$ and the low CG was 45 μV/e$^-$ without any discrepancy of CGs in 2 × 2 pixels. From the low CG mode, the linear full well capacity of PD was calculated to 27700 e$^-$.

PTC with binning read-out mode is shown in Figure 7. The output voltage swing at the low CG mode was extended to 1.6V by the pixel binning and it is limited by FD swing.

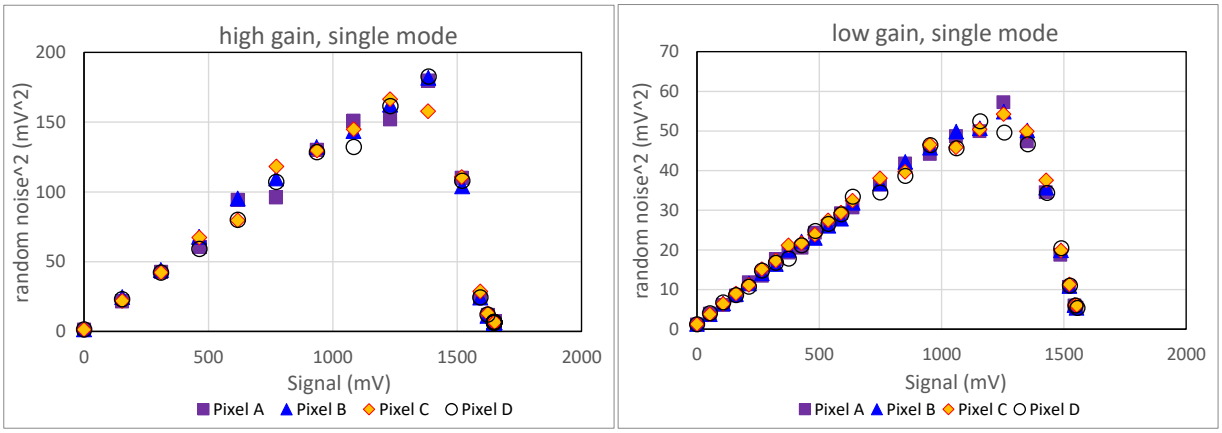

Figure 6: Photon Transfer Curve (PTC) of 2 × 2 pixels with single read-out. (A) High CG mode and (B) Low CG mode

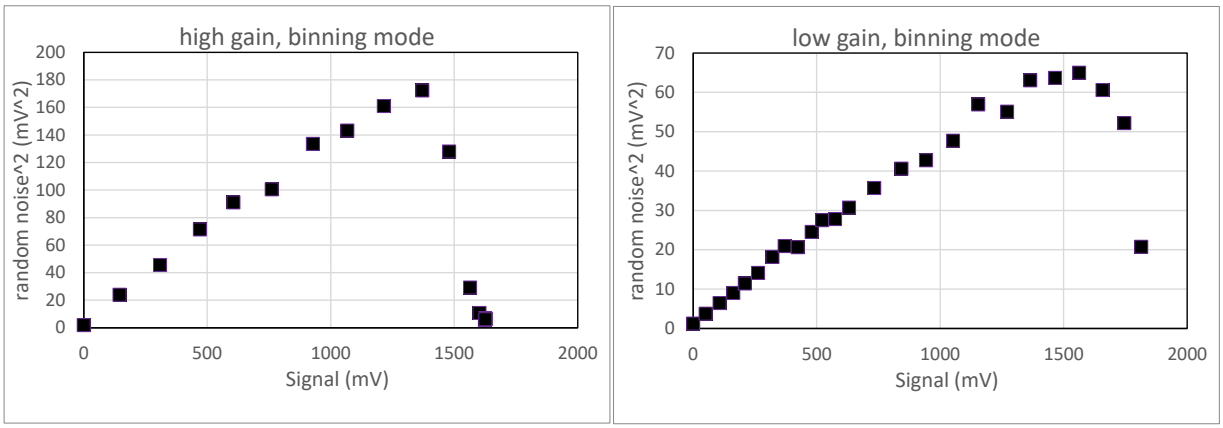

Figure 7: Photon Transfer Curve (PTC) with binning read-out. (A) High CG mode and (B) Low CG mode.

The temporal noise distribution with the high CG mode is shown in Figure 8. Thanks to the high CG 130 µV/e$^-$, 0.96 e$^-$ rms temporal noise was achieved.

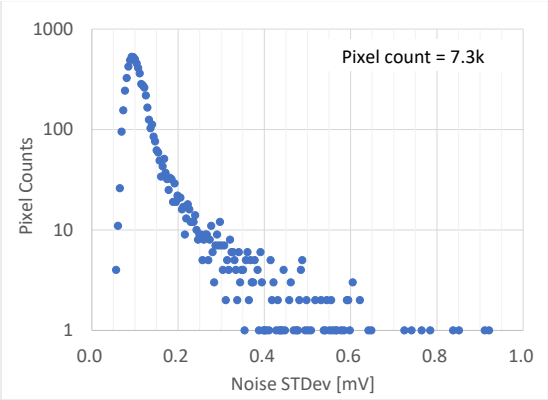

Figure 8: Temporal noise distribution at High CG mode

Finally Figure 9 shows the image lag distribution at TG1. It shows the normal probability distribution which means no image lag outlier.

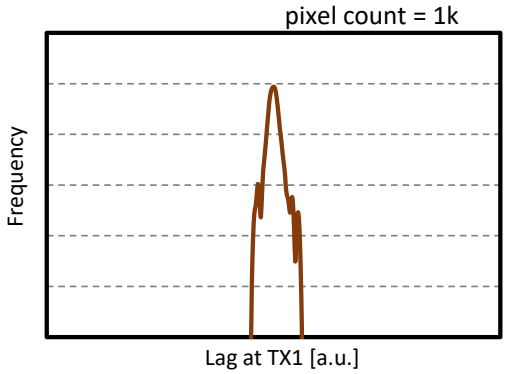

Figure 9: Histogram Image

CONCLUSION

We developed a new 8.0µm pixel for the night vision sensor, which has a unique double transfer scheme to realize both the high CG and the pixel binning. This double transfer architecture allowed the pixel to achieve both 130µV/e$^-$ high CG and 2 × 2 pixel binning. Thanks to such high conversion gain, 0.96e$^-$ rms temporal noise was achieved. Low CG was 45V/e$^-$, and linear full well capacity was 27700 e$^-$.

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