June. 14, 2022

A 64 × 64 SPAD-Based Indirect Time-of-Flight Image Sensor with a depth range of 50m

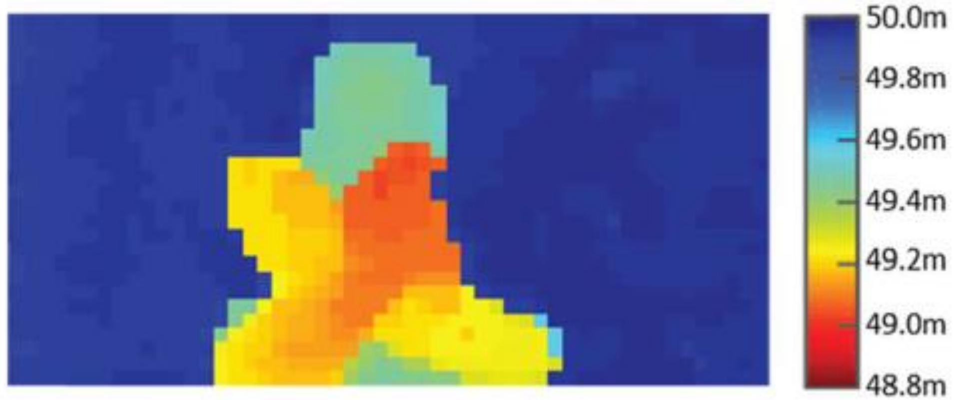
International SPAD Sensor Workshop 2022

BYUNGCHOUL PARK

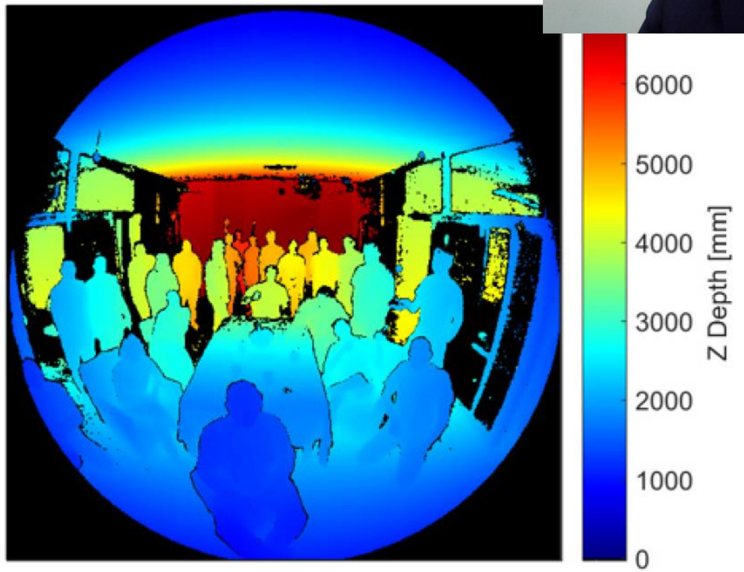
Outline

- Motivation – SPAD-based Time-of-Flight sensor
- Proposed SPAD-based iToF sensor
  - Pulse-shaping circuit
  - Analog pulse counter
- Measurement results
- Conclusion

2 types of ToF sensors



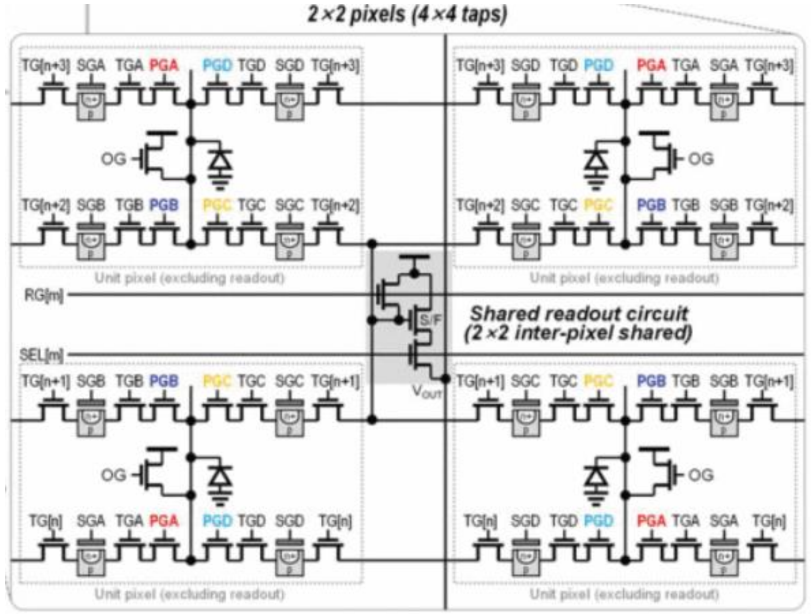
S. W. Hutchings [JSCC' 19]



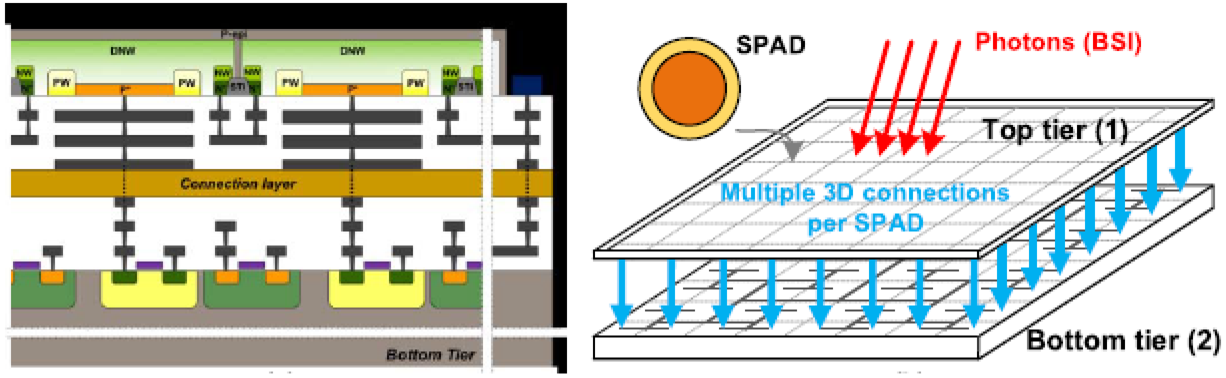
C. S. Bamji [ISSCC' 18]

- Time-of-Flight (ToF) Sensors
  - Direct: Long-range (> 100m) ☺, large pixel pitch, 3-D stacking ☹
  - Indirect: High pixel resolution, high frame rate ☺, short-range ☹

Trend in ToF sensors



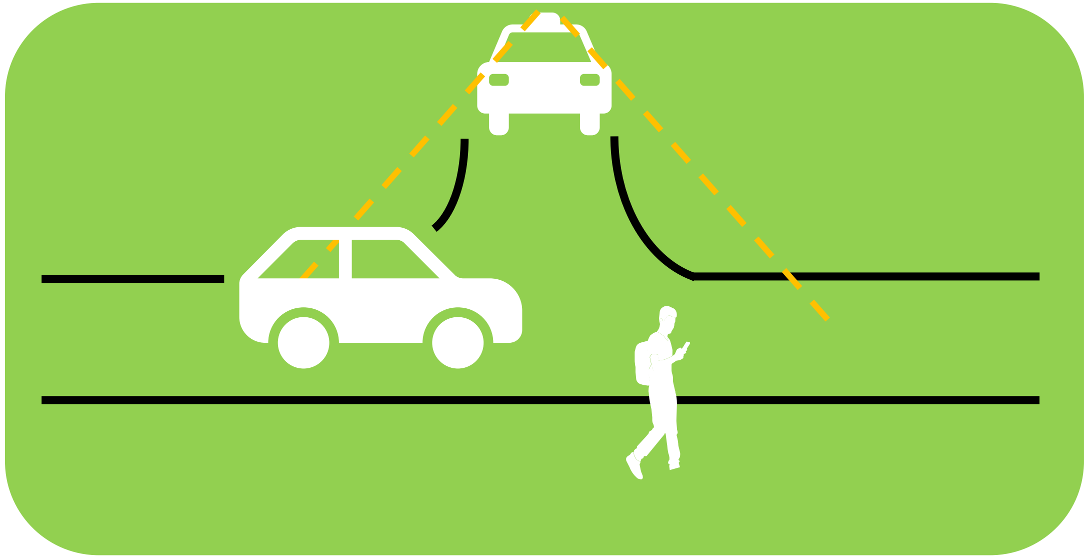
M.-S. Keel [ISSCC' 21]

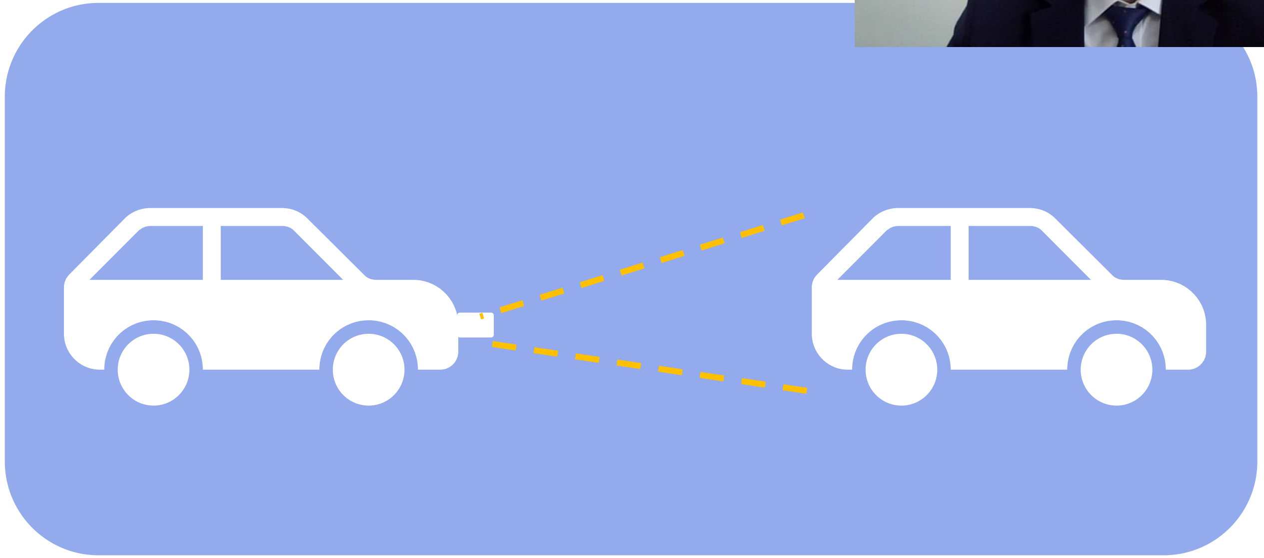


A. R. Ximenes [JSSC' 19]

- Multiple integration capacitor (iToF), up to 4 taps
- Small pixel pitch, down to 3.5 μm (iToF), 9.2 μm (dToF)
- 3-D stacked wafer (iToF, dToF both)
  - Resulting in a high production cost ☹

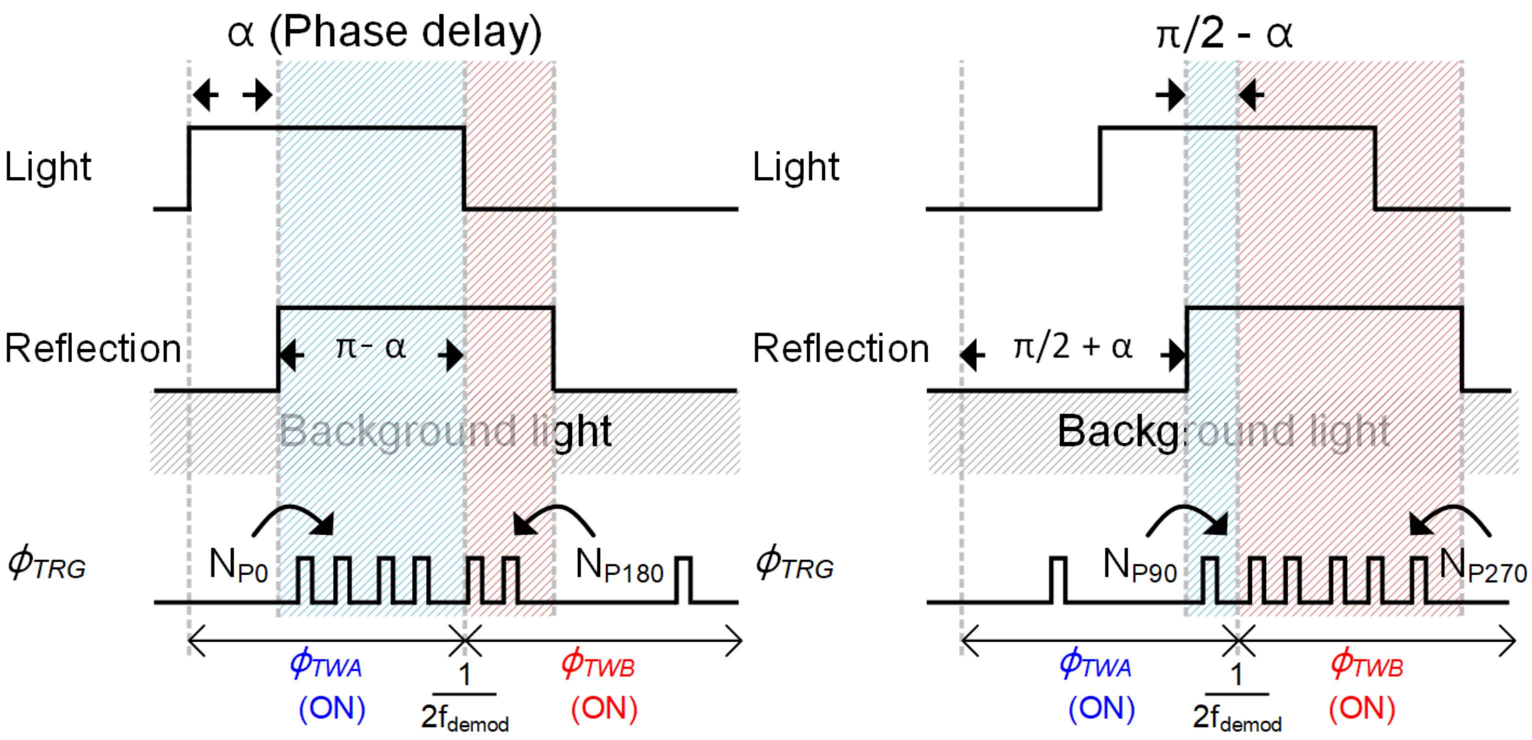
Sensor target – ADAS





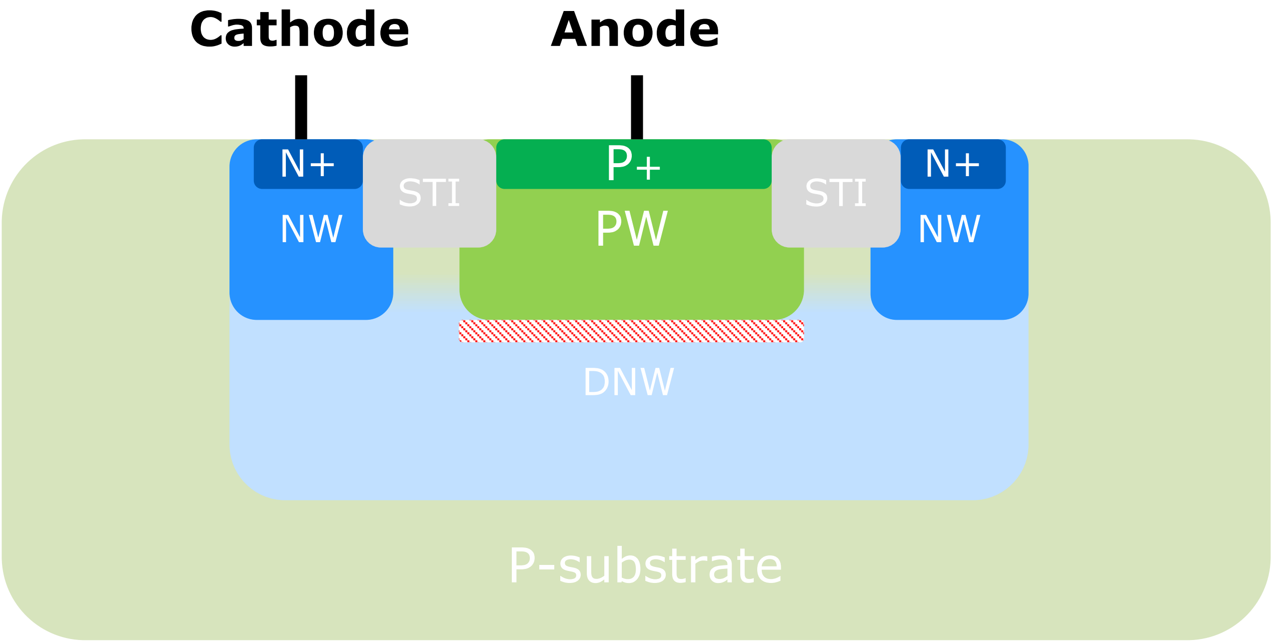
- Average of 35 m is required for emergency braking (at 100 km/h)
- Required distance: 50 m, FoV: 20 °
  - Pixel resolution: at least 60 (to detect pedestrian)
  - iToF sensor: high frame rate, high accuracy, pixel scalability✓

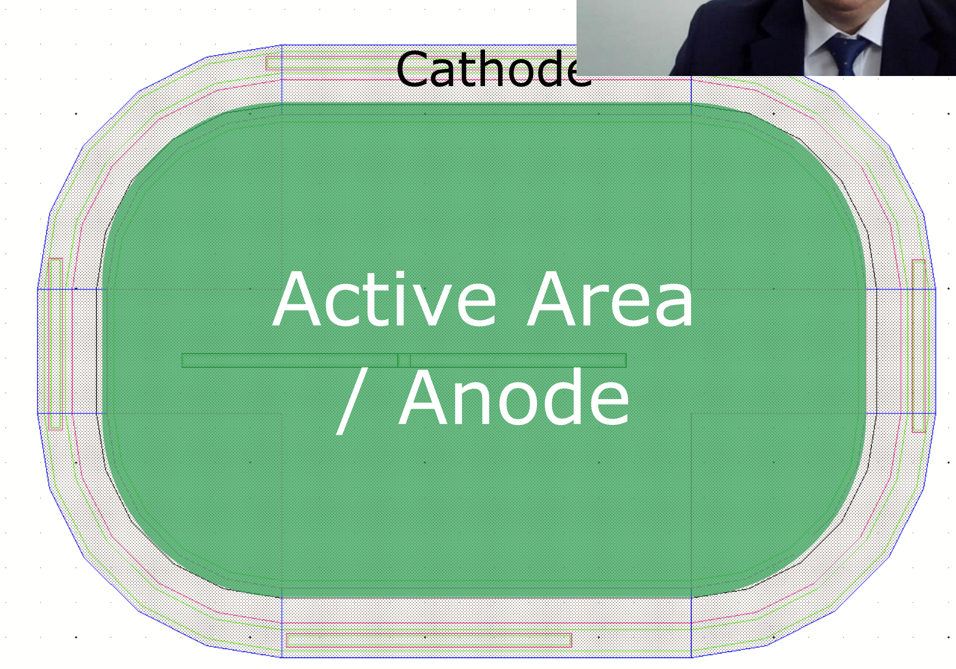
Principle of indirect ToF



- Correlation between reflected light and time-window for iToF sensors
  - Integrate photon current in selected time-window (PD)
  - Counting photon in selected time-window (SPAD)
- Immune to background light ☺ (removed as an offset)

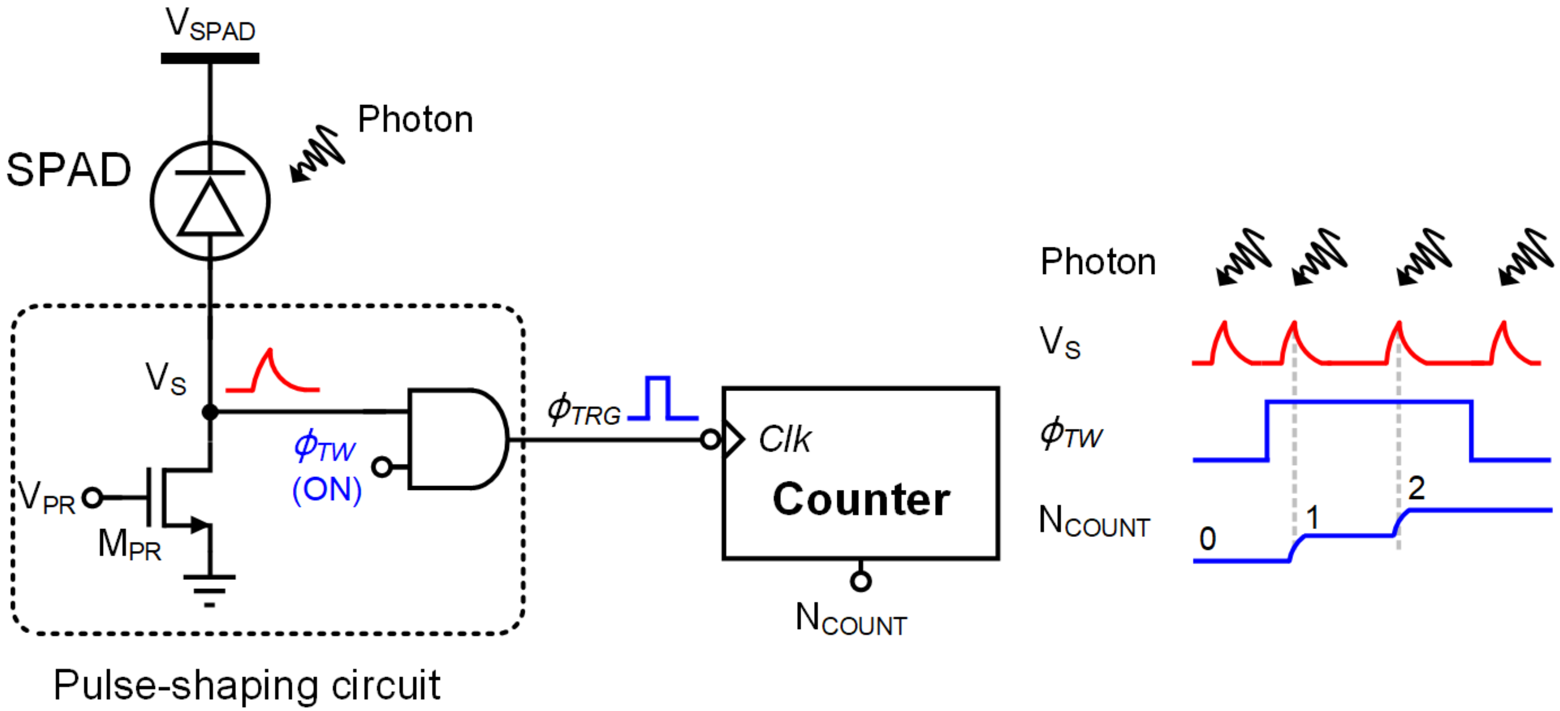
SPAD used in the proposed sensor





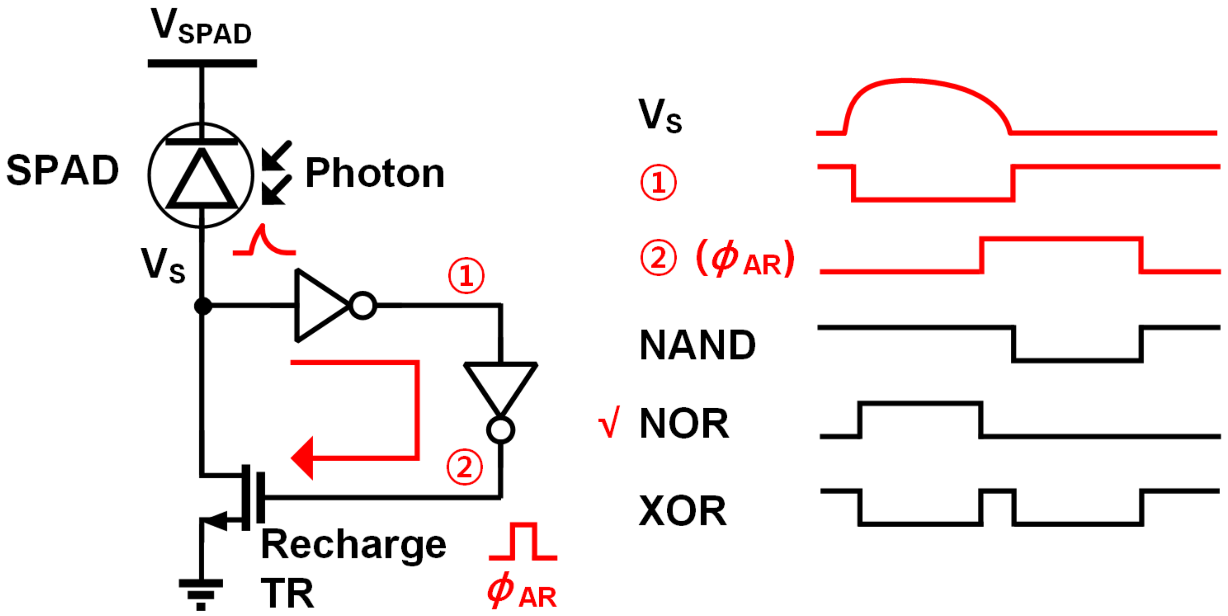
- PW / DNW junction SPAD with retrograde DNW guard-ring
  - Rounded corner shape > maximize active area
  - Integrated DNW > thin cathode (1 μm)
  - Improved fill factor > up to 50 % (previous work, SSC-L' 20)

Time-gated photon counting



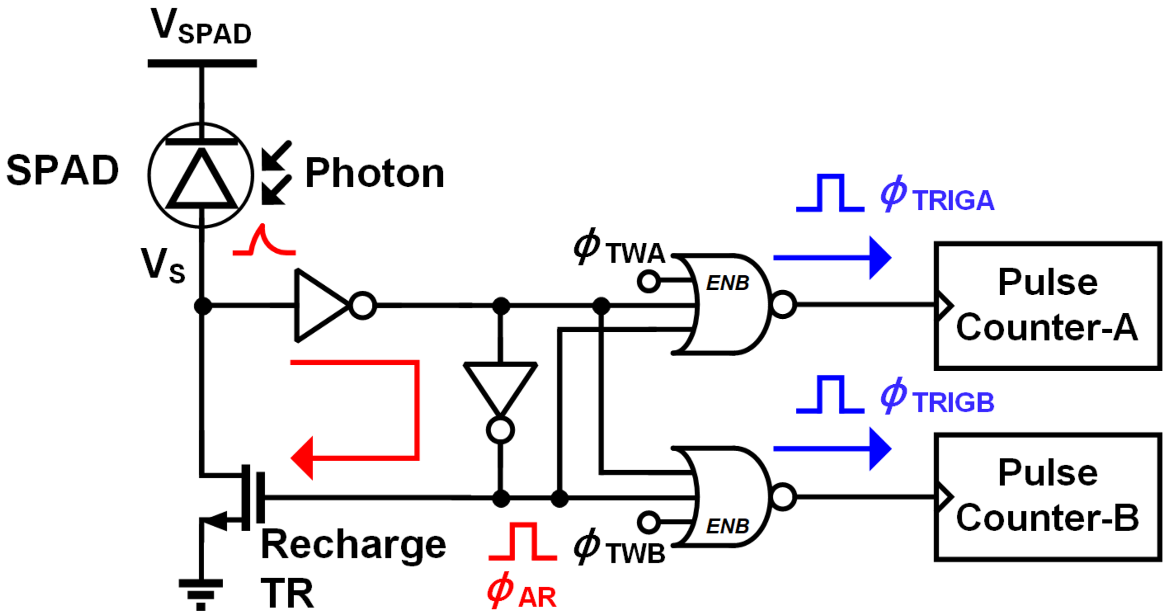
- Logic gate (pulse-shaping circuit) is attached for gating V_S
  - V_S propagates to counter only Φ_{TW} is on (enable correlation)
- However, passive recharge slows down counting rate ☹
  > requires active recharge circuit

Implementing pulse-shaping circuit



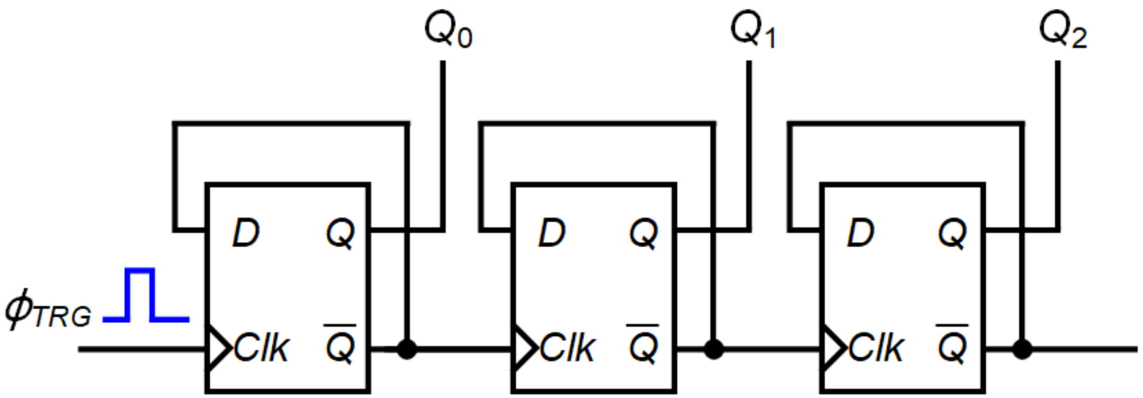
- 2 inverters are added to sharpen pulse edge of V_S
  - First inverter: skewed between P/N for threshold control
  - Second inverter: added for the polarity of the Φ_{AR}
- Pulse-shaping circuit: inverter outputs and “NOR gate”

Implementing pulse-shaping circuit

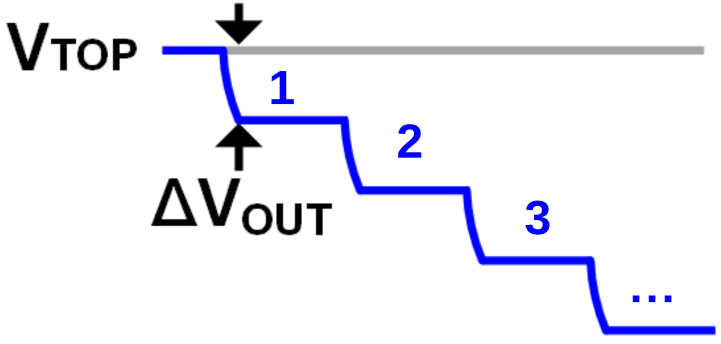


- 3-input NOR gate: gated by Φ_{TW} for time-gated photon counting
  - Operation rate of pulse counter: determined by feedback delay
- Multiple counter: motion artifact↓, light efficiency↑

Selecting pulse counter



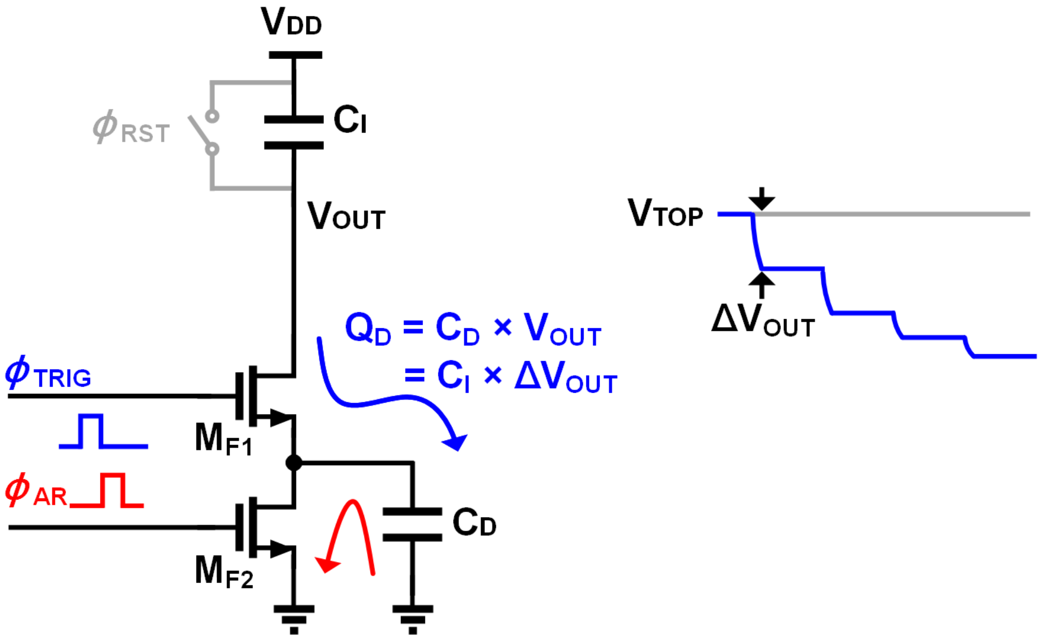
Digital counter



Analog counter

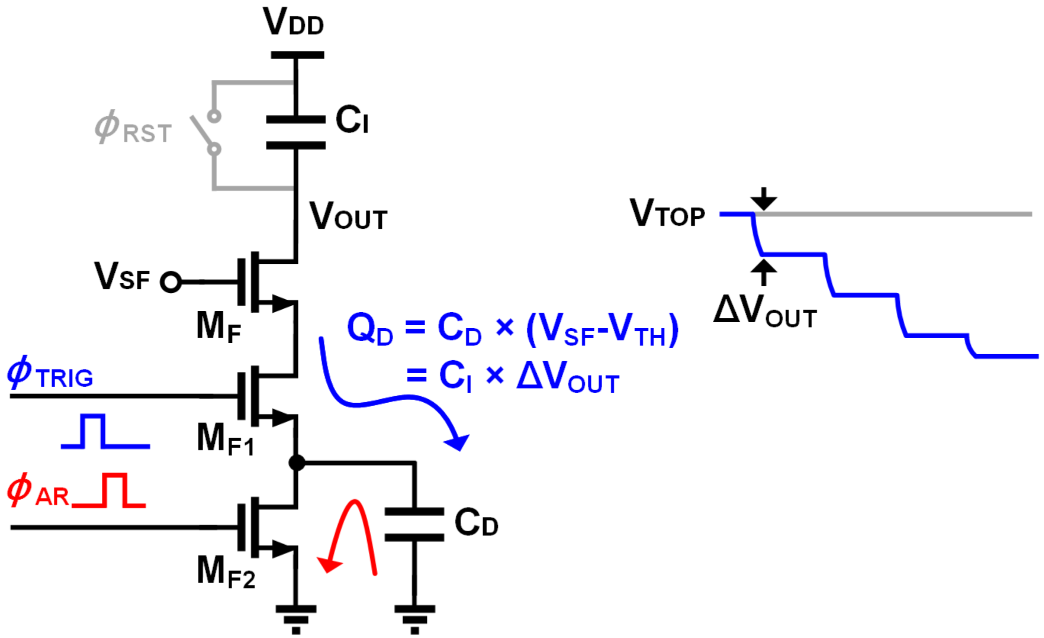
- Digital / analog pulse counter
  - Digital : high speed, linearity, no additional readout circuit
    large pixel pitch, 3-D stack process ☹
  - Analog : area-efficient, pixel-level implementation ✓
    medium operation speed, limited linearity ☹

Charge-sharing based counter



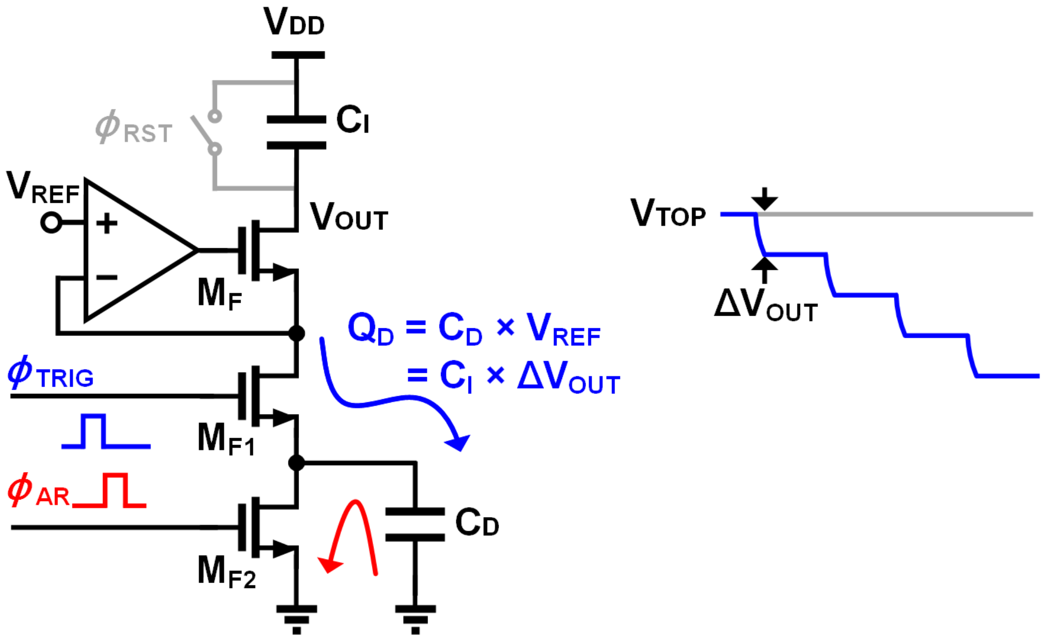
- Charge sharing between integration (C_I) & degeneration capacitor (C_D)
- 2 NMOS transistors used as switches (Φ_{TRIG} and Φ_{AR})
  - Counting step, $\Delta V_{OUT} \propto V_{OUT}$ > limited linearity & no tunability
- Additional technique for improving linearity

Charge-injection based counter



- Source follower (M_F) is added, separating C_D from V_{OUT}
  - Constant charge-injection and offers tunability by changing V_{SF}
  - Suffers threshold variation, resulting in counting step variation

Proposed analog counter



- Amplifier regulates source voltage of M_F to V_{REF}
  - Constant charge-injection without suffering threshold variation
  - Offers step tunability by adjusting V_{REF}

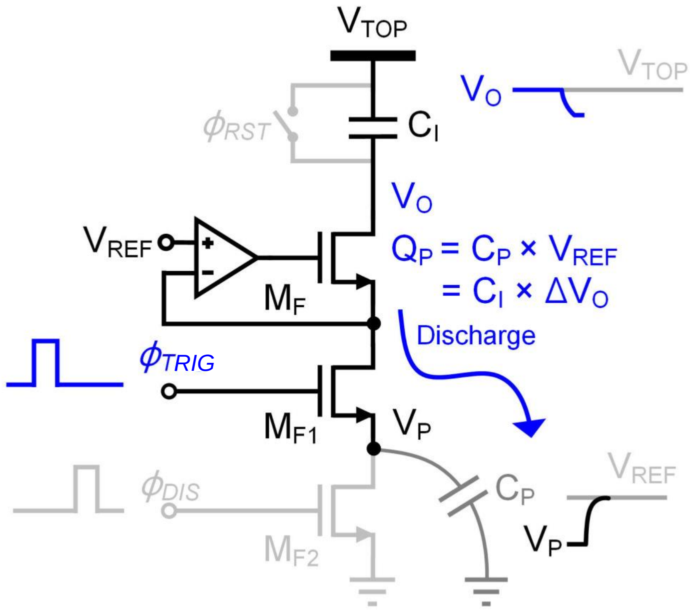
Pulse counter comparison

Structure	Digital	Charge-sharing	Charge-injection	Proposed
Occupied area [μm²]	1200	40†	44†	60†
Simulated linearity	-	6 bit	8 bit	9 bit
Tunability	x	x	○	○

†Estimated value with $C_I = 250$ fF

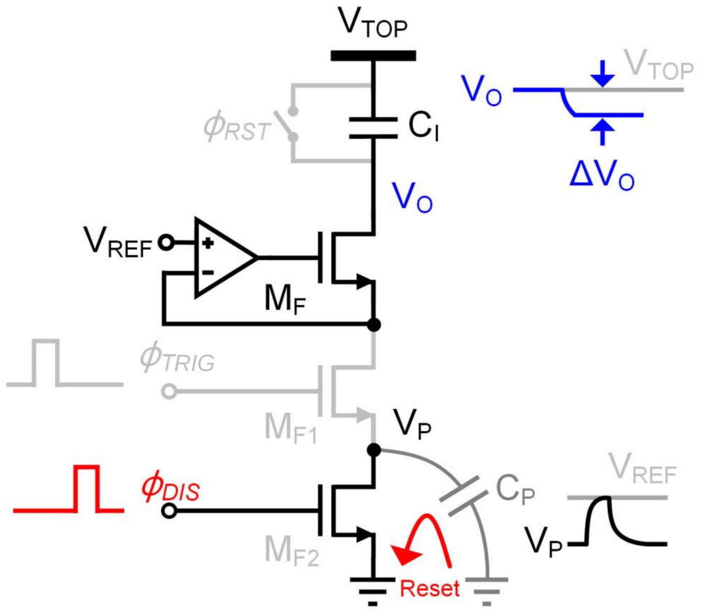
- Digital counter occupies largest area
- Analog counter shows limited linearity (< 8-bit)
    - Charge-injection based counter may suffer threshold variation
- Proposed counter achieves high linearity (> 9-bit), tunability ☺

Proposed counter: Discharge phase



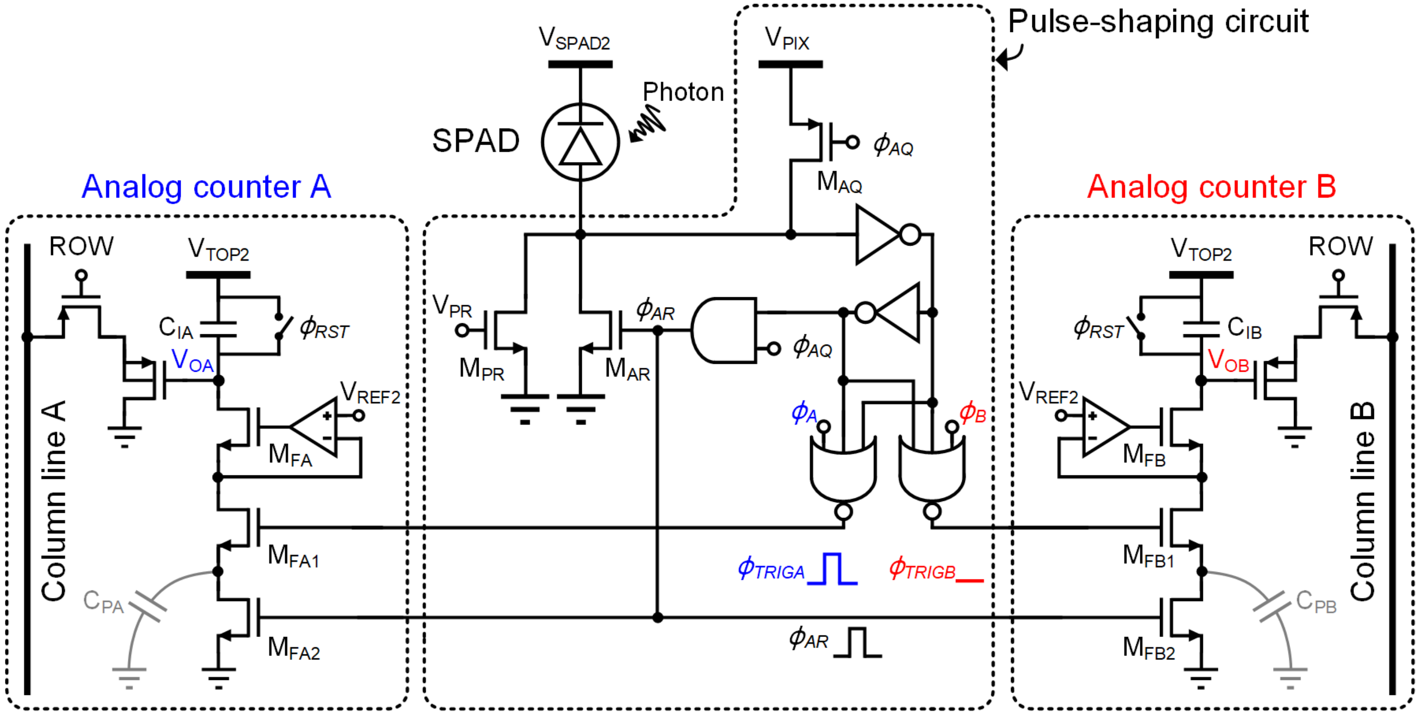
- Amplifier: 5 transistor with 600 nA bias, 30 dB DC gain
- M_{F1}, M_{F2}: NMOS switches , C_P: parasitic capacitor at V_P
  - C_P: charged from ground to V_{REF}, C_I: discharged by Q_P (Φ_{TRIG})
  - Counting step $\Delta V_O = C_P / C_I * V_{REF}$

Proposed counter: Reset phase



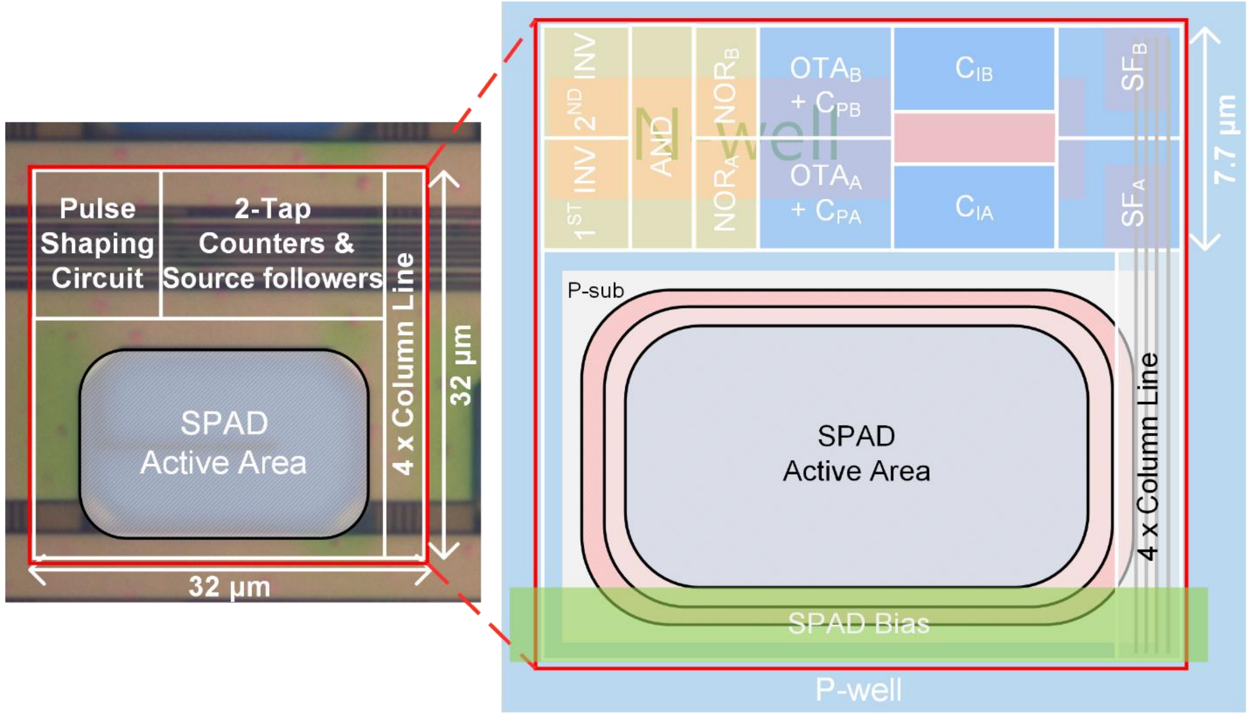
- C_P is reset to ground (Φ_{DIS}), remaining still until next trigger
  - Discharge and reset phases: should be separated
  - Requires delay between control signals (Φ_{TRIG} and Φ_{DIS})

Schematic of the proposed pixel



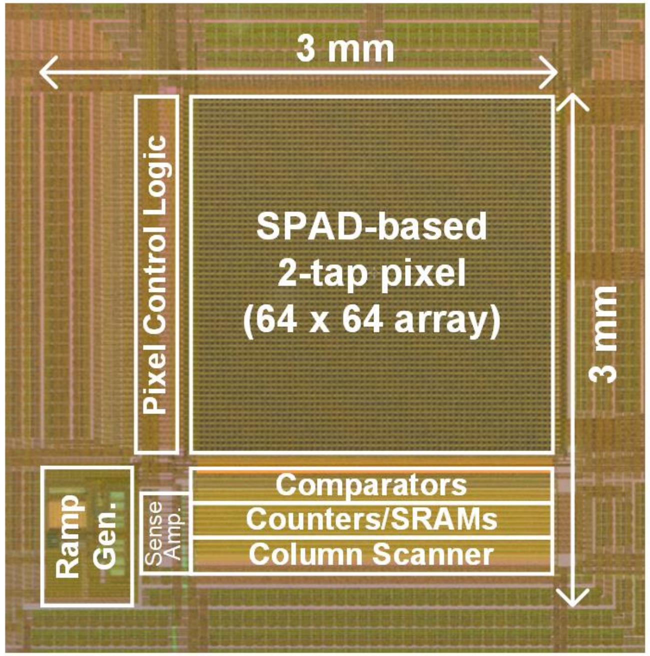
- AND gate: adding delay between Φ_{AQ} and Φ_{AR} ✓
  - Disabling SPAD: Φ_{AQ} to low ($V_{PIX} > V_{EX}$)
  - M_{AR}: turned off to avoid short circuit current ✓
- PMOS source follower & row switch: pixel readout

Layout of the proposed pixel



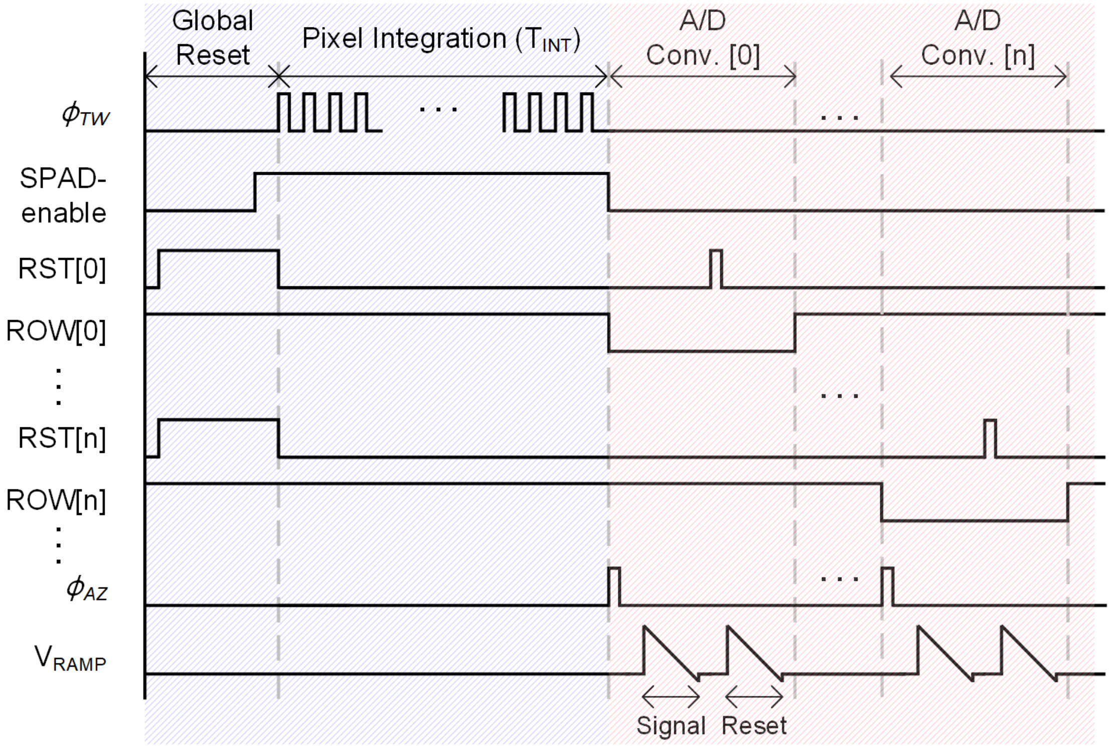
- Pixel pitch: 32 µm, considering fill factor > 25 % ☺
- Pulse shaping: 8.5 µm, counter: 20.5 µm length
  - Layout optimization: C_{IA} and C_{IB}
  - Source follower: below column readout line

Chip micrograph



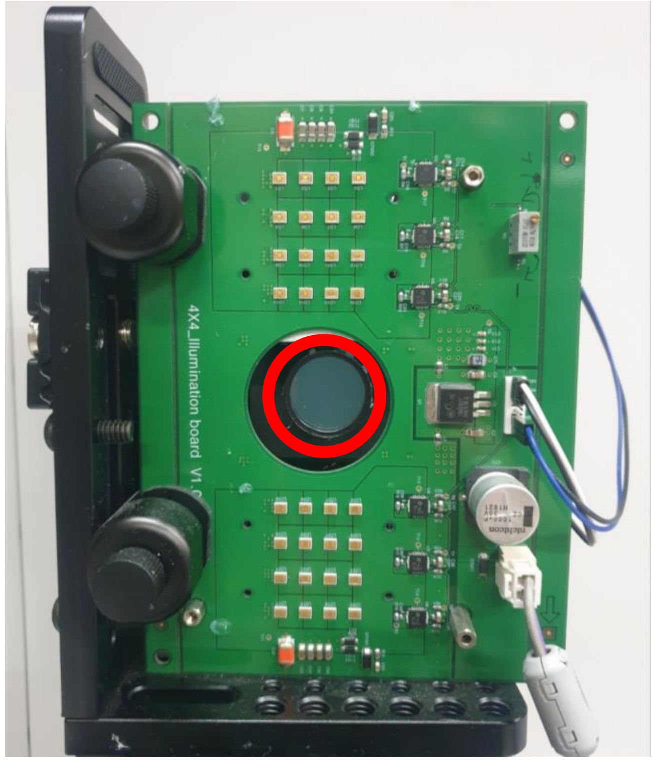
- 110 nm FSI process, core area: 3 x 3 mm^2
  - 64 x 64 SPAD pixel array
  - 256 single-slope ADC (4 ADCs / column)

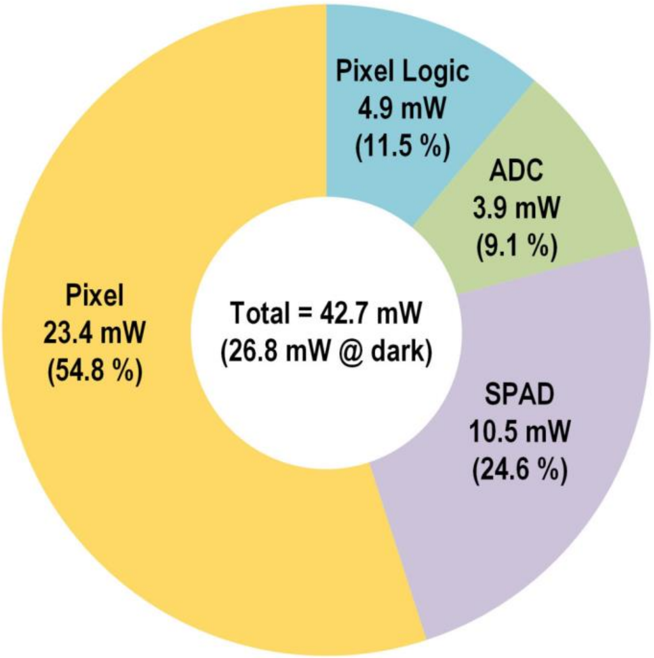
Overall timing diagram



- Global reset, pixel integration: 125 μs, pixel readout: 1.8 ms
- Frame rate of the proposed sensor: 520 fps (2-D)
  - 3-D frame: consists of four 2-D frames
  - Two 3-D frames (high, low f_{demod}) > 65 fps (depth image)

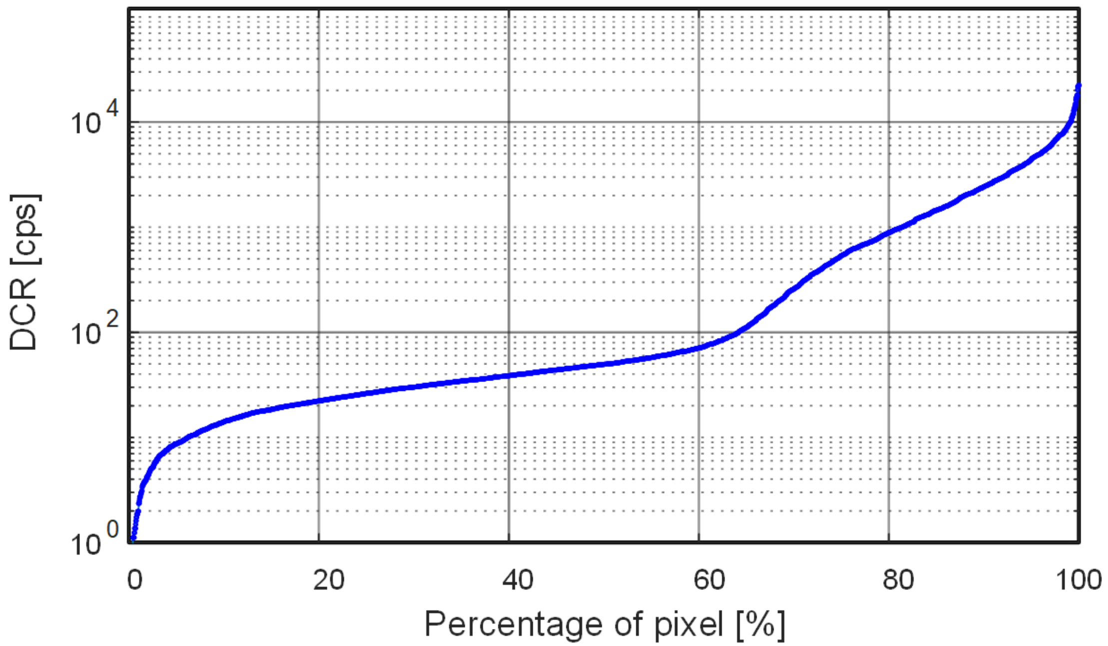
Measurement setup

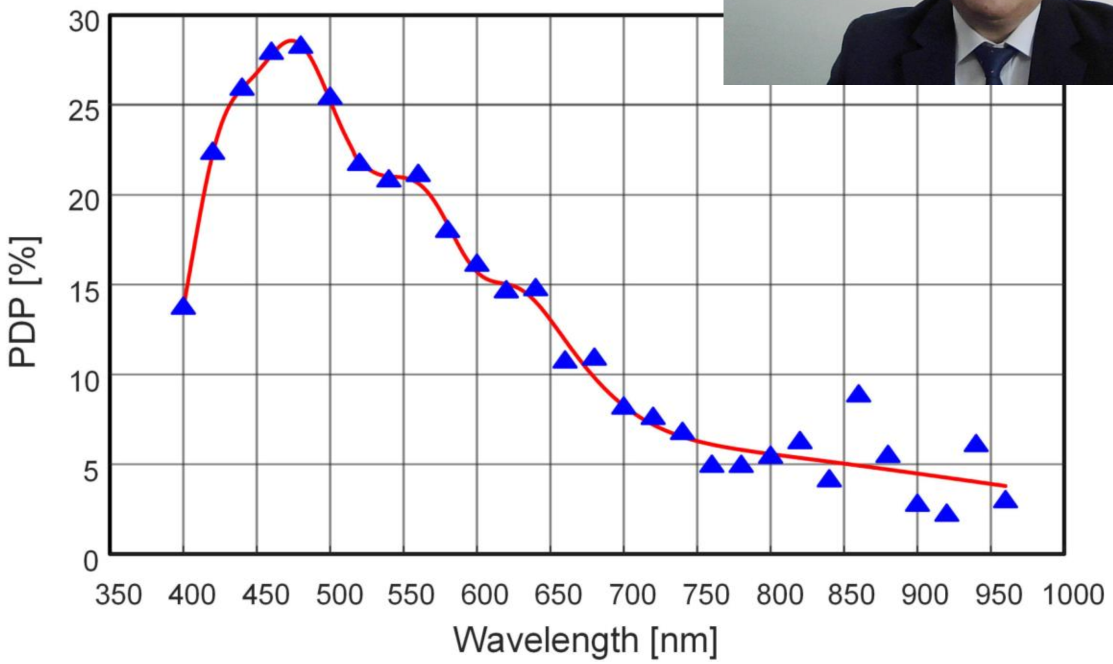




- VCSEL (850 nm) emission power: 1.16 mW/cm^2 (@ 1 m)
  - VCSEL emission angle: 20 °, FoV of optical lens: 17 °
  - Optical filter > CWL: 850 nm, FWHM: 10 nm, OD: 4.0
- Power consumption: 42.7 mW

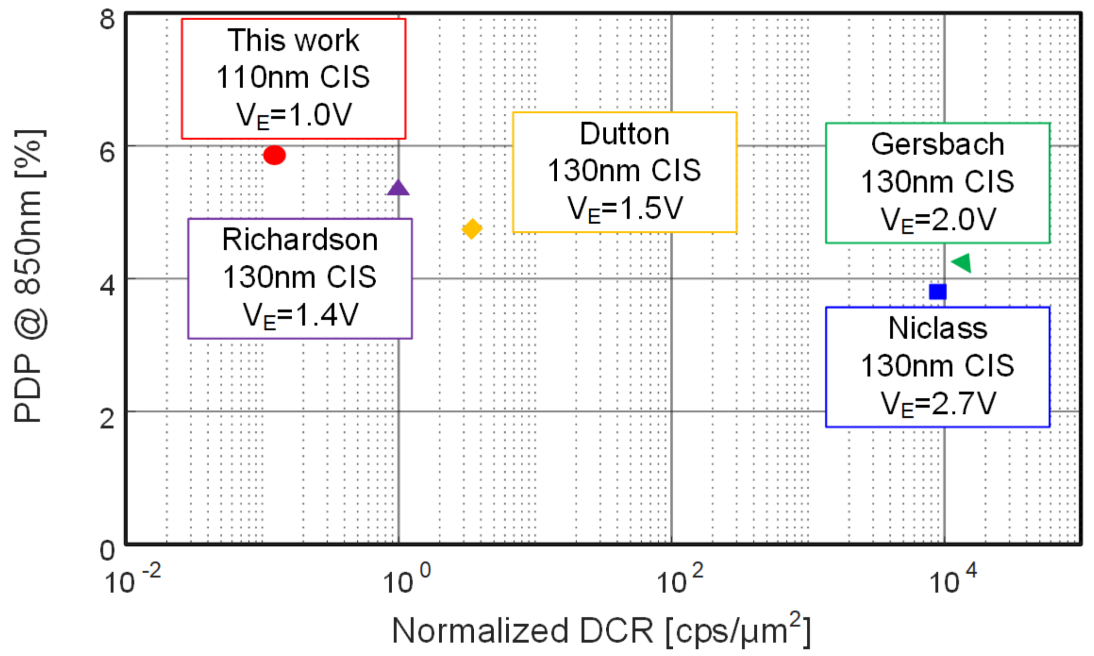
DCR / PDP of the proposed SPAD





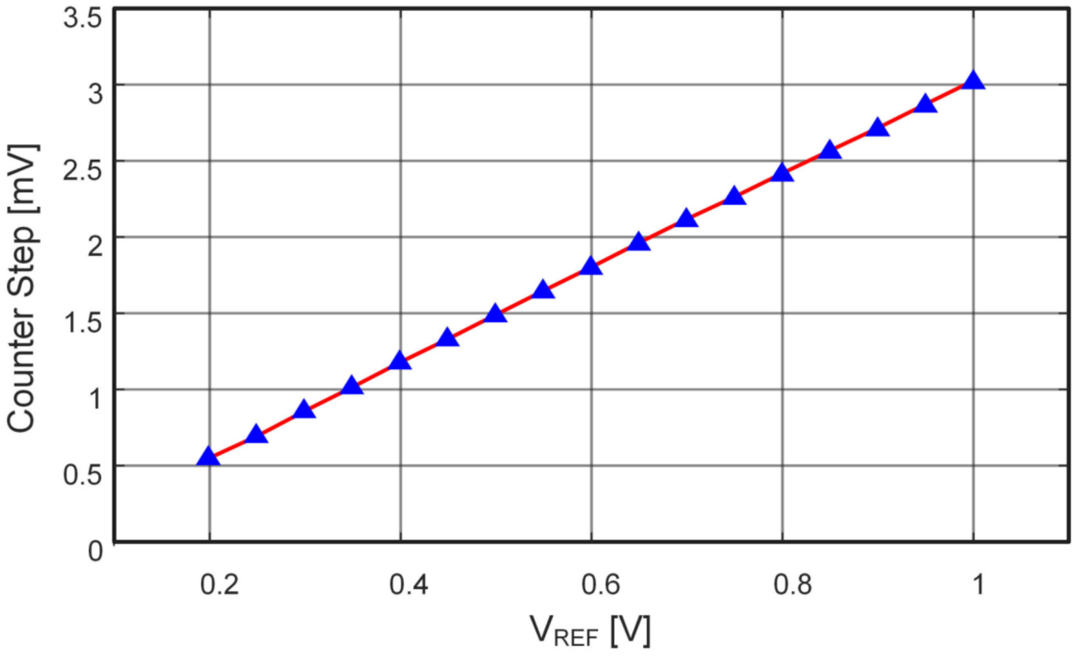
- 64 x 64 SPAD array dark count rate (DCR)
  - 33 (median) / 1800 cps (mean)
- Photon detection probability (PDP)
  - Peak: 28.2 % (@ 480 nm), 5.85 % (@ 850 nm)

Comparison with other SPADs



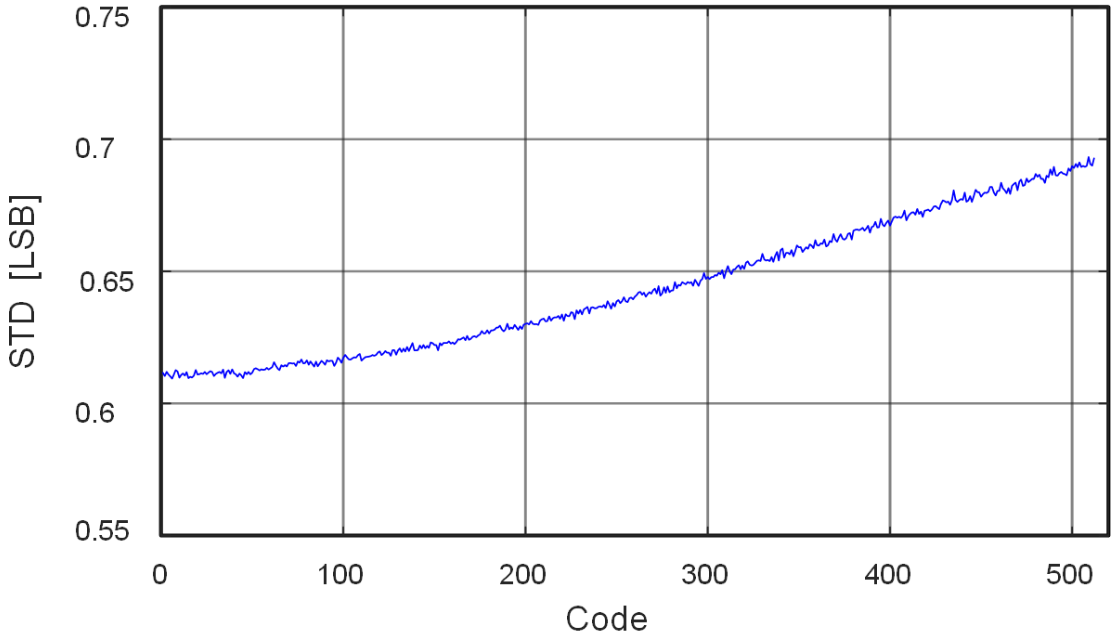
- Proposed SPAD and SPADs in similar technology nodes
  - Achieves lowest normalized DCR and comparable PDP
  - Low excess bias voltage, deep junction (PW/DNW)

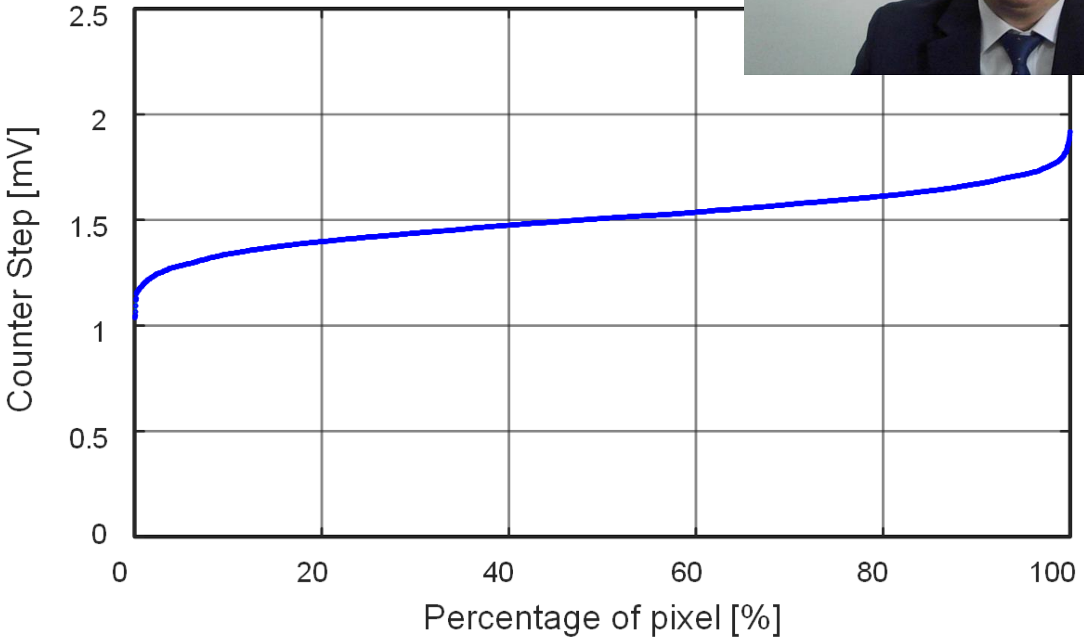
Step tunability of analog counter



- Measured counting step versus V_{REF}
  - V_{REF} tuned from 0.2 to 1 V, counting step > 0.6 to 3 mV
  - V_{REF} = 0.5 V, C_P = 0.75 fF, C_I = 250 fF > 9-bit counter

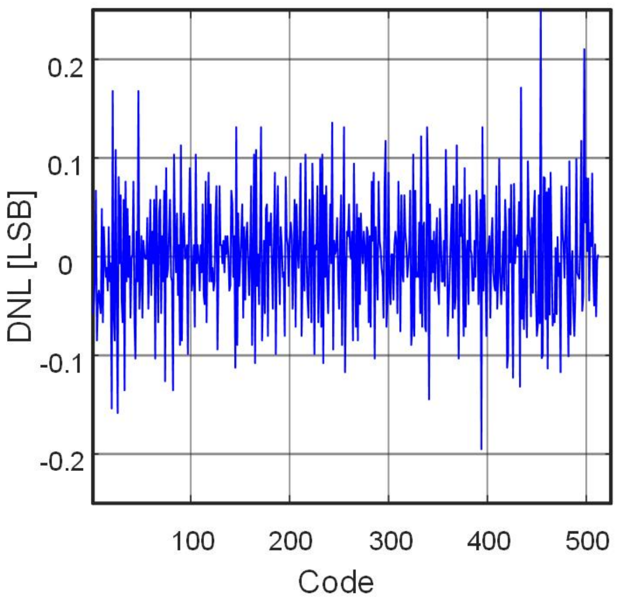
Noise / step variation of analog count

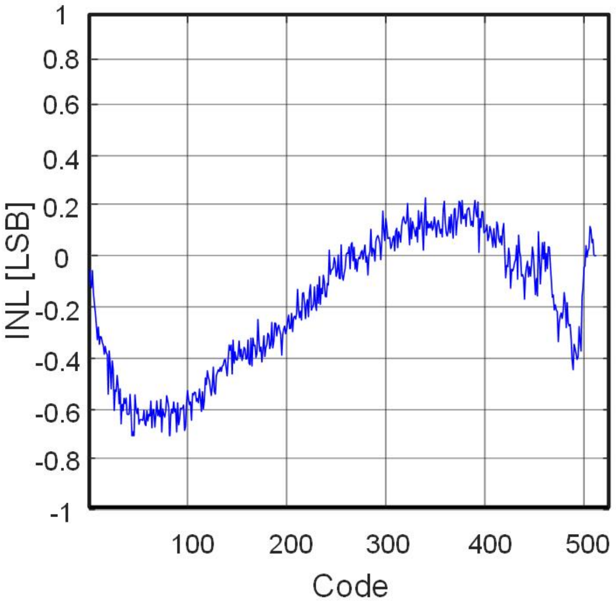


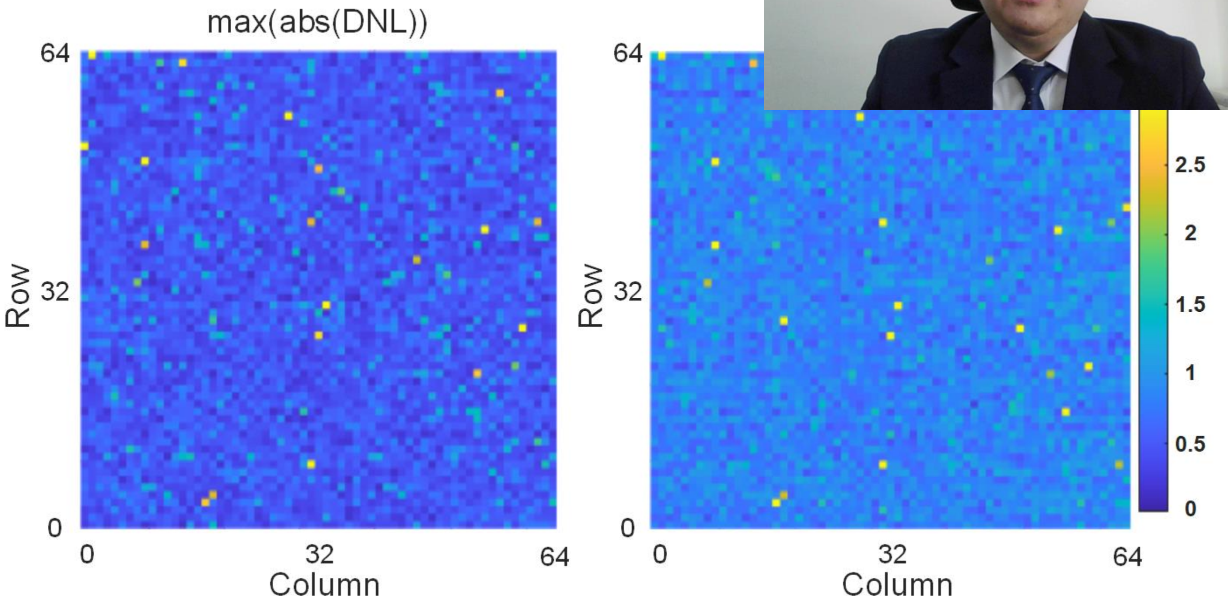


- Measured noise and step variation of proposed counter
  - Φ_{AQ}: test signal, externally controls the counting number
  - Measured noise (1-σ): > 0.7 LSB for entire codes
  - Step variation: 8.3 %, offset mismatch and C_P variation

DNL / INL of analog counter array

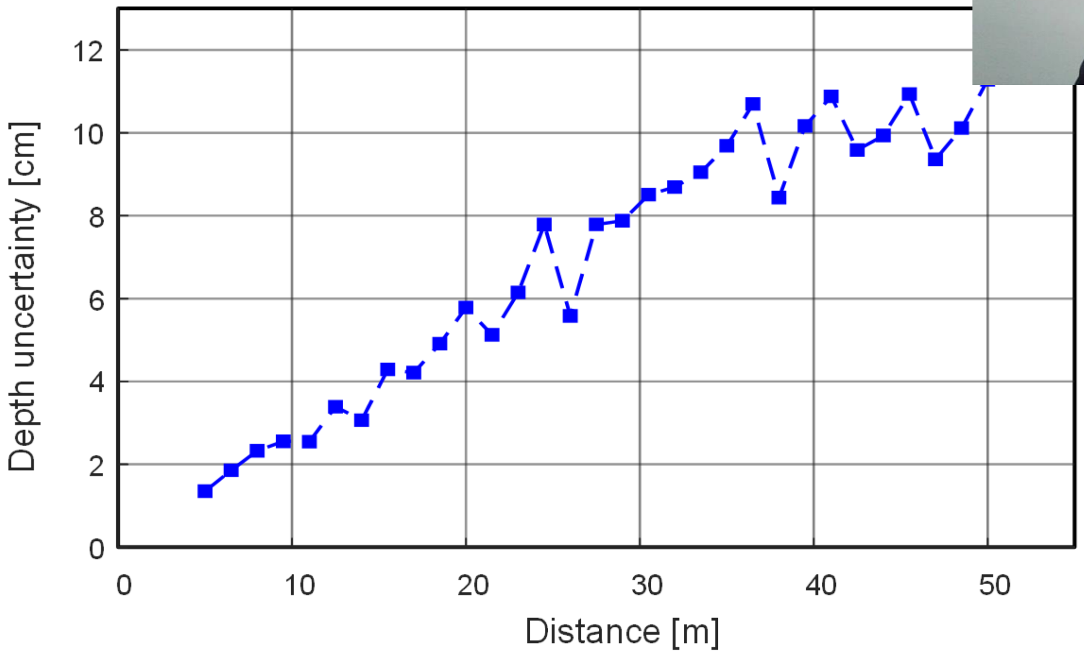






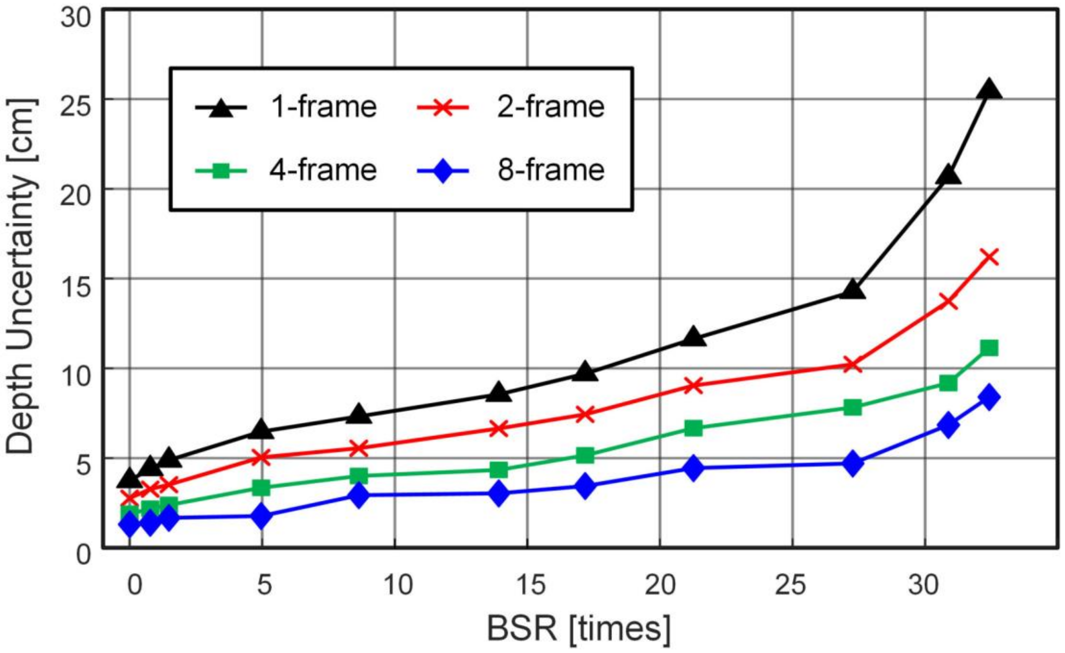
- Measured DNL / INL of analog pulse counter array
  - DNL: +0.25 / -0.19 LSB, INL: +0.22 / -0.72 LSB
  - Outliers: less than 3 % of pixel population
  - Proposed pulse counter: operates as 9-bit counter ☺

Depth uncertainty result



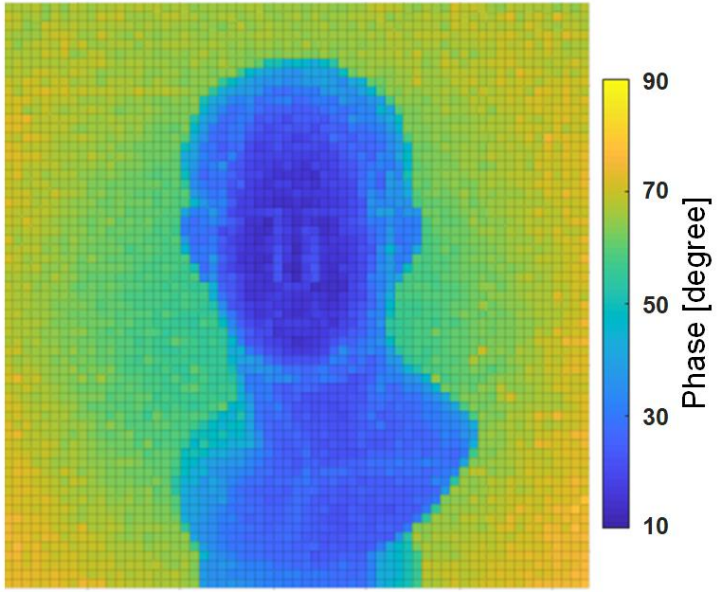
- Measured depth uncertainty (1-σ) result in range of 5 to 50 m (65 fps)
  - Depth uncertainty: STD of distance over 400 measurements
  - 1.35 to 11.3 cm in range of 5 to 50 m
  - Relative depth uncertainty: 0.22 % (at 50 m)

Depth uncertainty result with BGL



- Measured depth uncertainty varying background-to-signal ratio (BSR)
  - Variable IR source: applied as background (target @ 1.5 m)
  - Depth uncertainty increases until counter saturation
  - Accumulating multiple frames improves depth uncertainty

3-D measurement results

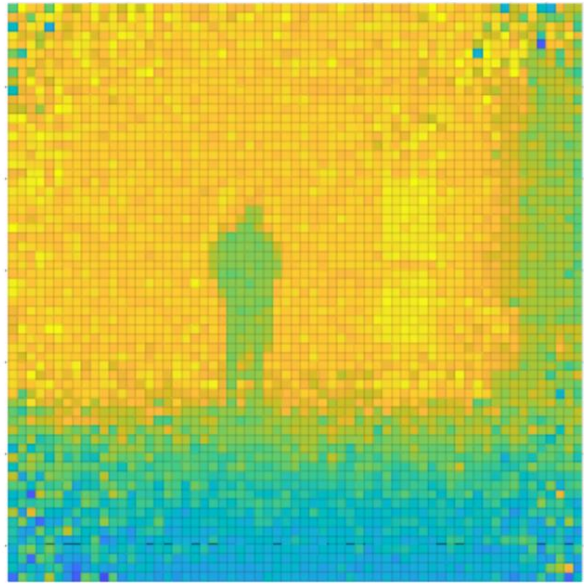


f_{demod} = 50 MHz

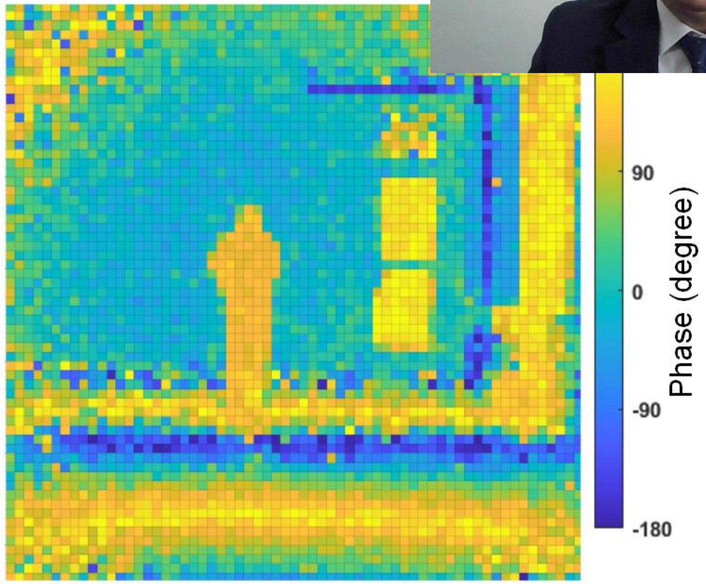
- Sample 3-D images of Agrippa statue
  - Demodulated with maximum designed frequency (50 MHz)
  - Result shows detail with high demodulation frequency

3-D measurement results

BGL = 120 klx



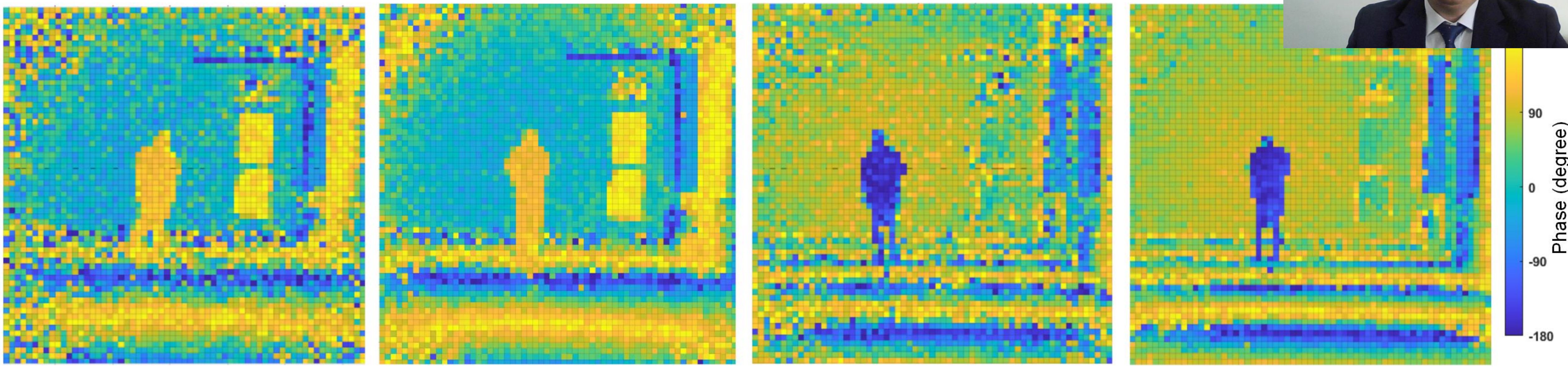
f_{demod} = 3.125 MHz



f_{demod} = 25 MHz

- Sample 3-D images with 120 klx sunlight
  - Vertical wall: 20 m, 8-frame accumulation (16.25 fps)
  - Optical bandpass filter: reduce sunlight by 95 %

3-D measurement results



f_{demod} = 25 MHz, 65 fps | f_{demod} = 25 MHz, 16.25 fps | f_{demod} = 50 MHz, 65 fps | f_{demod} = 50 MHz, 16.25 fps

- Depth uncertainty improvement by frame accumulation
  - Increasing frames by 4 times > more details & lower noise
  - Optical bandpass filter & frame accumulation

  > 3-D image is reconstructed successfully!

Performance comparison

	This Work	B. Park SSC-L20 [1]	C. S. Bamji ISSCC18 [2]	T. Okino ISSCC20 [3]	E. Manuzzato ISSCC22 [4]	M. Perenzoni SSC-L20 [5]	C. Niclass JSSC14 [6]	S. W JS	
Photodetector	**SPAD**	SPAD	PD	SPAD (Vertical)	SPAD	SPAD	SPAD	SPAD	SPAD
ToF technique	**iToF**	iToF	iToF	iToF + dToF	dToF	dToF	dToF	dToF	dToF
Key feature	**2-tap pulse counter**	1-tap pulse counter	2-tap photogate	1-tap pulse counter	Per-pixel TDC	Per-column TDC	Per-column TDC	16-Shared TDC	128-Shared TDC
Technology [nm]	**110**	110	65 (BSI)	65	110	150	180	40 / 90	45 / 65
Pixel resolution	**64 × 64**	64 × 64	1024 × 1024	1200 × 900	64 × 64	50 × 40 (2-SPAD)	202 × 96	256 × 256 (4 × 4 SPAD)	256 × 256 (16 × 8 SPAD)
Pixel pitch [μm]	**32**	32	3.5	6	48	38.5 × 33.5	N/A	9.2 (36.8 × 36.8)	19.8 (316.8 × 158.4)
Fill factor [%]	**26.3**	17.3	100 (with μ-lens)	N/A	12.9	4.8-15.3	70	51	31.3
Background [klx]	**120**†	90†	25	N/A	30	18	100†	1	3
Emitter wavelength [nm]	**850**	850	860	N/A	905	650	870	671	532
Frame rate [fps]	**65**	90	30	30	25	1 kHz @ 1000 pts	10	30	2000 pixel/s
Maximum distance [m]	**50**	40	4.2	13(iToF) / 250(dToF)	8.2	3	100	50	150
Depth uncertainty [%]	**0.22**	0.51	0.2	0.38 / N/A	3.29	0.05	0.14	N/A	0.1
Chip power [mW]	**42.7**	33.5	650	2500	205.74	28.3	530	77.6	N/A

† Measured at the Target

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Photodetector	**SPAD**	SPAD	PD	SPAD (Vertical)	SPAD	SPAD	SPAD	[illegible]	[illegible]
ToF technique	**iToF**	iToF	iToF	iToF + dToF	dToF	dToF	dToF	dToF	dToF
Key feature	**2-tap pulse counter**	1-tap pulse counter	2-tap photogate	1-tap pulse counter	Per-pixel TDC	Per-column TDC	Per-column TDC	16-Shared TDC	128-Shared TDC
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Depth uncertainty [%]	**0.22**	0.51	0.2	0.38 / N/A	3.29	0.05	0.14	N/A	0.1
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Photodetector	**SPAD**	SPAD	PD	SPAD (Vertical)	SPAD	SPAD	SPAD	SPAD	SPAD
ToF technique	**iToF**	iToF	iToF	iToF + dToF	dToF	dToF	dToF	dToF	dToF
Key feature	**2-tap pulse counter**	1-tap pulse counter	2-tap photogate	1-tap pulse counter	Per-pixel TDC	Per-column TDC	Per-column TDC	16-Shared TDC	128-Shared TDC
Technology [nm]	**110**	110	65 (BSI)	65	110	150	180	40 / 90	45 / 65
Pixel resolution	**64 × 64**	64 × 64	1024 × 1024	1200 × 900	64 × 64	50 × 40 (2-SPAD)	202 × 96	256 × 256 (4 × 4 SPAD)	256 × 256 (16 × 8 SPAD)
Pixel pitch [μm]	**32**	32	3.5	6	48	38.5 × 33.5	N/A	9.2 (36.8 × 36.8)	19.8 (316.8 × 158.4)
Fill factor [%]	**26.3**	17.3	100 (with μ-lens)	N/A	12.9	4.8-15.3	70	51	31.3
Background [klx]	**120†**	90†	25	N/A	30	18	100†	1	3
Emitter wavelength [nm]	**850**	850	860	N/A	905	650	870	671	532
Frame rate [fps]	**65**	90	30	30	25	1 kHz @ 1000 pts	10	30	2000 pixel/s
Maximum distance [m]	**50**	40	4.2	13(iToF) / 250(dToF)	8.2	3	100	50	150
Depth uncertainty [%]	**0.22**	0.51	0.2	0.38 / N/A	3.29	0.05	0.14	N/A	0.1
Chip power [mW]	**42.7**	33.5	650	2500	205.74	28.3	530	77.6	N/A

† Measured at the Target

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Conclusion

- 64 x 64 SPAD-based iToF sensor with 2-tap analog pulse

- Time-gated photon counting method
  - Compact pixel pitch (32 μm), high fill factor (26.3 %)
  - Large detection range (50 m), low depth uncertainty (0.22 %)
  - High frame rate (65 fps), high sunlight tolerance (120 klx)

  > Suitable for outdoor applications

- This work shows high potential of **SPAD-based iToF sensors**

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Thank you for your attention !