Sensing is life

A Back Side Illuminated 3D-Stacked SPAD in 45nm Technology

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Outline of Presentation

1. From a CMOS integrated FSI towards a BSI 3d-stacked SPAD
2. Test Structure
3. Impact of technology options on PDE and cross talk
4. Results for 10um pitch SPAD (BV, PDE, DCR, Jitter, cross-talk, after pulsing probability)

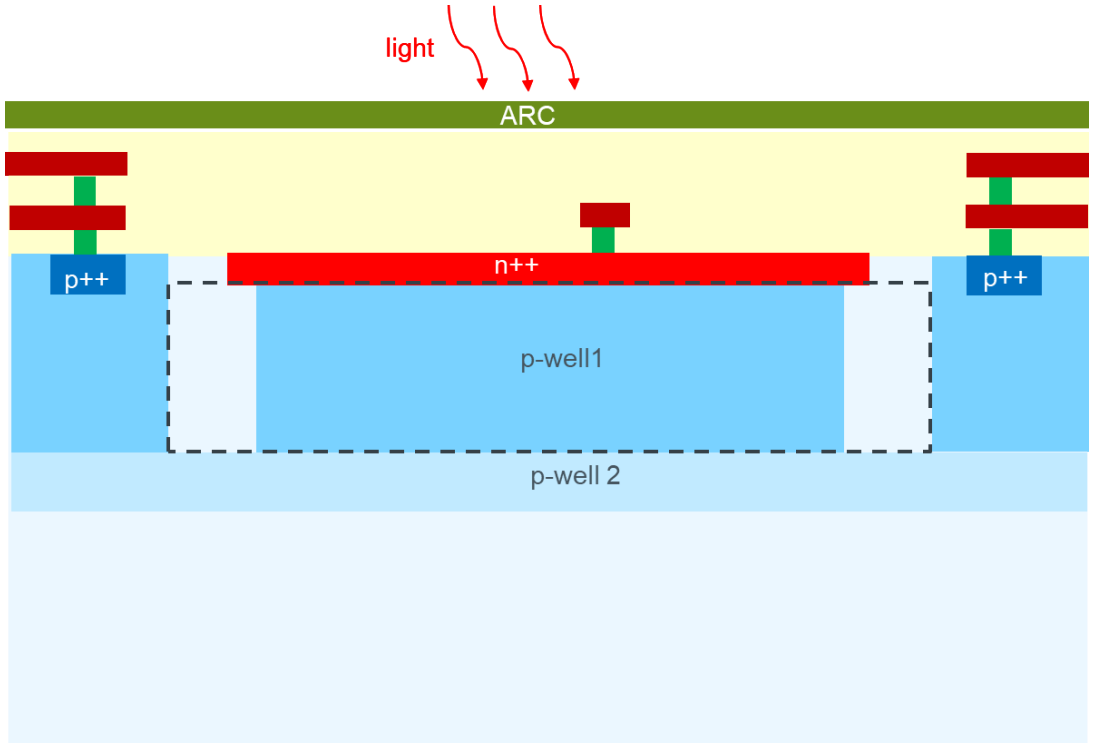
From a CMOS integrated FSI towards a BSI 3d-stacked SPAD (1)

For a front side illuminated SPAD in a CMOS process, PDE is limited by:

- Transmission losses through BEOL (back end of line) dielectric stack.
- Part of active area shielded by metal and contacts
- Poor fill factor when taking the CMOS area (e.g. quencher, inverter, TDCs (time to digital converters) into account.
- Small volume from which the carriers can enter the avalanche multiplication region
- Limited process optimization potential because of side effects on CMOS

Potential improvements for FSI SPAD:

- Anti reflective coating (ARC)
- Maximize volume from which carriers can enter the avalanche multiplication region.
- Micro lens array (increases effective fill factor)



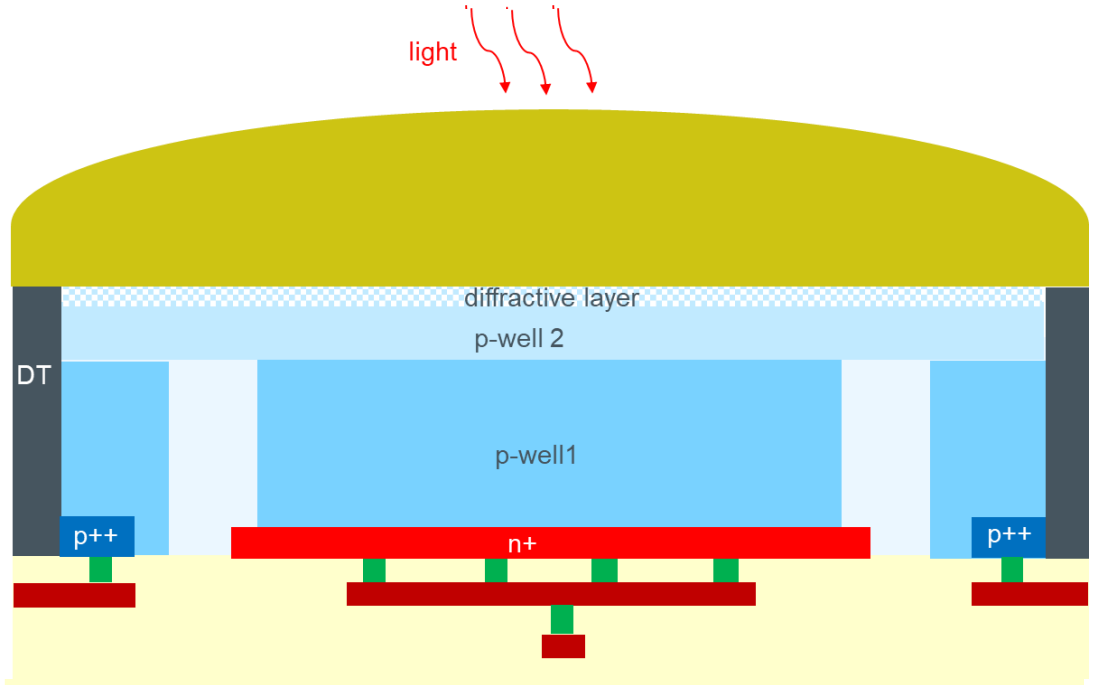
From a CMOS integrated FSI towards a BSI 3d-stacked SPAD (2)

BSI SPAD

- Light losses of BEOL stack avoided.
- No shadowing of active region due to contacts

Further improvement

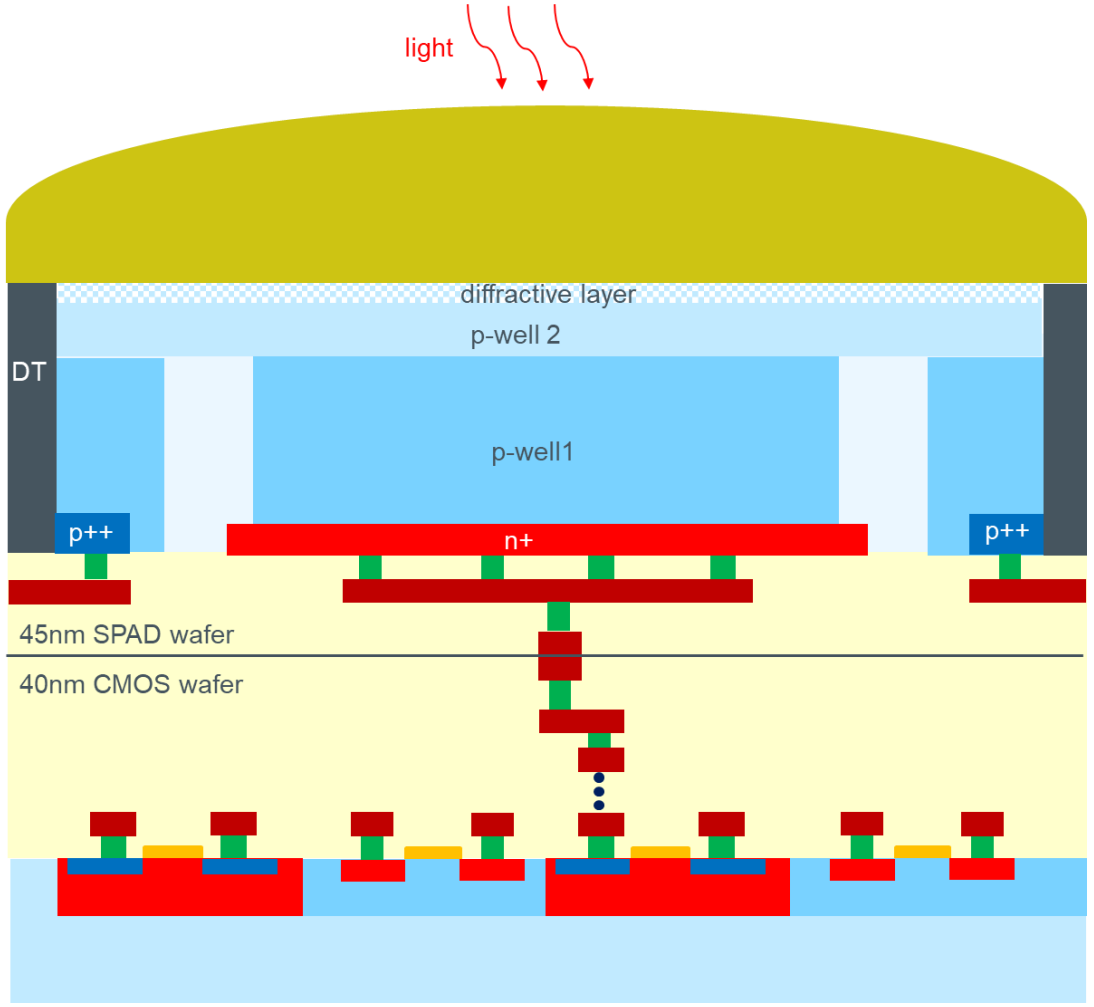
- Surface diffractive layer (DL) or ARC
- Deep trench isolation
- Micro lens



From a CMOS integrated FSI towards a BSI 3d-stacked SPAD (3)

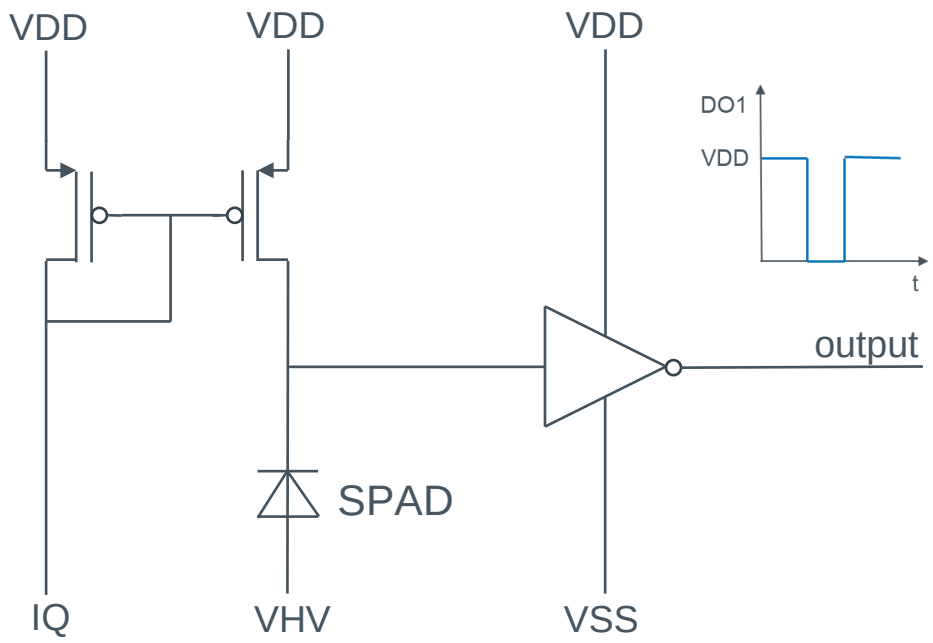
3d stacked BSI SPAD:

- Fill factor limited by SPAD design only – CMOS circuitry is underneath the SPAD array.
- SPAD can be optimized completely independent of CMOS processing.
- SPAD wafer can be combined with different CMOS nodes enabling products optimized in performance and cost.



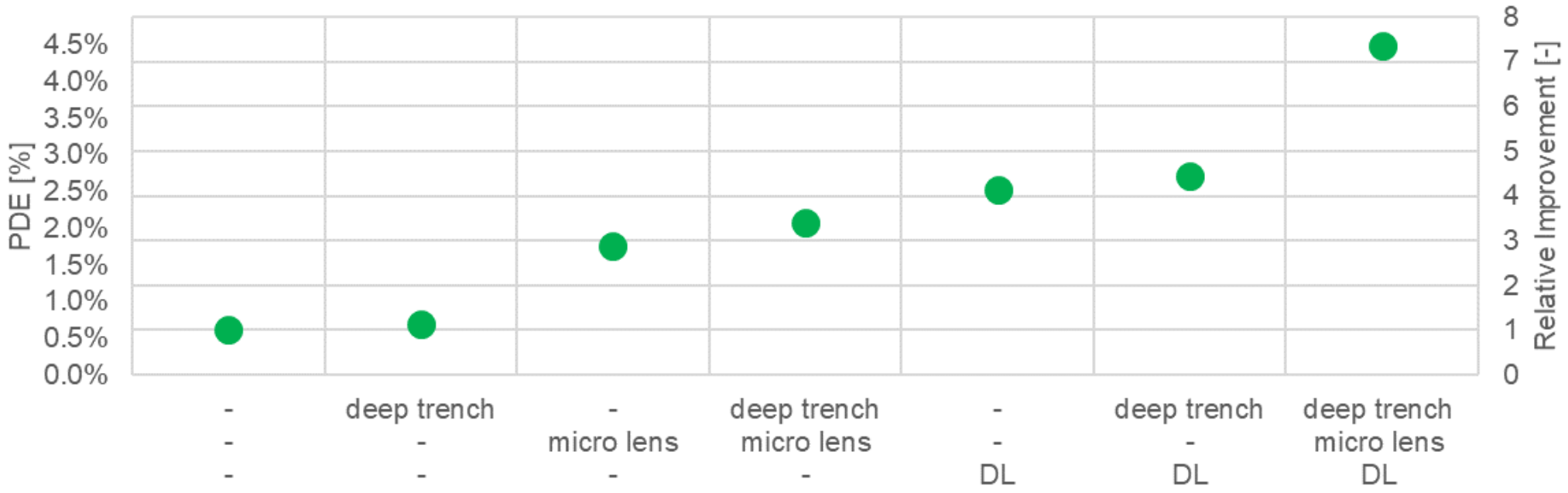
Test Structure and SPAD Schematic

- SPAD is biased between VDD and VHV (negative).
- Passive quenching used.
- Current IQ used to set the dead time over a wide range (~10ns….~10µs).
- For crosstalk characterization, outputs for two neighboring SPADs are available.
- Measurement results apply for 2V excess bias voltage and 940nm (if not stated otherwise).



Improvements of PDE with deep trench, micro lens and diffractive layer (DL)

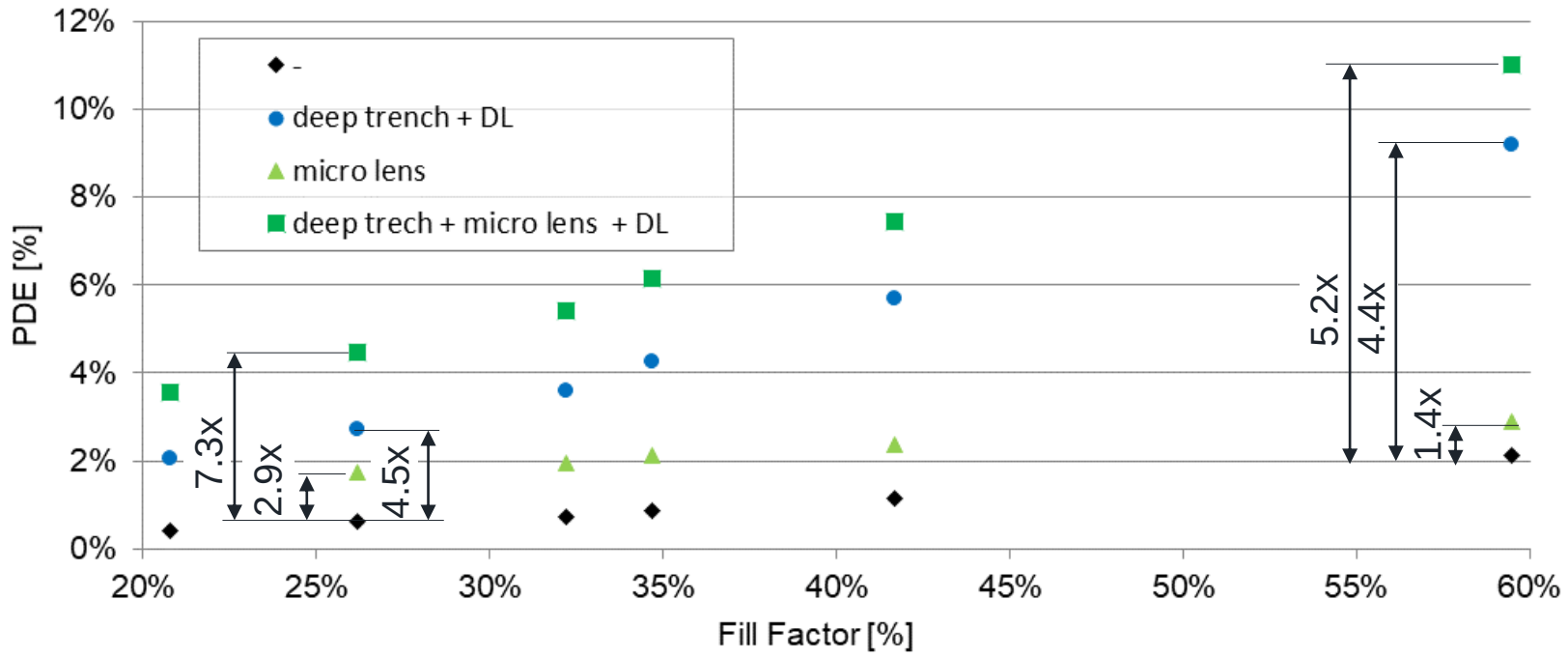
Low fill factor SPAD



→ Micro lens and diffractive layer are the most important technologies to enhance PDE (~7x relative improvement)!

Improvements of PDE with deep trench, micro lens and diffractive layer (DL)

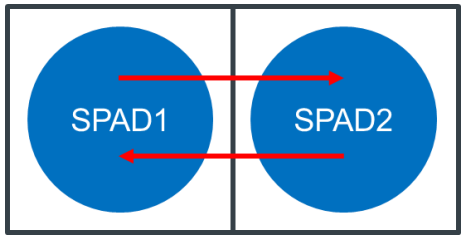
Low to high fill factor SPADs



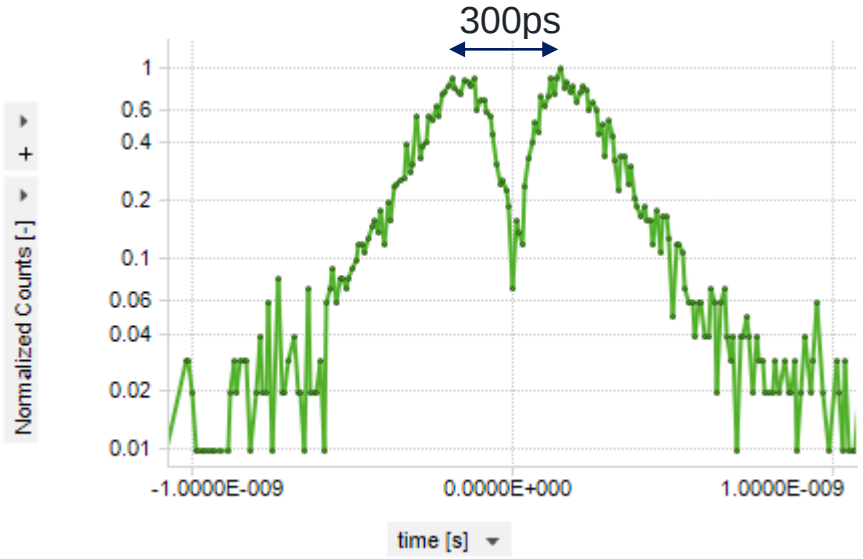
- The diffractive layer improves PDE by ~4.5x independent of the fill factor.
- The improvement with a micro lens depends strongly on the fill factor (low fill factor SPADs improve much stronger with micro lens compared to high fill factor SPADs).

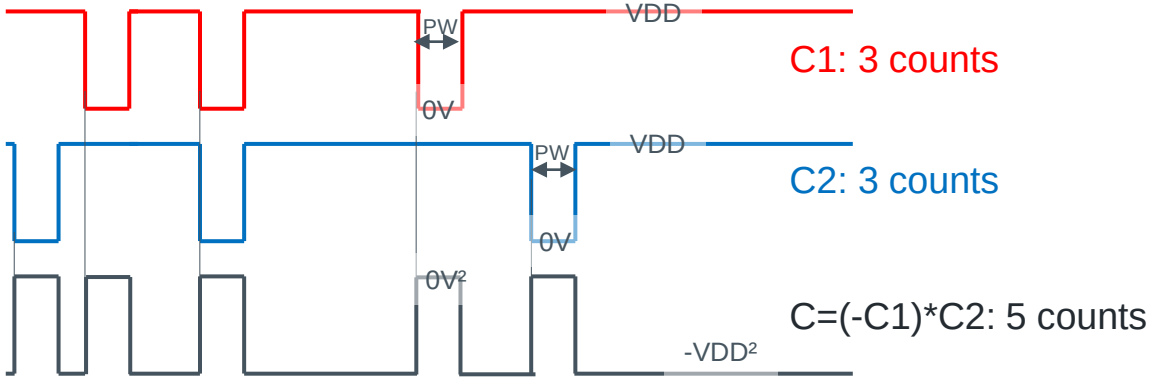
Cross Talk

Measurement Method



Light emission of SPAD1 (when triggered by DCR or light) can trigger the neighboring SPAD2 (or vice versa) → optical orthogonal cross-talk.



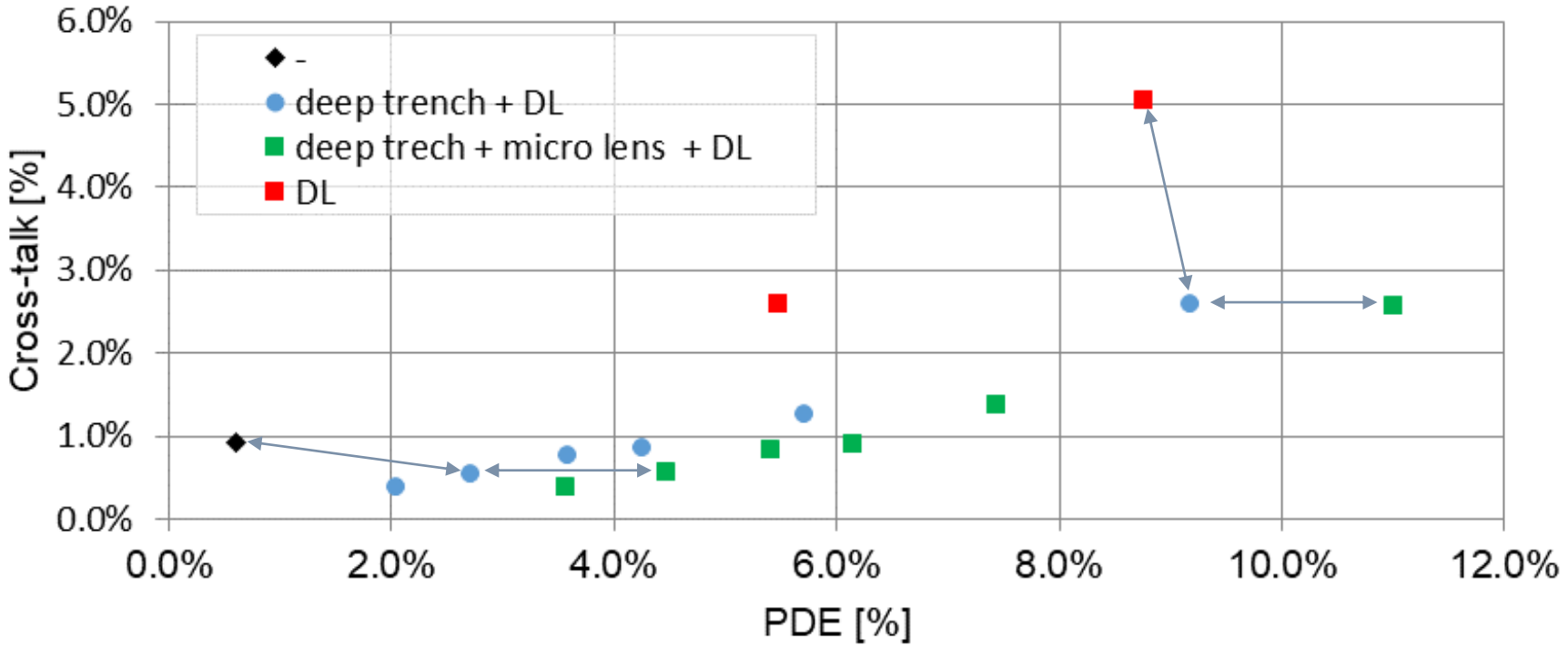


The cross talk between SPAD1 and SPAD2 is measured by counting the events for SPAD1, SPAD2 and both SPADs combined.

Cross talk is calculated as: (C1+C2-C)/C

Cross-Talk

Impact of deep trench, diffractive layer (DL) and micro lens



- Cross talk increases with PDE since a higher PDE increases the probability that SPAD triggering occurs by light emission of neighbor.
- Without deep trench, cross talk is about 2x higher
- Micro lens improves PDE without increasing cross talk

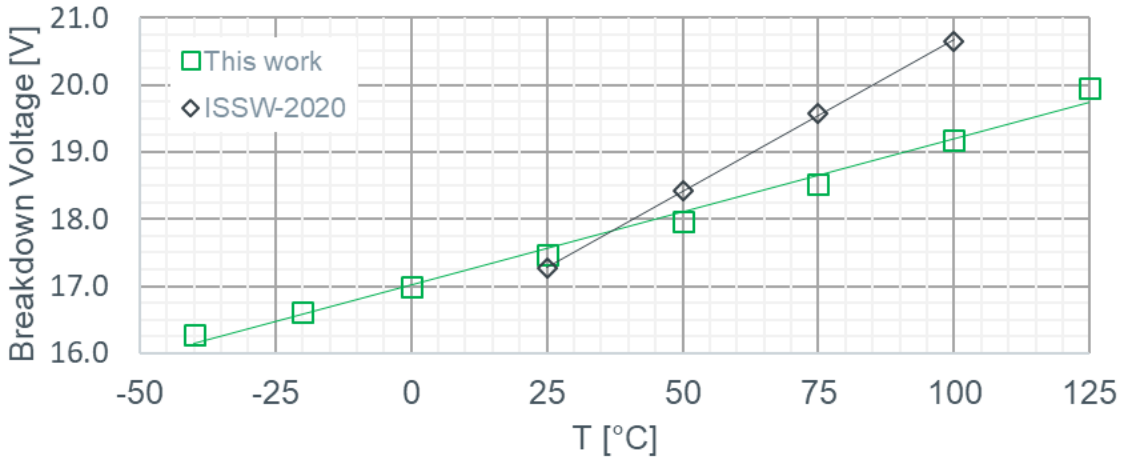
Key Results for Optimized SPAD

3d stacked 45/40nm, deep trench, diffractive layer

Breakdown Voltage

Breakdown voltage is key for many SPAD parameters:

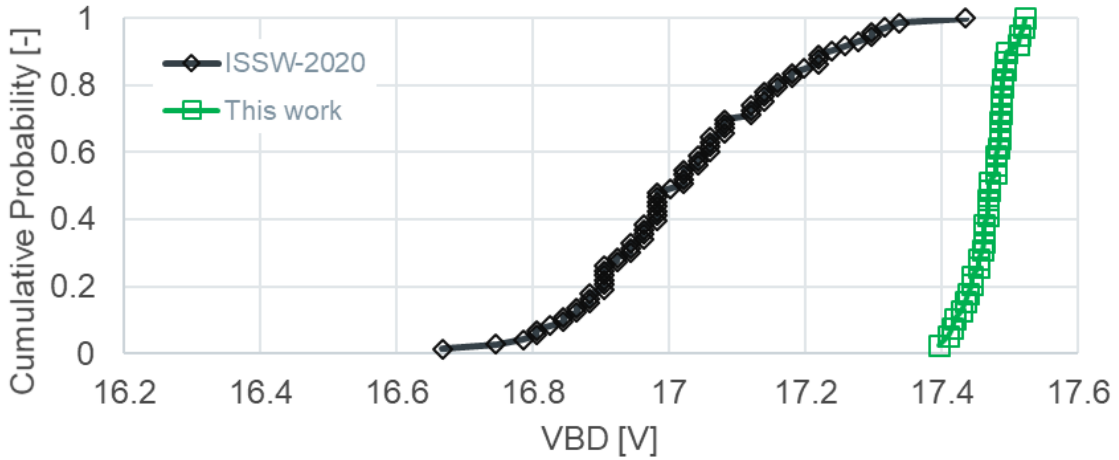
- Achievable fill factor determined by BV (size of overhead region).
- Depletion layer width (impacts PDE, capacitance, jitter)
- DCR (for low BV, tunneling dominates DCR)
- Energy per SPAD event scales with breakdown voltage.



Results:

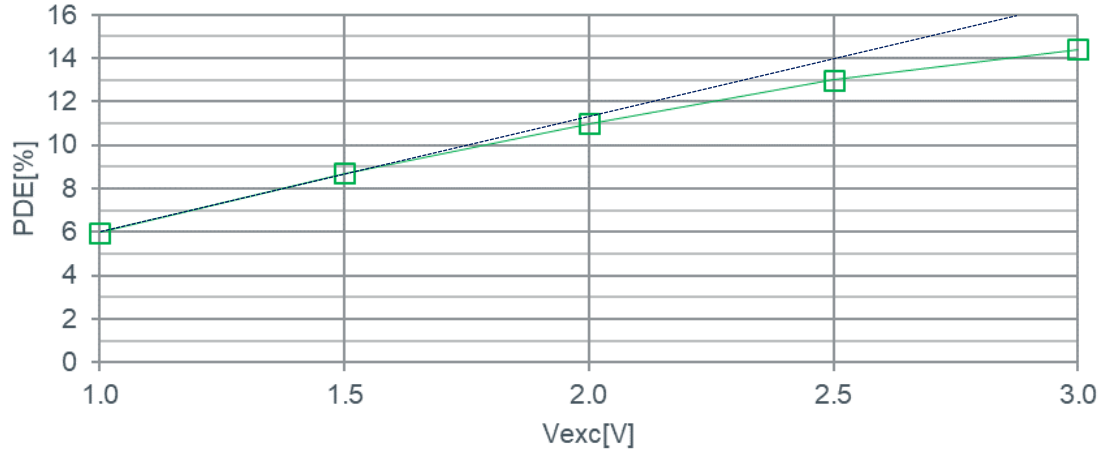
- Breakdown voltage at 25°C very similar to previous work but by junction optimization the temperature coefficient is reduced from 45mV/K to 20mV/K.

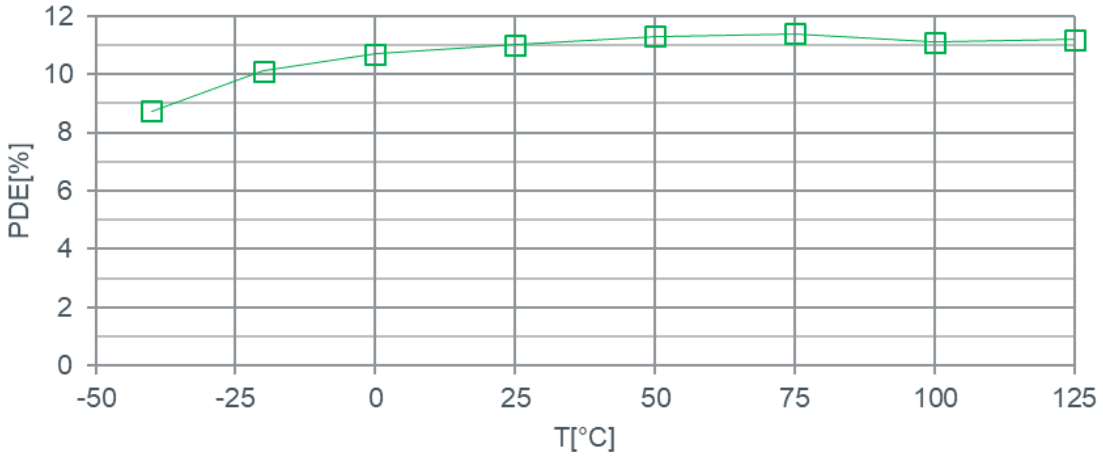
- Standard deviation within wafer distribution reduced from ~150mV to 30mV!



PDE

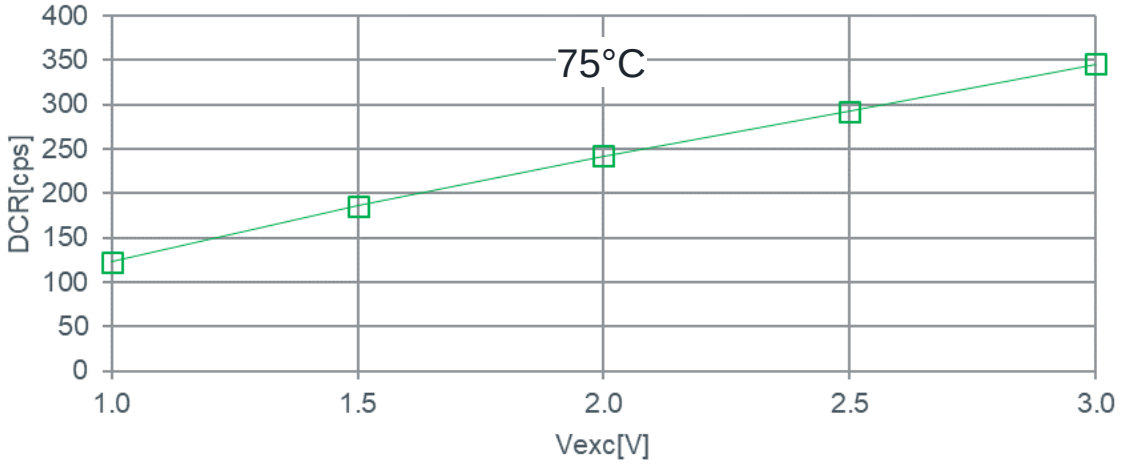
- PDE starts to saturate at ~2V excess bias voltage
- PDE quite constant from 0°C to 125°C

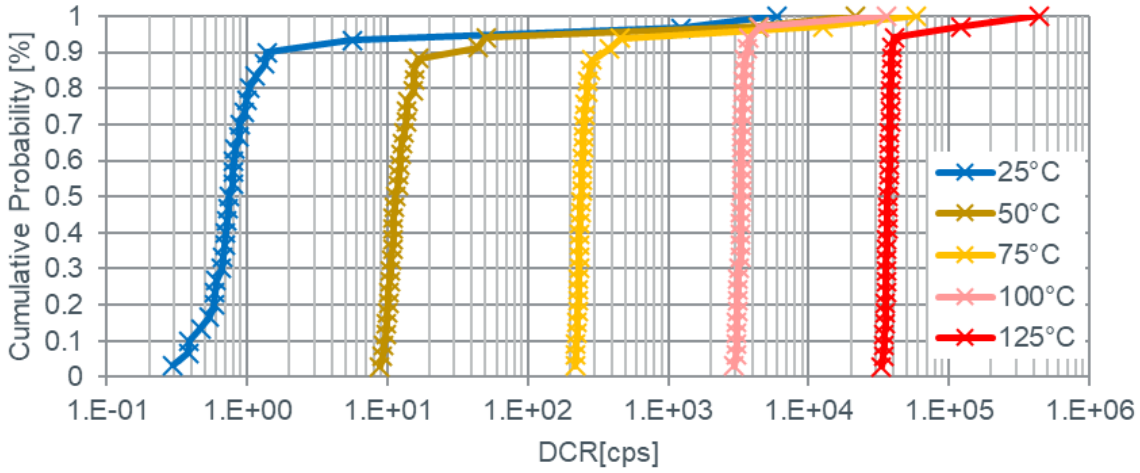




DCR

- DCR increases linearly with excess bias voltage
- Around 90% of SPADs with DCR close to median value
- Extracted activation energy: 1.20eV

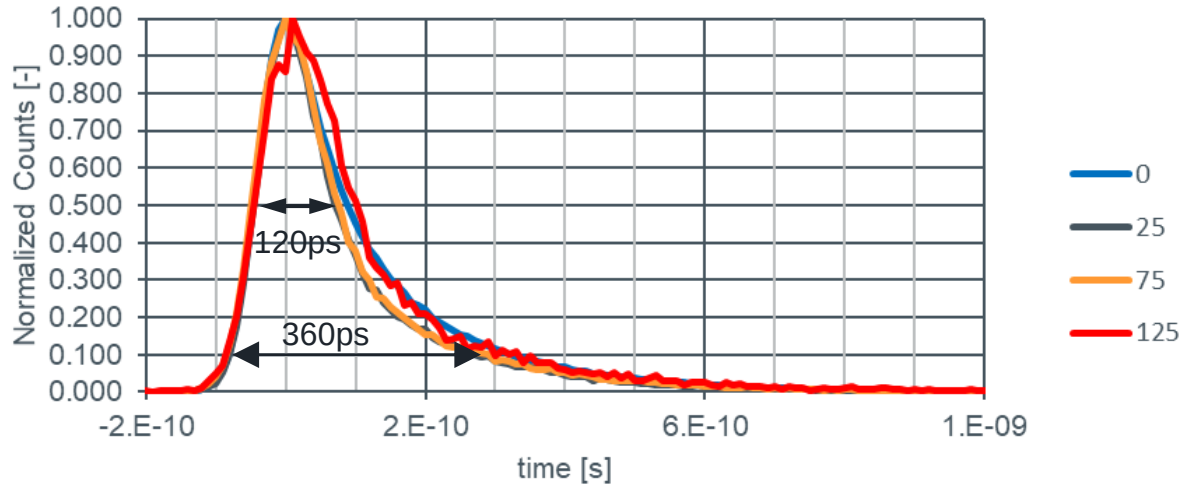


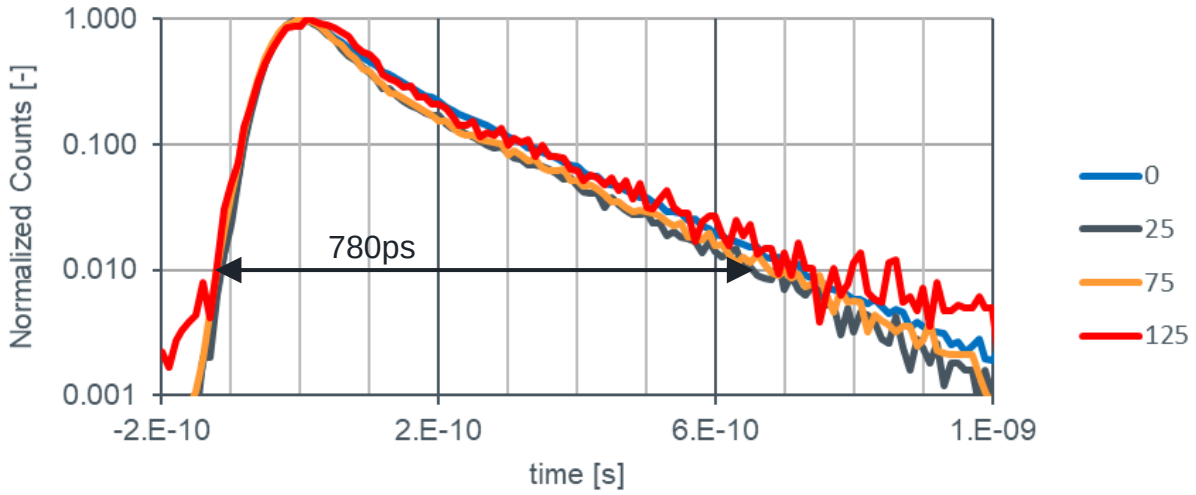


Temperature Impact on Jitter

940nm, Vexc=2.0V

- Timing jitter is hardly affected by the temperature
- Good jitter characteristics at 940nm





Performance Table

Typical performance at 2V excess bias voltage and 940nm

Key Performance Indicator	Unit	This Work	ISSW2020
Pixel pitch	um	10.0	~12.5
Technology Features	-	DT, DL	DT, DL
Breakdown voltage	V	17.5	17
Breakdown voltage temperature coefficient	mV/K	20	45
DCR (25°C)	cps	0.7	14
DCR (75°C)	cps	240	270
PDE	%	11	4.5
Timing jitter FWHM	ps	120	145
Timing jitter (FW10%M)	ps	360	310
Timing jitter (FW1%M)	ps	780	790
After pulsing probability at 7ns dead time	%	<0.1	<0.5
Cross talk probability	%	2.3	0.8

Thank you for your attention!