New SPAD Device dspc

Third Generation

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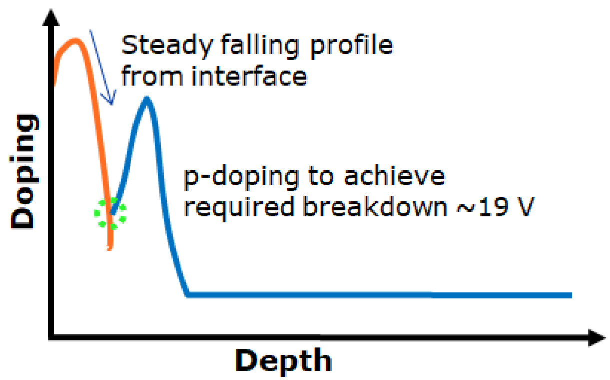
Content

Intro – A fundamental issue in SPAD design

- A major issue with SPAD device designs is, that often there is a doping hump, just before the multiplication area. To reach a required “low” breakdown voltage the substrate doping is too low, so an additional implant is needed.



- Which means that the photon detection probability is reduced and highly depended on the excess bias (at least until it saturates).
- One can choose if the limitation should be for the short or the long wavelengths, by the placement of the doping. But as implantation cannot easily reach deep, usually the long wavelength range is adversely affected.

Intro – A fundamental issue in SPAD design

- It is known from photodiodes or pixels that for high efficiency charge transfer, dips or humps in the electrostatic potential are to be avoided.
- A perfect SPAD device would amplify every photon generated carrier in the multiplication region. None is lost or collected without avalanche multiplication.
- In real SPADs many carriers are hindered to reach the multiplication region and get collected without amplification in the virtual guard ring.

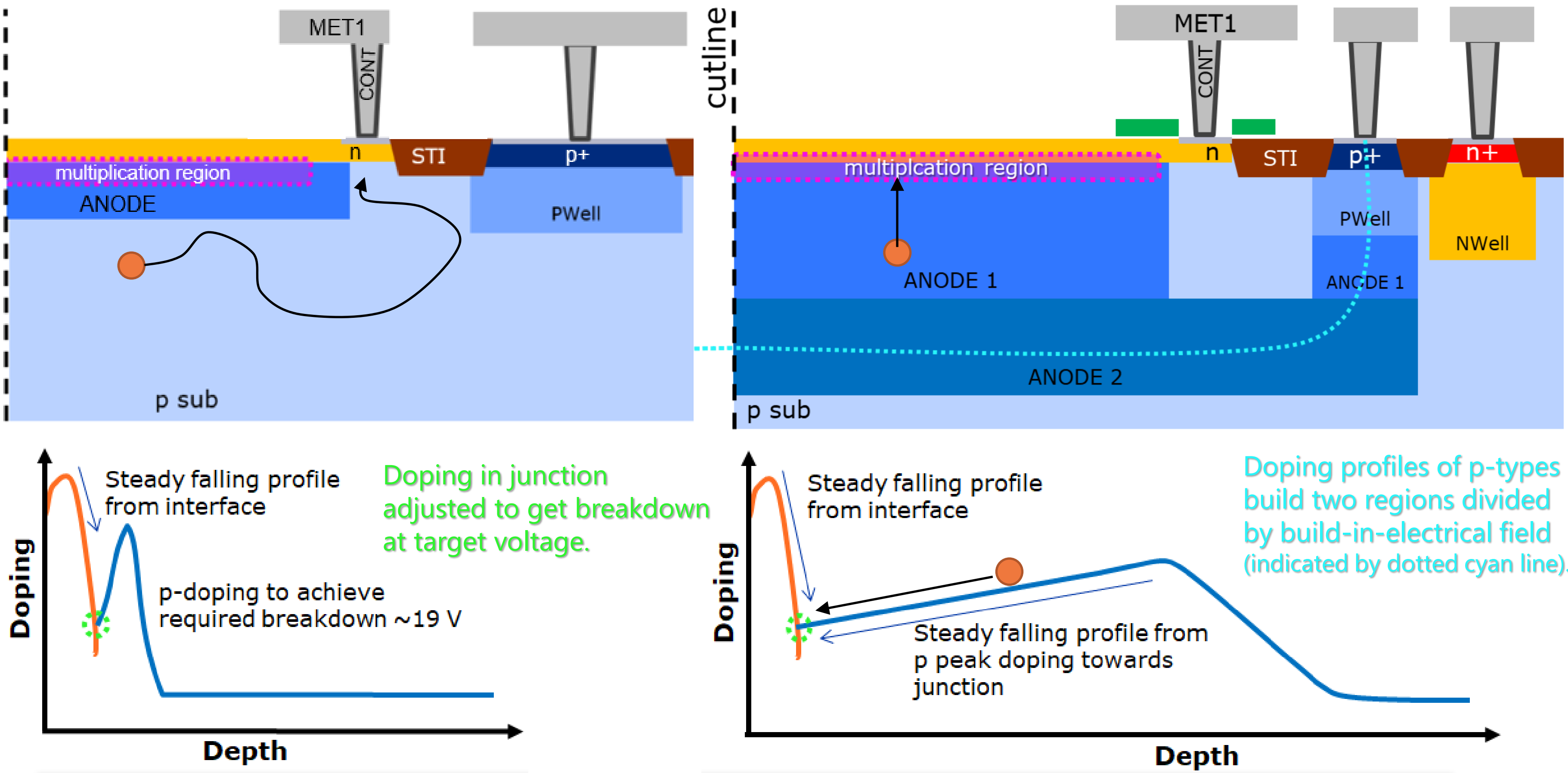
- Several ideas try to improve the situation:

Method	How it works	Limiting factors	Example
High BV/EB	Using a high Breakdown Voltage or high Excess Bias to overcome the potential barrier of the doping hump with a strong electrical field.	***costly*** (requires high voltage process) ***slow*** and high ***power*** consumption less good ***Fill Factor*** (high voltage control needs space)	IMEC Charge Focusing SPAD
Deep Well	Bring the junction (and the hump) deeper, using deep wells or buried layers (epitaxy).	***costly*** (requires special process) limited ***manufacturability***/yield (thick resist required, large design rules, high energy implant, less good controlled)	Eric Webster, IEEE Electron Device Letters, Vol. 33, NO. 11, p 1589-91
Reach Through	Balance the doping to reach through the hump with the depletion at breakdown .	limited ***manufacturability***/yield (requires precise doping) ***patent*** protected (~12 years)	Toyota, Niclass, US9257589
Large Device	Use larger devices, so the carriers will spill over and less likely be collected in the low gain virtual guard ring (Increase area against perimeter).	not usable for imager (no high resolution) ***costly*** (large chip size) ***after pulsing*** issue (scales with device area) ***slow*** and high ***power*** consumption (large capacity) limited ***dynamic range*** (high DCR, long dead time)	Edoardo Charbon, Video: "Photon counting cameras for quantum imaging applications"

Concept

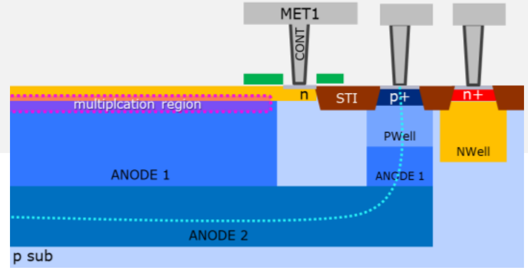
Barrier free SPAD - dspc

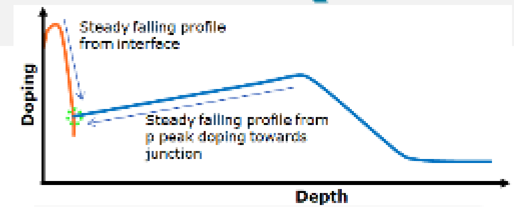
Concept – barrier free SPAD - dspc



- Anode formation is split in two layers:
  1. The upper one defines the multiplication region and the virtual guard ring (ANODE 1) .
  2. The lower one forms the doping peak and isolation as well as the low ohmic connection to the contact (ANODE 2).

Concept - dspc





Advantages of the design:

1. No unwanted potential barrier. High gain for RED/IR with low Excess Bias.
2. Multiplication region and virtual guard ring close to the surface. No thick masks needed, small designs rules (good Fill Factor) and tight manufacturing control (of BV for example).
3. Confined collection volume. Lower DCR, less Cross-Talk and smaller RED/IR Jitter.
4. Compatible regarding the pins (readout/quenching) and footprint with the existing devices dspada and dspb.
5. Dual operation mode, with confined collection volume for low Excess Bias and extended collection region by the usage of higher Excess Bias.
6. 15-fold higher current capability due to significantly lower series resistance, allows for faster passive quenching and simplified active quenching .

Disadvantages of the design:

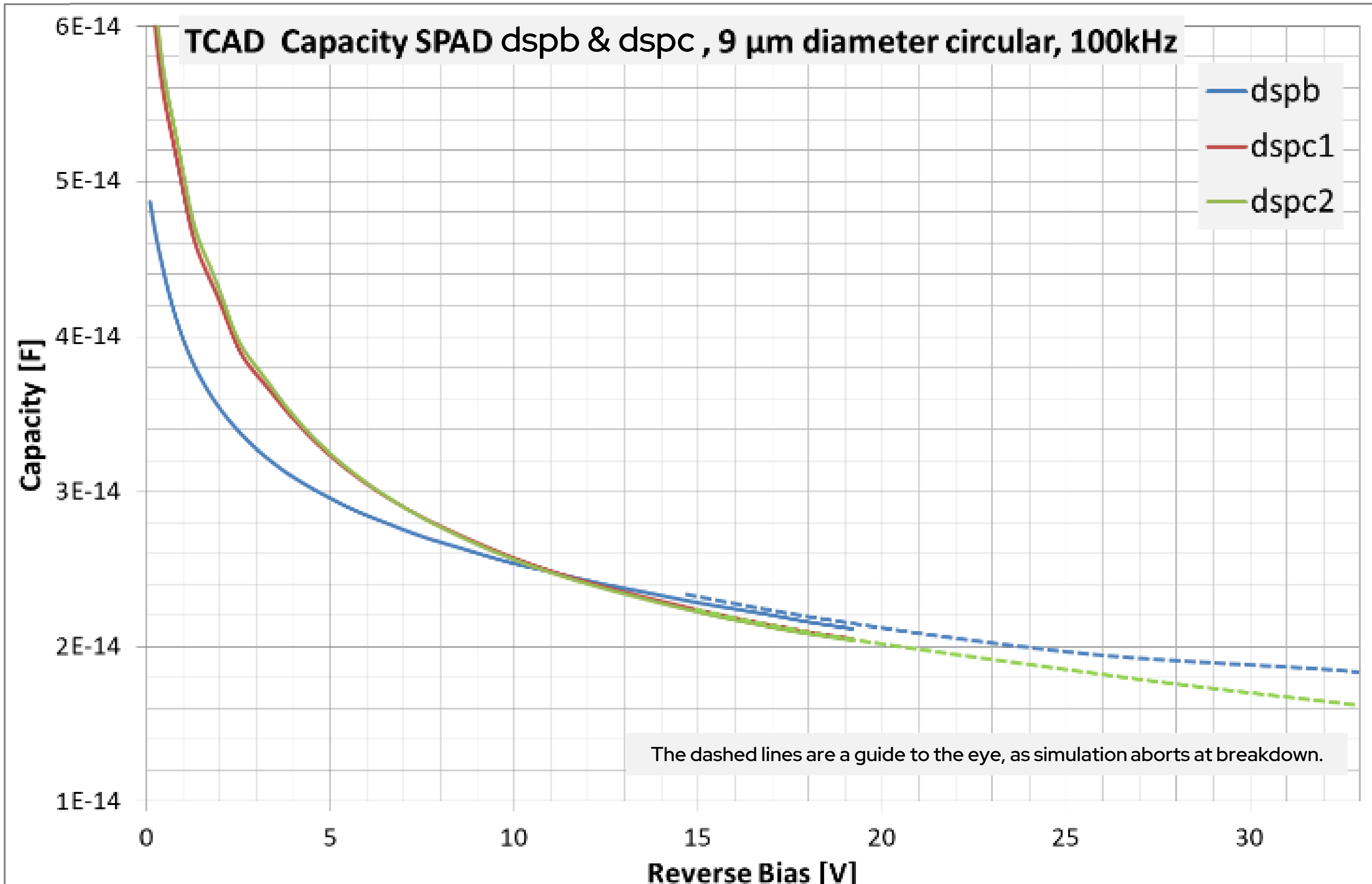
1. One additional mask and high dose/energy implant for the buried peak and isolation.
2. Due to the confined collection volume, there is the need for a drain junction (guard ring) if large arrays are built, to sufficiently prevent the spill over of carriers from outside.
3. To fully unleash the performance, quenching must be adapted to deal with the higher current capability and control the after pulses.

Results

CV, IV, Gain, DCR, PDP, Summary

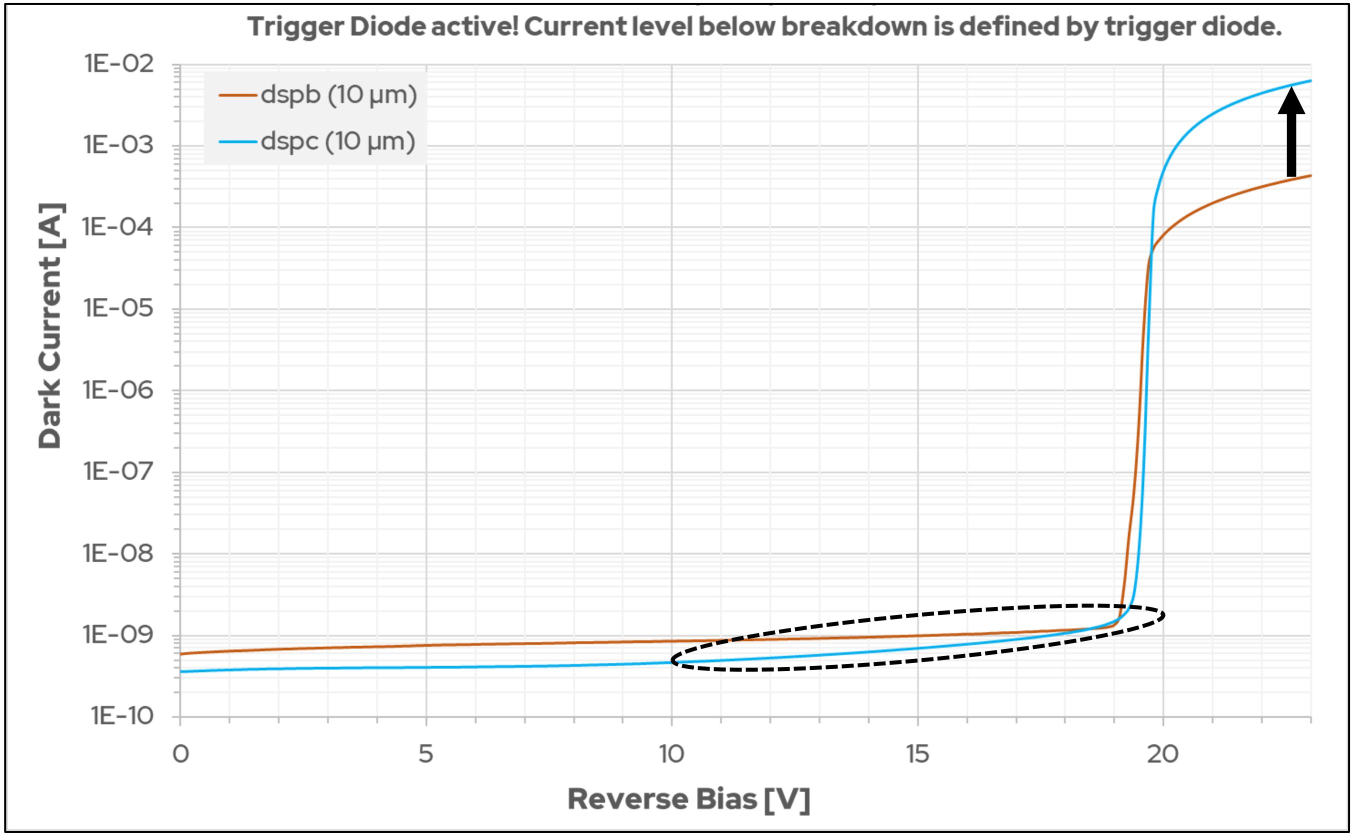
Results – Capacitance

- dspc has slightly lower capacity (~5%), in the “relevant” bias range (>15 V)
- This is due to the different anode doping profile.



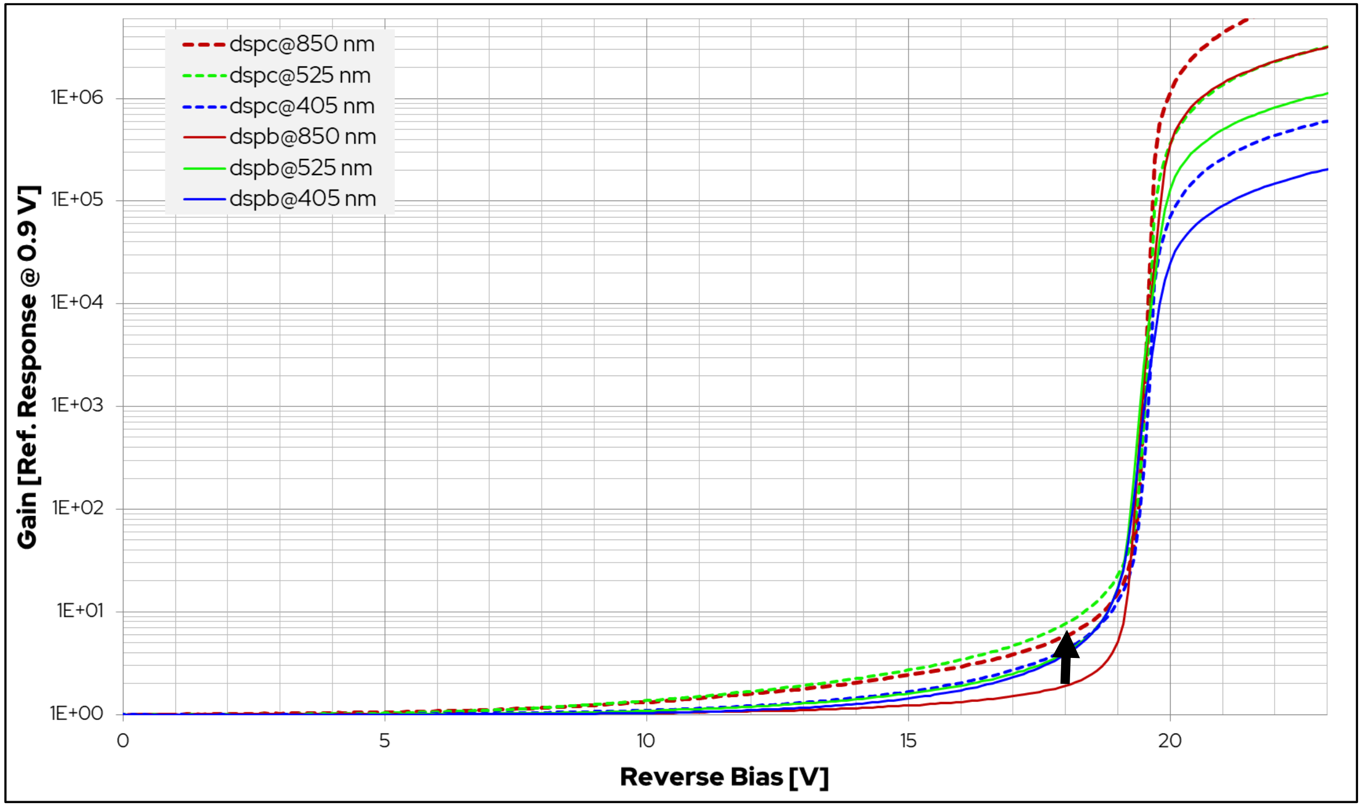
Results - IV

- The IV-curve shows that the breakdown voltage was perfectly hit and the new device dspc has exactly the same BV as the previous dspb.
- In addition it can be seen that the breakdown current is 15 times higher for the dspc.
- This is because of the significant reduced Anode resistance.
- The slope in the current below breakdown indicates how much better the collection efficiency is.



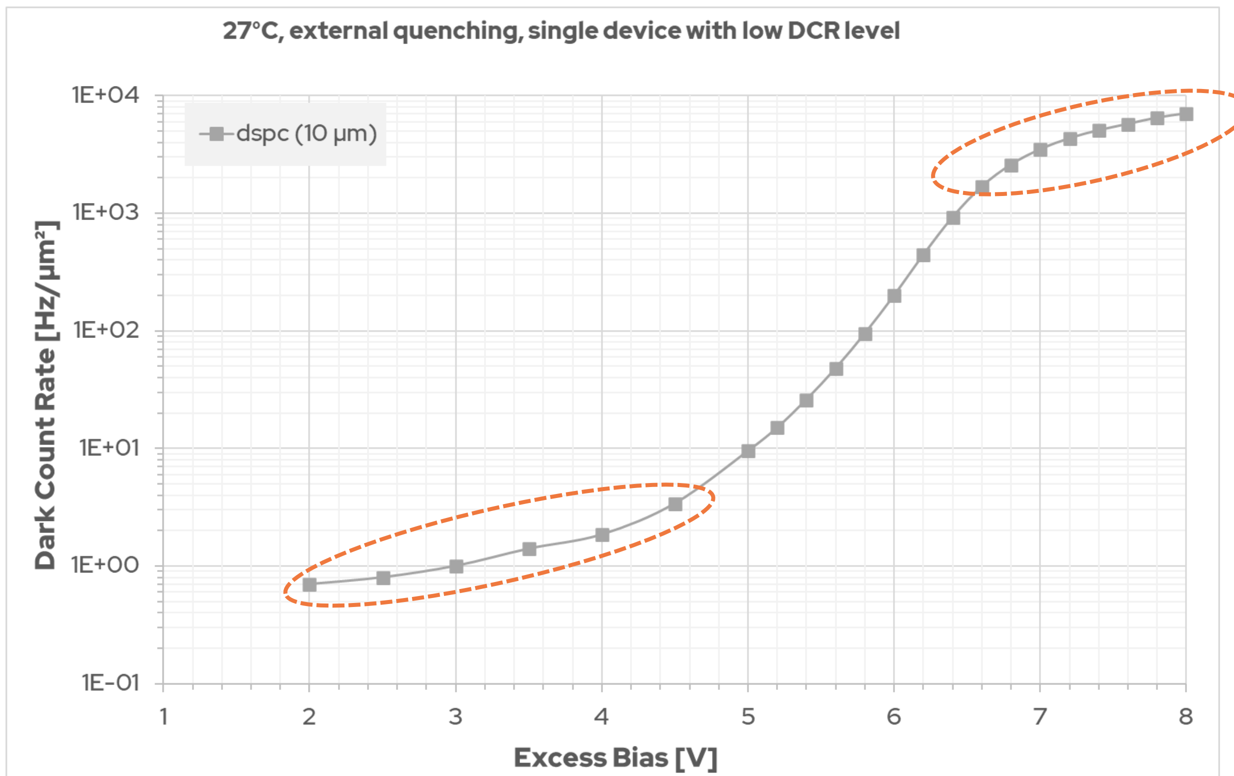
Results - Gain

- A gain measurement can be done without quenching and is below the breakdown (APD mode), thus it tells how good the collection efficiency is with no Excess Bias.
- Especially the IR gain is significantly improved compared to dspb.
- The solid brown curve shows how poor the IR gain usually is.
- The dashed brown curve is the IR gain of the dspc.
- This is a 3x gain improvement for long wavelengths.



Results - DCR

- As expected from the design, the dspc shows two regions of operation.
- At low Excess Bias (< 5V) the device works “isolated” and the DCR is low. Whereas with higher EB, the DCR increases significantly and finally “saturates” for > 7 V EB when, there is no isolation anymore.
- Overall, the device shows a reduced DCR even though it has a higher PDP.

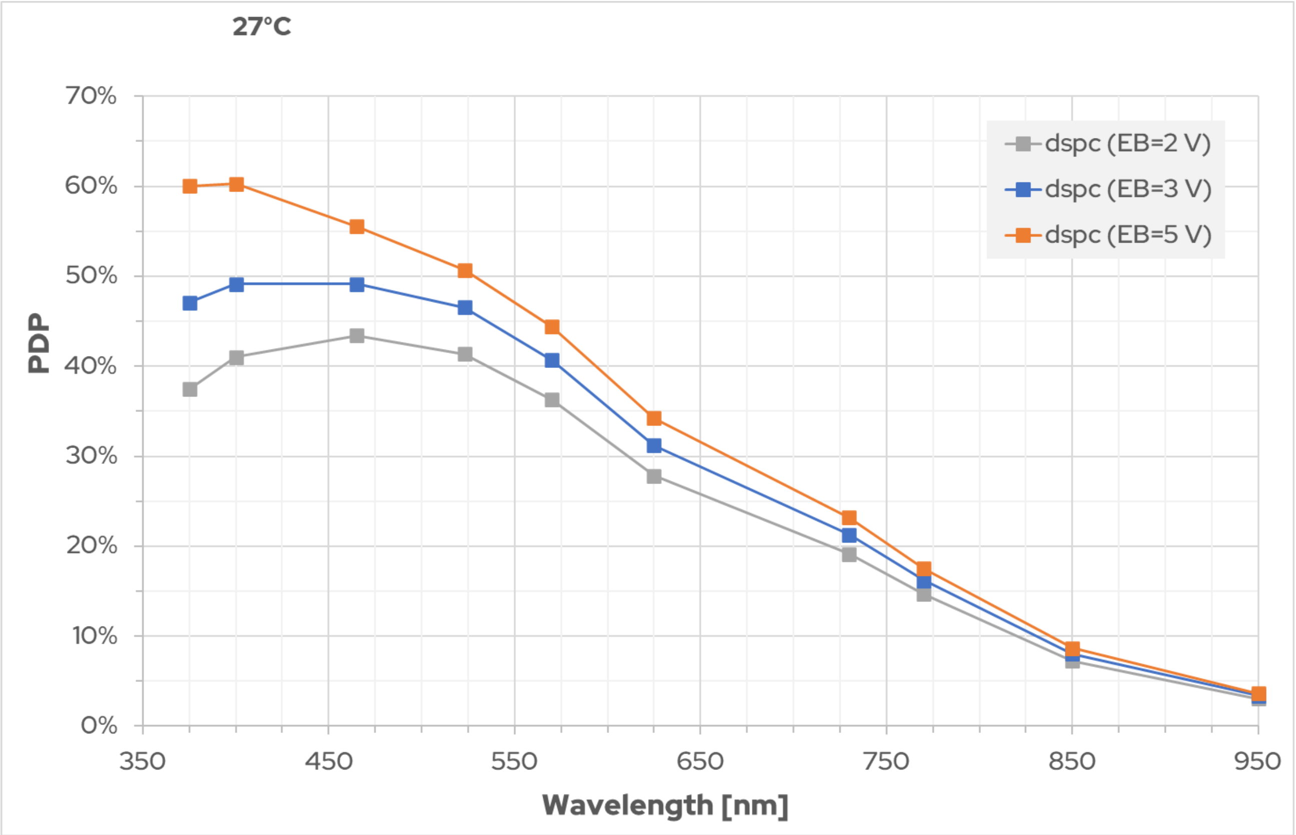


Device	DCR [Hz/µm²]*	Spec
dspada	6.3	8
dspb	14.32	12.5
dspc	6.05	NA

*passive quenching, 2 V EB, Median 68 samples

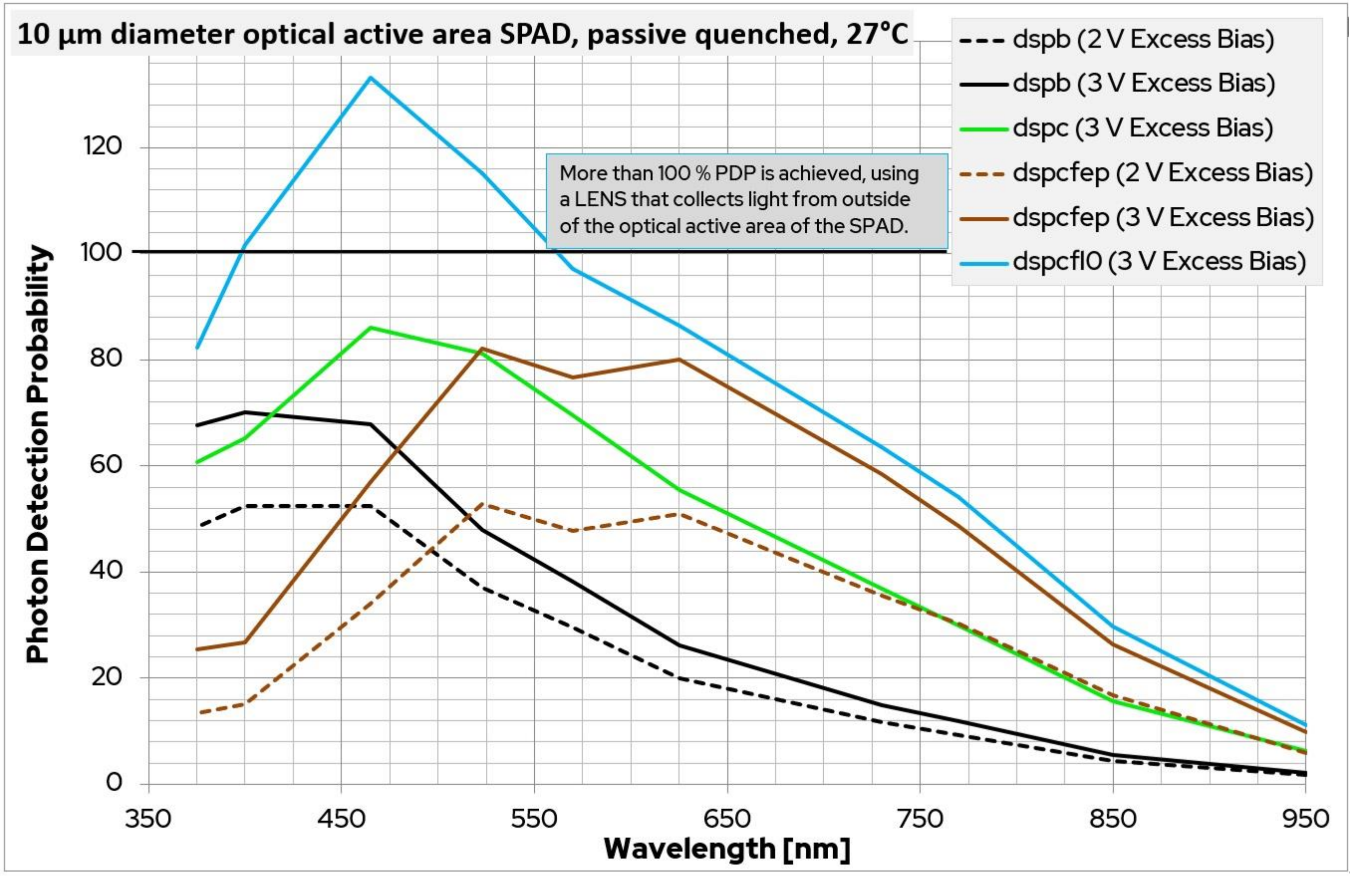
Results - PDP

- Here we are in doubt, as we got different results with different methods.
- Let us start with our first results from a chip level measurement. (SPAD die bonded to external passive quencher).



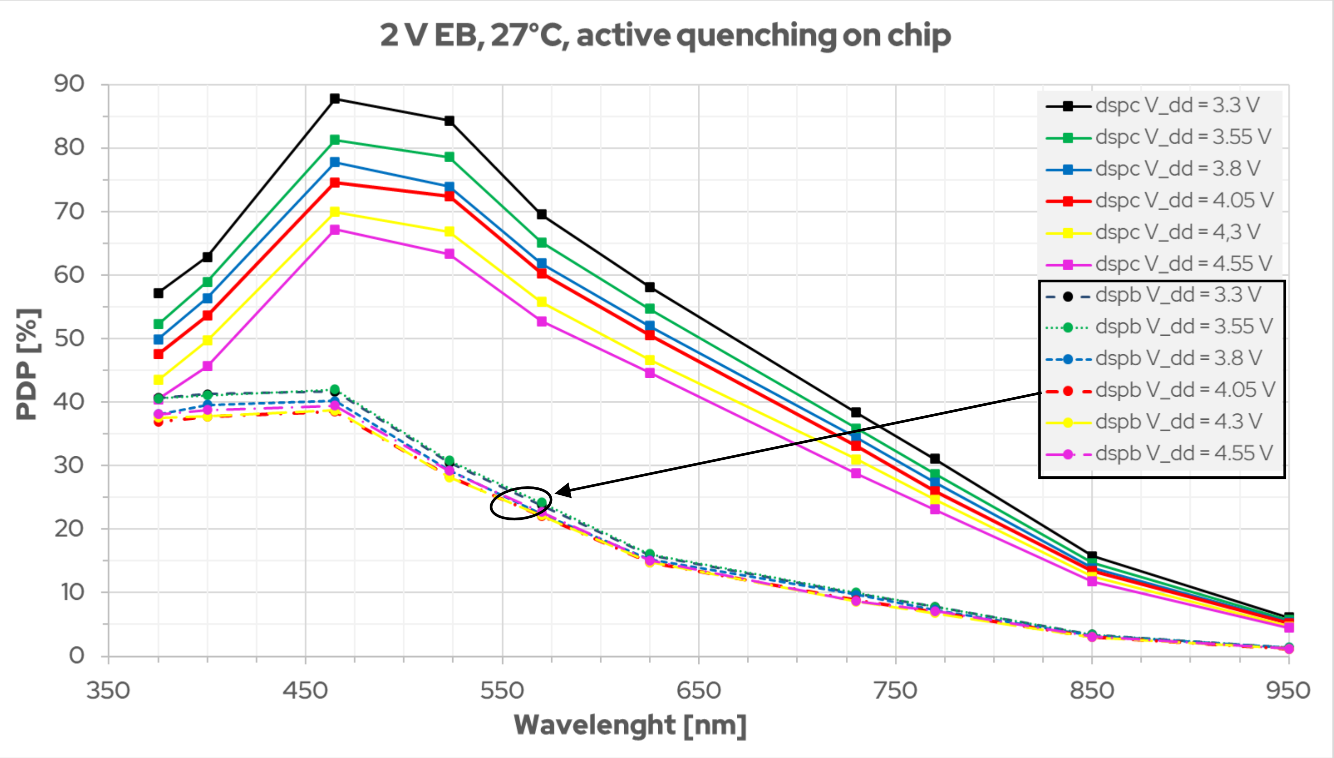
Results - PDP

- Second is a wafer level measurement with external passive quenching. (SPAD connected via probe needles to the external passive quencher).
- Our reference the dspb matches the spec relatively well. The dspc has significantly higher PDP with this measurement.
- dspcfep and dspcfl0 show additional improvements which can be applied to other SPADs as well.
  -> sponsored talk



Results - PDP

- Third is a wafer level measurement, with on chip active quenching. (Quencher driver connected via probe needles to the oscilloscope).
- Our reference the dspb matches the spec relatively well. The dspc has significantly higher PDP with this measurement. We get higher DCR by this method as well.
  The DCR reduces for increasing VDD up to ~4 V (red curve), for higher VDD it strongly increases.
- The PDP depends on how deep below the breakdown the quenching is done.
- dspb is nearly not changing on that.



Results Summary

- We have seen several expected improvements for the new device concept.
- The capacitance is slightly lower in the relevant voltage range around breakdown.
- Breakdown was matched to dspb (19.6 V) and the breakdown current is higher.
- Gain for longer wavelengths is no longer reduced, doping hump and reaches as good levels as for short wavelengths.
- The DCR is lower (due to the confined collection volume) for Excess Bias below 5 V and with higher Excess Bias the device enters a second operation mode.
- PDP is still with a question mark, as we did get different values for different measurement configurations. Likely after pulsing is causing the discrepancy.
- Cross Talk and Jitter are still to be measured.

Device	Capacitance	Current	Gain 850 nm	DCR [Hz/µm²]	PDP 850 nm	Fill Factor UV/BLUE	Fill Factor RED/IR
dspada	60 fF	100%	40%	6.3	2%	18.1 %	18.1 %
dspb	60 fF	100%	100%	14.3	5%	27.4 %	32.9 %
dspc	57 fF	15x 100%	3x 100%	6.0	8% or 15% ?	29.3%/23.1%*	35.1%/27.7%*

10 µm diameter optical active area, 2 V Excess Bias, passive quenching, 27°C, *including guard ring

Critical Discussion and Outlook

- The larger the device, or more precisely the bigger the volume of barrier free collection, the more likely after pulses show up.
- For our devices, a dead time of > 100 ns is needed to sufficiently suppress unwanted correlated pulses. Faster quenching is a challenge, unless you cancel out correlated pulses by their time stamp. But still, this will block the SPAD from sensing a wanted photon, which in turn is like a longer dead time.
- We will further investigate what could be done on the quenching side, to work best with this new device. Jitter, cross talk and PDP/DCR for different sizes are on our list (need a solution for the after pulses to be trustworthy).
- dspc is the first attempt to realize a new concept, and obviously needs a bit more time to get ready for a release.

Thank you.

Feel free to get in touch. We are happy to hear your thoughts.

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