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# Fast-gated $16 \times 16$ SPAD array with on-chip 6 ps TDCs for non-line-of-sight imaging

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# Outline

## Non-line-of-sight (NLOS) imaging

1. Working principle
2. System requirements
3. State-of-the-art

## 16 × 16 SPAD array architecture

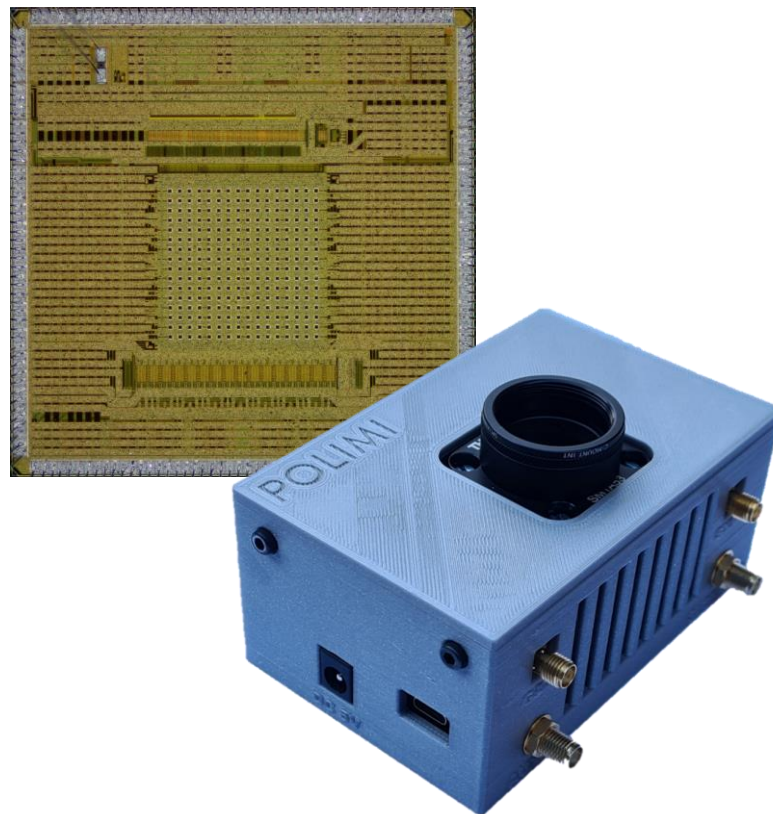
1. SPAD performance
2. Time-gated frontend
3. Resource sharing
4. Time-to-digital converters (TDCs)

## Camera overview

## Characterization results

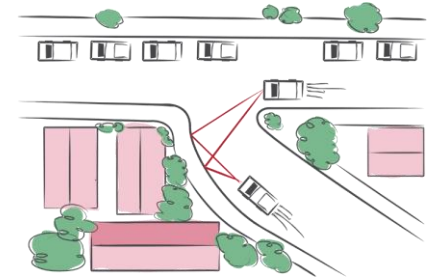
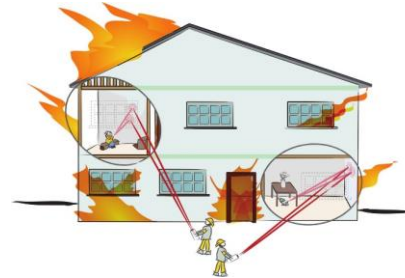
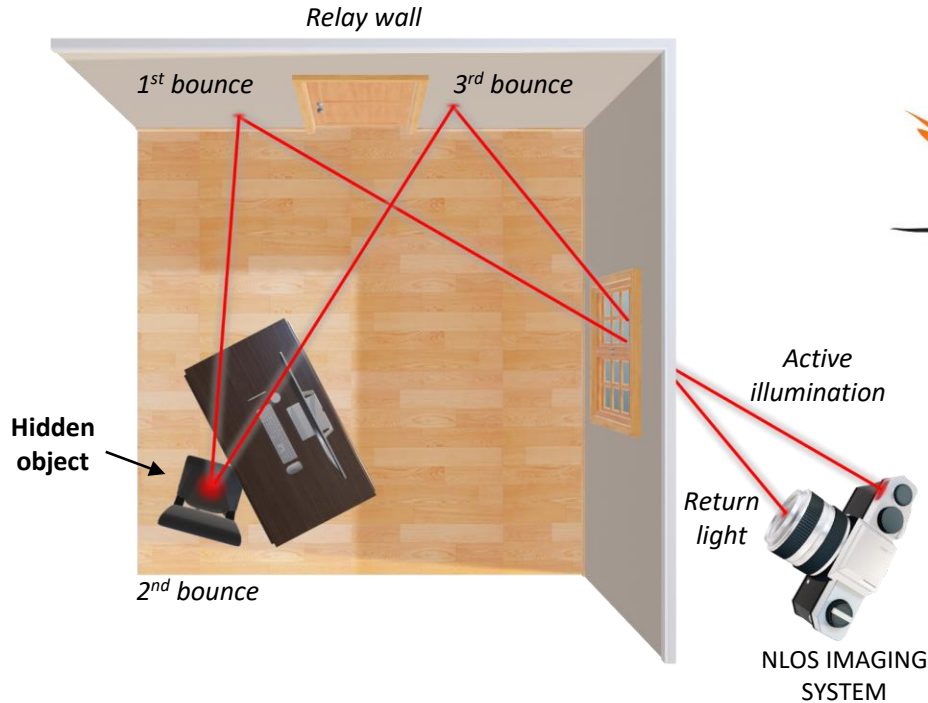
1. IRF
2. Time-gating
3. Conversion linearity

## Conclusions



# Non-line-of-sight imaging

Reconstruction of hidden objects by collecting light that diffuses multiple times

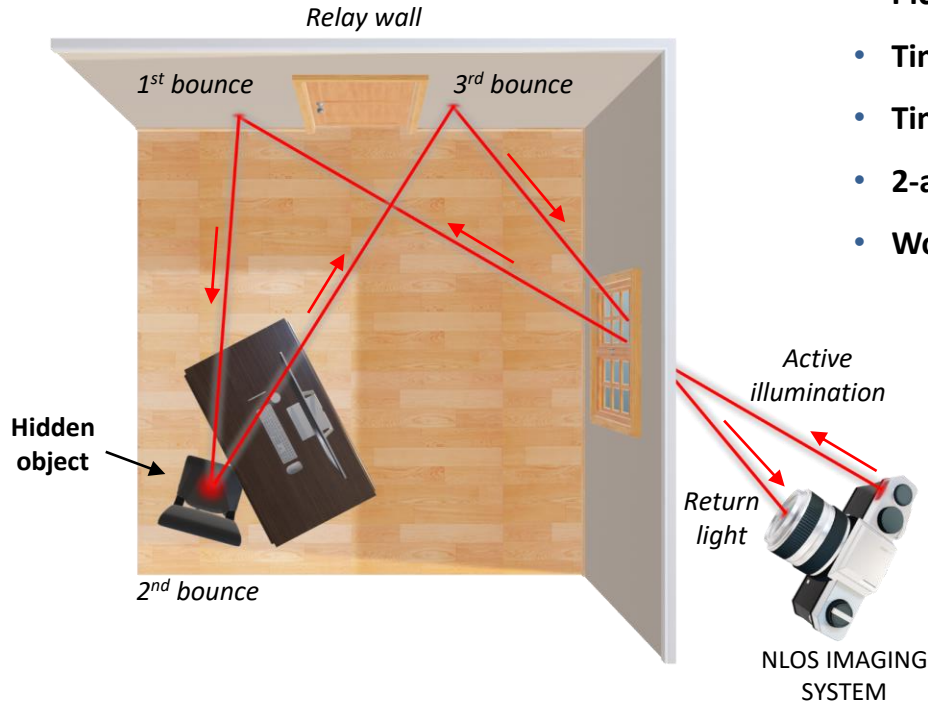


## Examples of applications:

- Security and defense
- Search and rescue
- Monitoring hazardous environments
- Autonomous vehicles and ADAS
- Remote sensing



# Time-of-flight NLOS imaging system



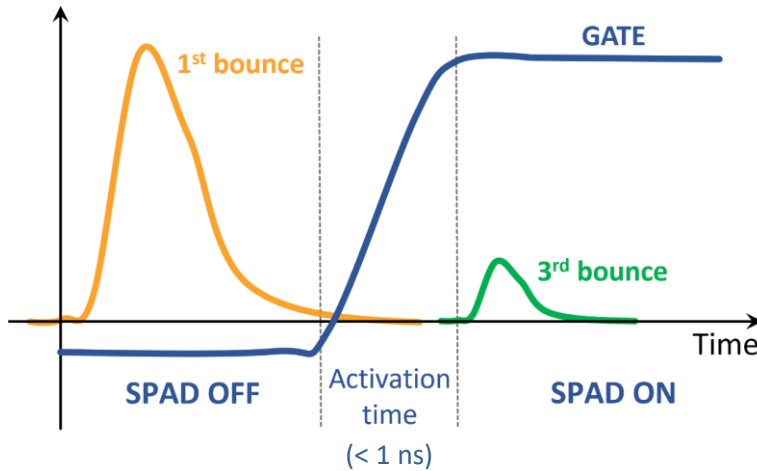
- **Picosecond pulsed laser** → illuminates a relay wall
- **Time-resolved detector** → acquires return light
- **Time-of-flight processing unit** → time stamps single-photons
- **2-axis scanning system** → increases image resolution
- **Workstation** → runs the reconstruction algorithms

# Detector requirements

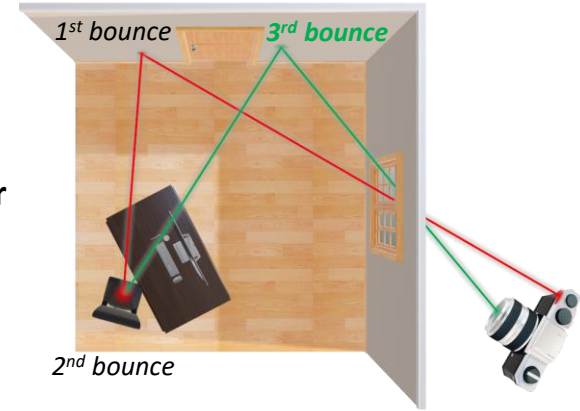
- Multiple scattering events → faint **3<sup>rd</sup> bounce** signal → **single-photon sensitivity**
- Undesired **1<sup>st</sup> bounce** reflections → time-domain filtering → **time-gated detector**



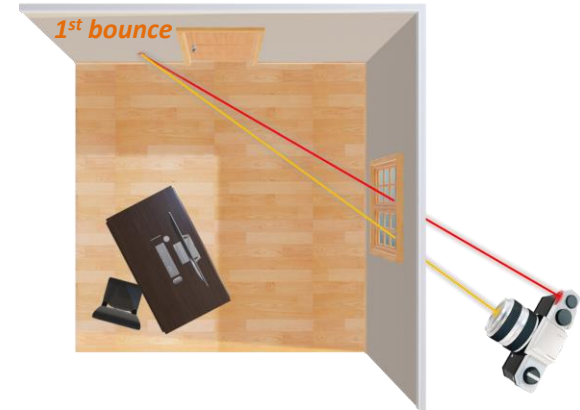
NLOS imaging requires **SPAD**-based sensors



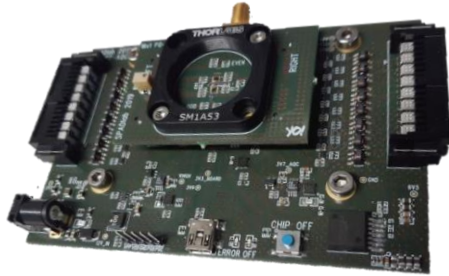
## INDIRECT LIGHT PATH



## DIRECT LIGHT PATH



# State-of-the-art



Fast-gated  $16 \times 1$  SPAD array



External TCSPC unit (PicoQuant HydraHarp 400)

- Reaches up to **5 fps**, **0.5 MP resolution**
- Hardware limited to **few pixels**, **8 TCSPC channels**

J. H. Nam, E. Brandt, S. Bauer, X. Liu, M. Renna, A. Tosi, E. Sifakis, and A. Velten,  
“Low-latency time-of-flight non-line-of-sight imaging at 5 frames per Second,” *Nature Communications*, vol. 12, no. 1, 2021.

## NLOS at video rates → Design of a new fully-integrated $16 \times 16$ SPAD array:

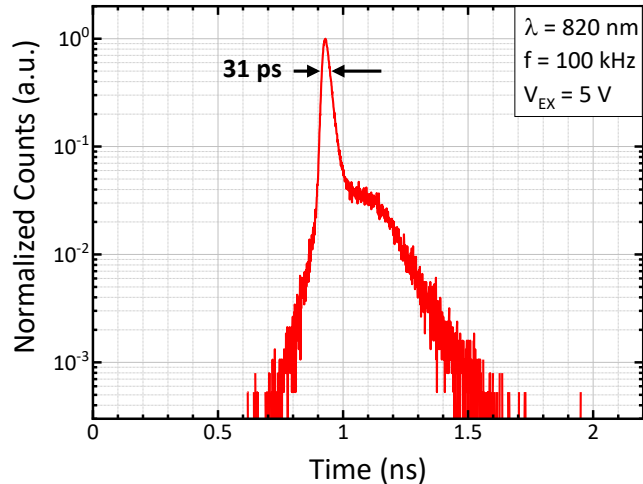
- Parallel acquisition: **multi-pixel sensor**
- Narrow IRF: **few tens of ps (FWHM)**
- Fast-gating: **< 1 ns gate-ON transition**
- SWaP-C optimized: **integrated TCSPC processing**



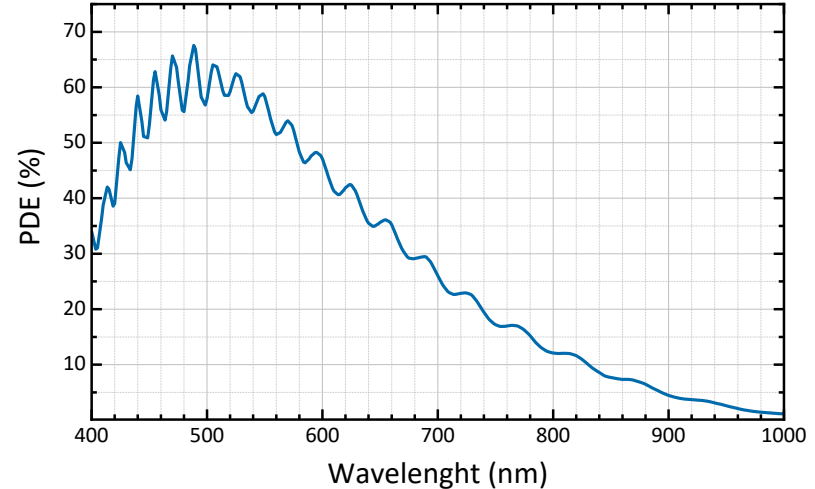
# 16 × 16 SPAD array: fabrication technology

Narrow IRF + High PDE → 160 nm BCD technology by STMicroelectronics

30 ps SPAD timing jitter FWHM



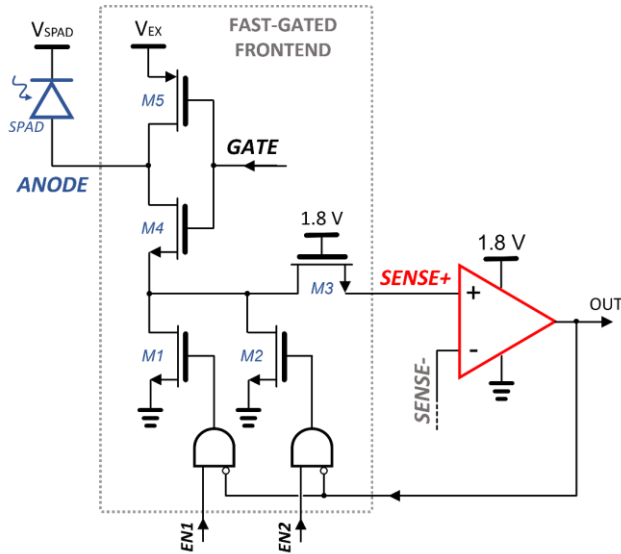
60% PDE @ 500 nm,  $V_{EX} = 5 \text{ V}$



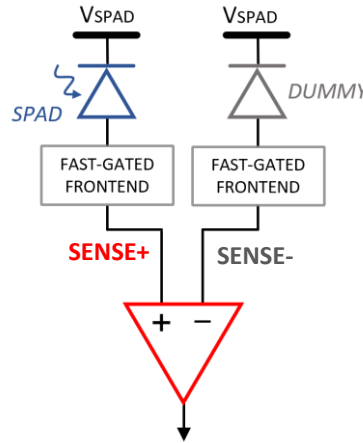
M. Sanzaro, P. Gattari, F. Villa, A. Tosi, G. Croce, and F. Zappa, "Single-photon avalanche diodes in a 0.16  $\mu\text{m}$  BCD technology with sharp timing response and red-enhanced sensitivity," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 2, pp. 1–9, 2018.



# 16 × 16 SPAD array: fast-gated frontend

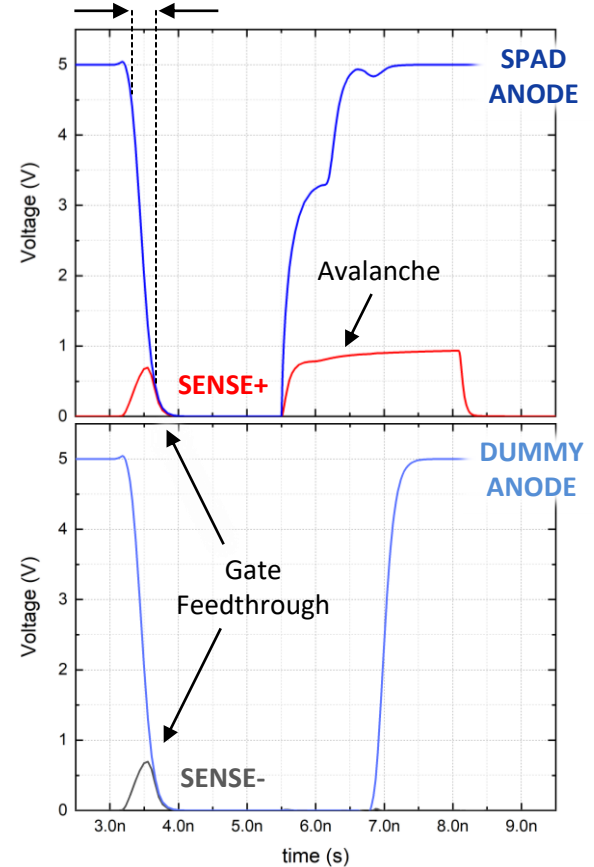


- M1 and M2 programmable to sense avalanches and tune the **activation time**
- M3 for level translation from 5 V (GATE) to 1.8 V (fast comparator)



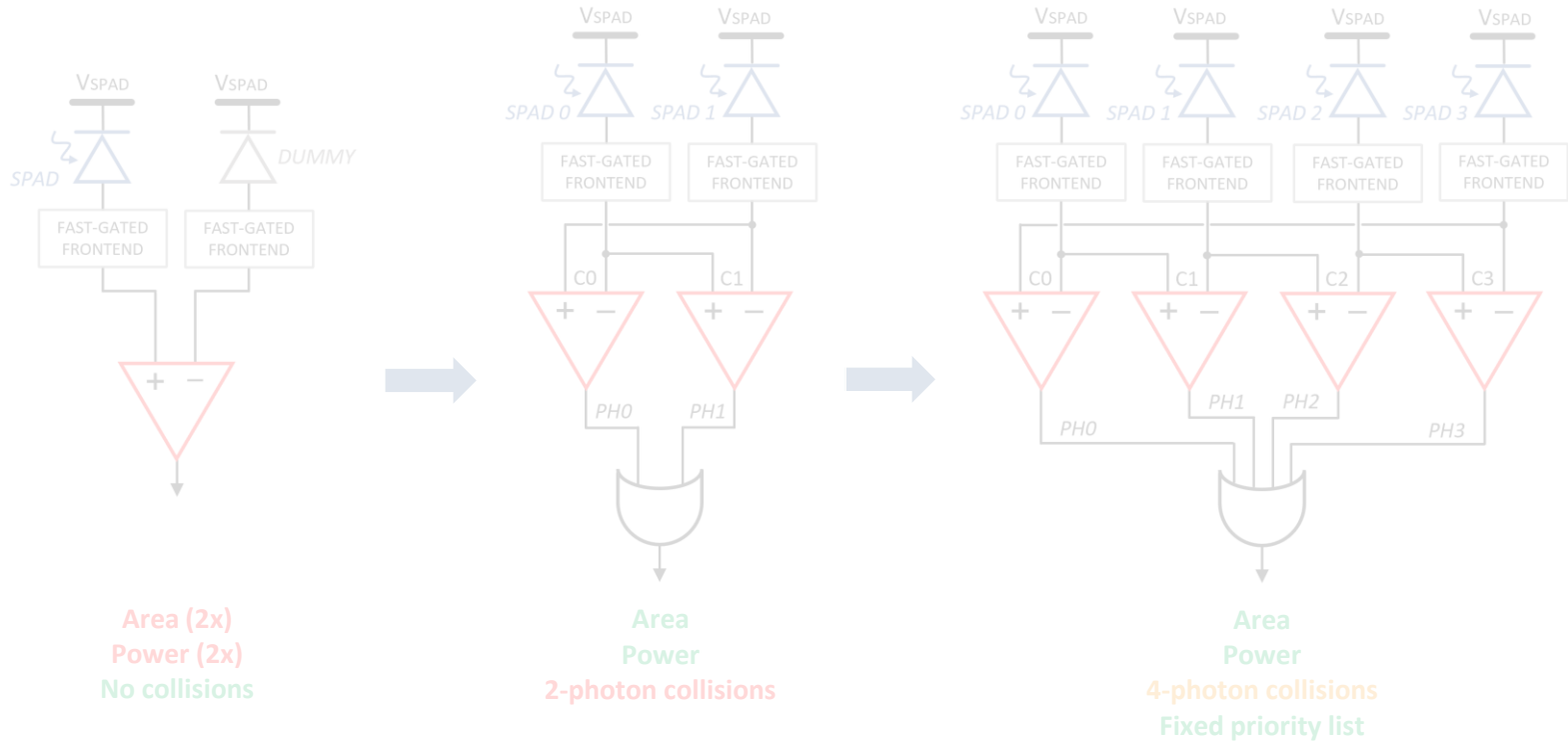
- **Differential sensing** to reject feedthrough pulses
- **Low threshold** for low timing jitter

Activation time < 400 ps





# 16 × 16 SPAD array: differential sensing approaches



# 16 × 16 SPAD array: microcell circuitry

## → 4 SPADs + low-threshold comparators

Low-jitter avalanche sensing  
Optimizes area and power + fast quenching

## → Identification logic

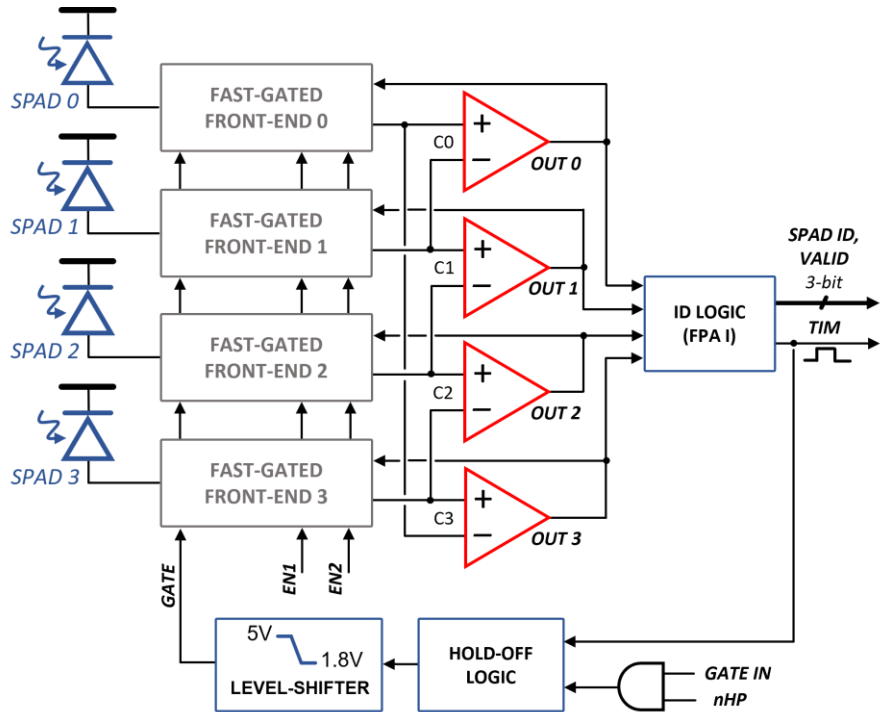
Encodes the firing SPAD address (SPAD ID)

## → Hold-off logic

Forces 30 ns dead-time to reduce afterpulsing

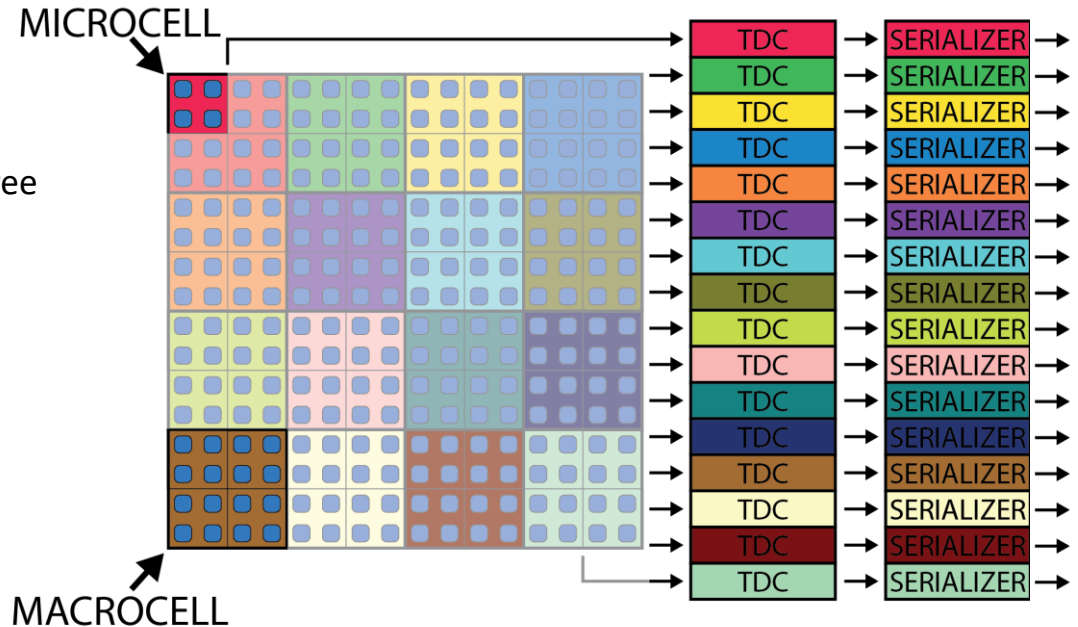
## → 1.8 V to 5 V level shifter

Maximizes  $V_{EX}$ , hence PDE



# 16 × 16 SPAD array: resource sharing

- **Sharing logic:** 2-level fixed priority arbiter tree
  - Microcells: 2 × 2 SPADs
  - Macrocells: 2 × 2 microcells
- **16 Time-to-Digital Converters (TDCs)**
- **16 event-driven output serializers**



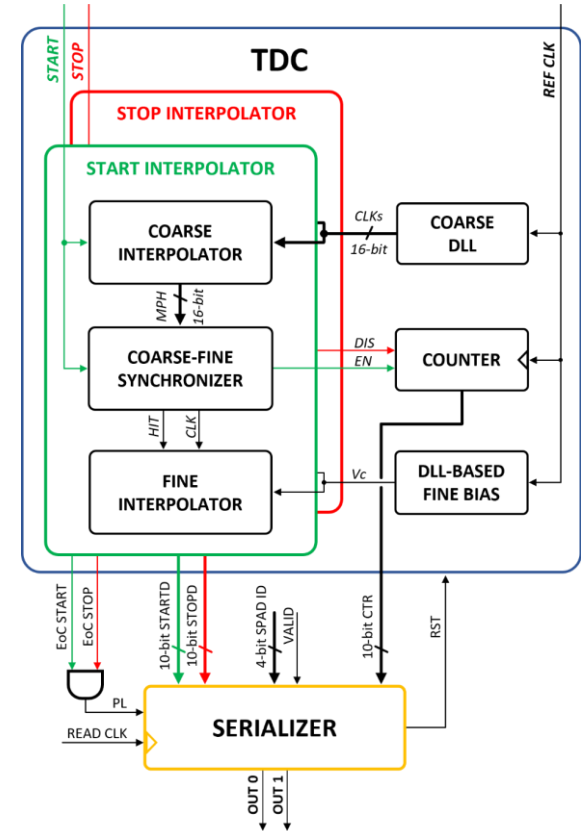
# 16 × 16 SPAD array: TDCs and output serializers

## 16 TDCs:

- START and STOP interpolators → sliding scale → **improved linearity**
- 10-bit counter @ 420 MHz → **FSR = 2.45 μs**
- Coarse multiphase interpolator → **conversion time < 50 ns**
- Single-stage Vernier fine interpolator → **LSB = 6 ps**

## 16 Serializers:

- 18-bit dual-channel @ 200 MHz → up to **10 Mevents/s** per TDC
- **Event-driven readout** → Time-Tagged Time-Resolved (TTTR) operation
- **Pipelined architecture** → conversion during data-transfers



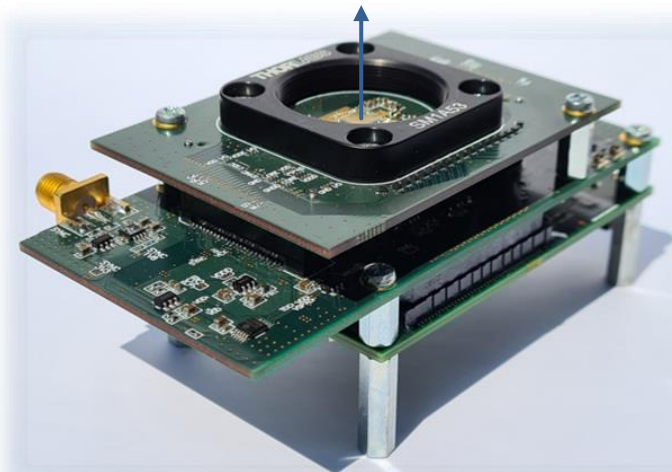
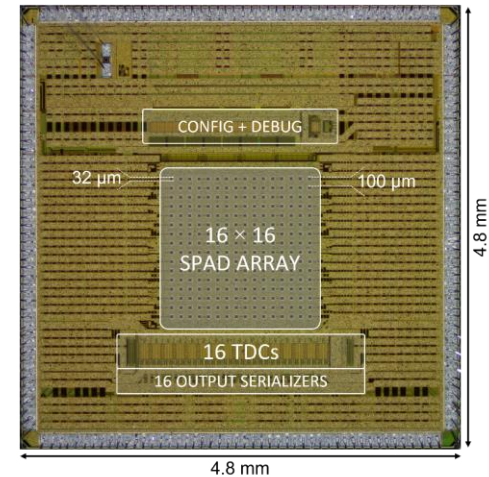
# Camera overview

## IC:

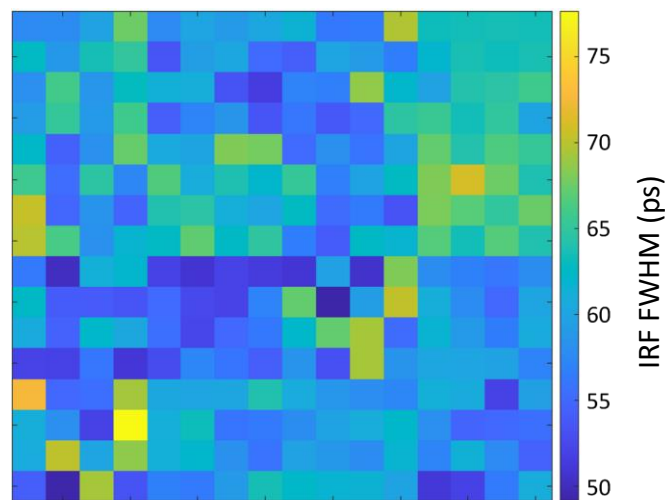
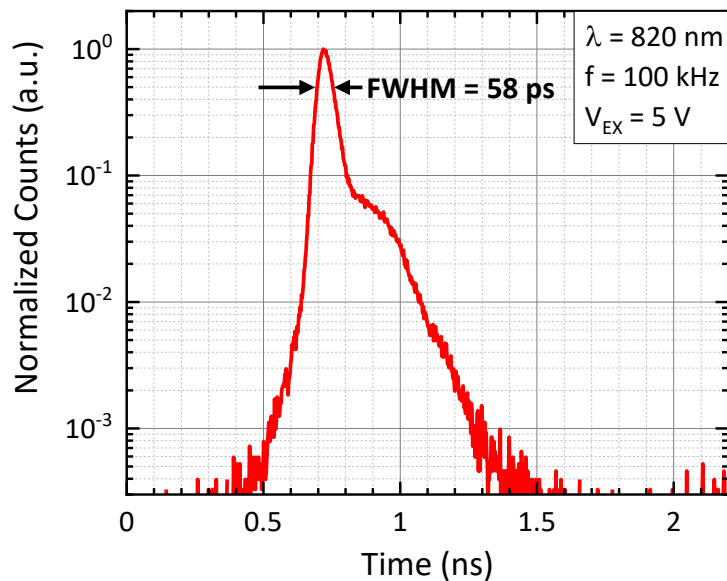
- 4.8 mm x 4.8 mm, PAD-limited
- In-pixel decoupling capacitors + deep trench isolation
- 32  $\mu\text{m}$  squared SPADs @ 100  $\mu\text{m}$  pitch  $\rightarrow$  **Fill-factor = 9.6%**

## Camera:

- **Chip-carrier board**  $\rightarrow$  hosts the wire-bonded IC
- **Power board**  $\rightarrow$  power management + signal conditioning
- **FPGA board**  $\rightarrow$  TCSPC processing + USB 3.0 interface



# Characterization results: instrument response function



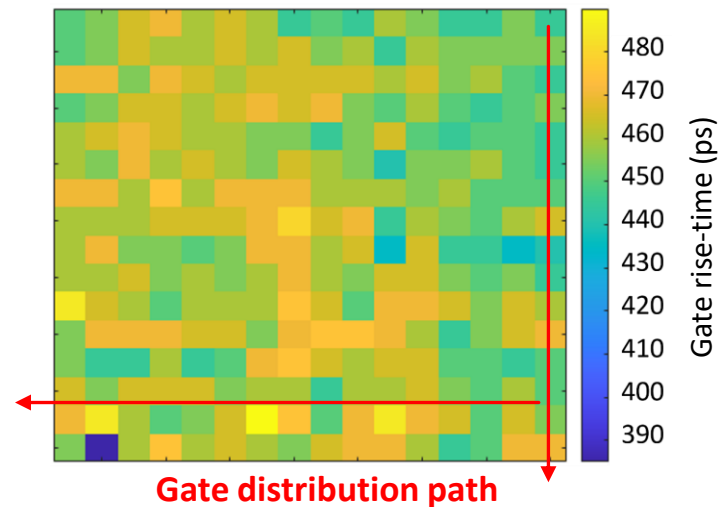
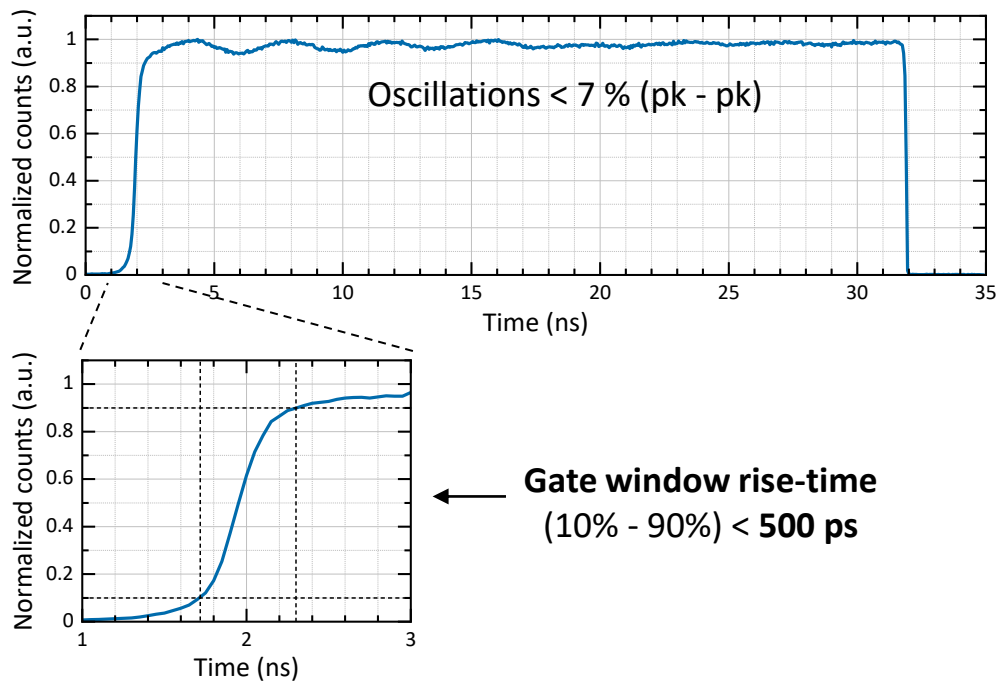
Average = 62 ps

Max = 77 ps

→ Values obtained by illuminating the array with a 10 ps 820 nm pulsed laser running at 100 kHz



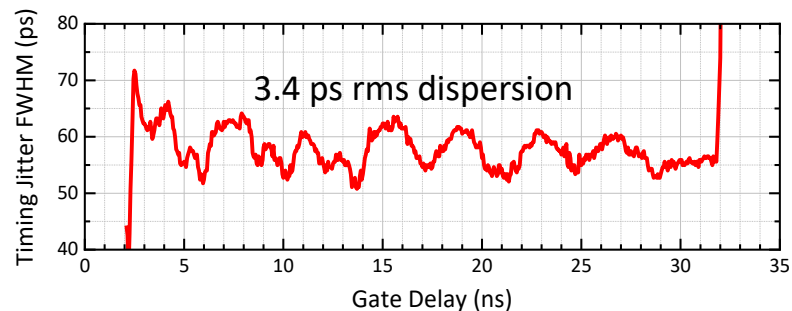
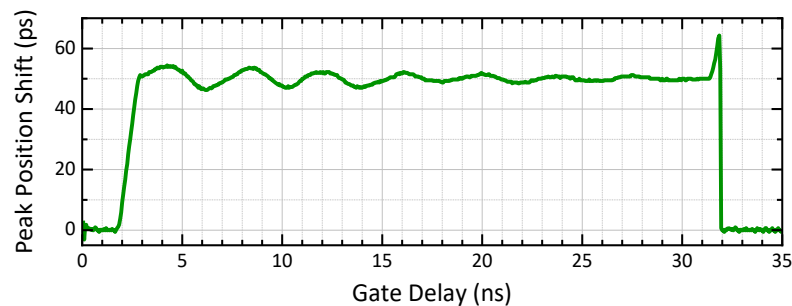
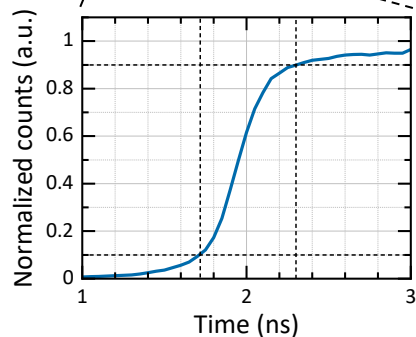
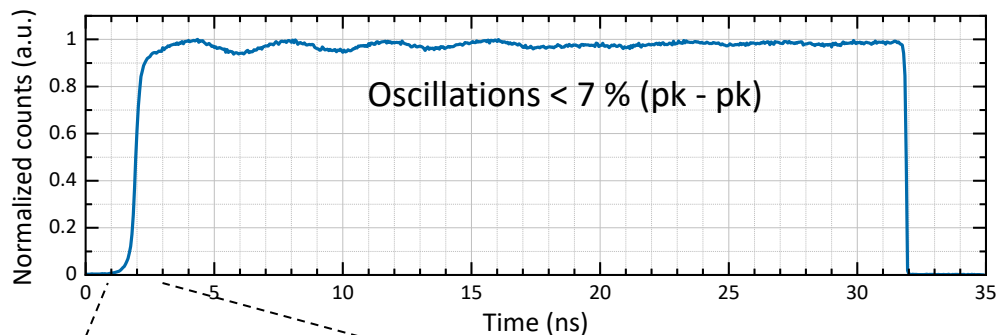
# Characterization results: gating performance



→ Values obtained scanning a 52 ps (FWHM) 850 nm pulsed laser at 50 ps steps across a 30 ns gate window at 1 MHz repetition rate



# Characterization results: gating performance

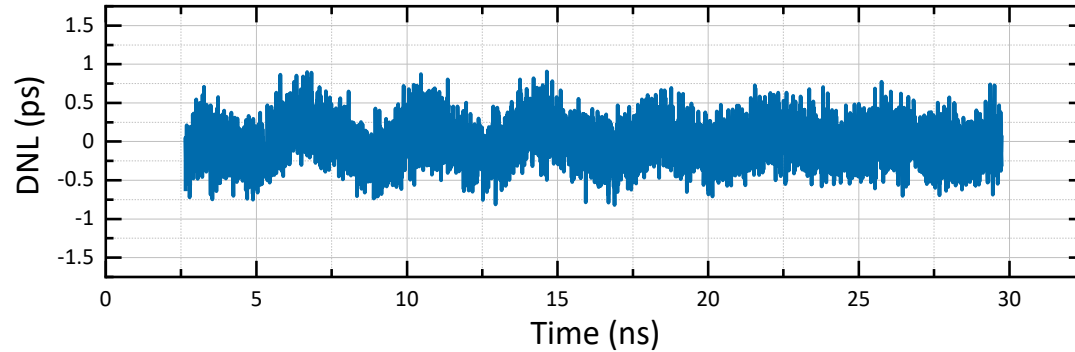


→ Values obtained scanning a 52 ps (FWHM) 850 nm pulsed laser at 50 ps steps across a 30 ns gate window at 1 MHz repetition rate

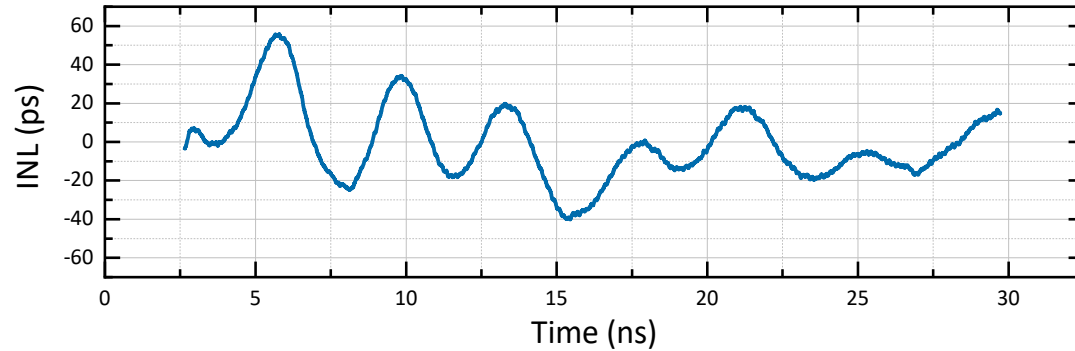




# Characterization results: conversion linearity



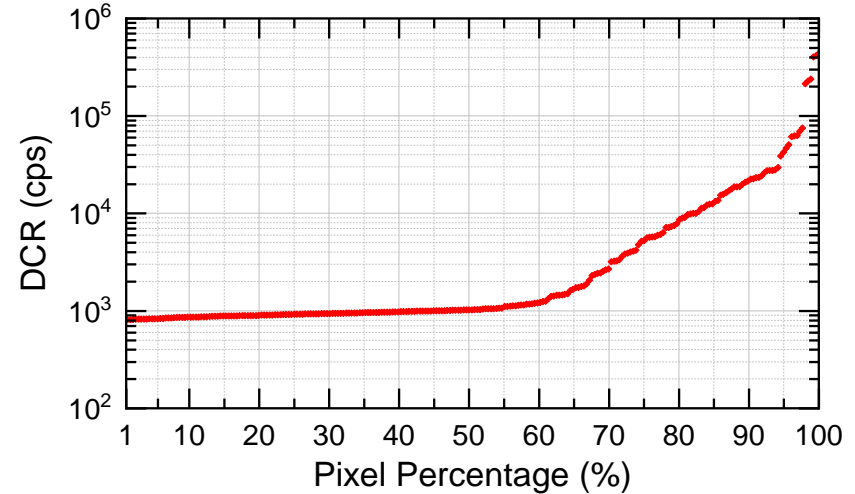
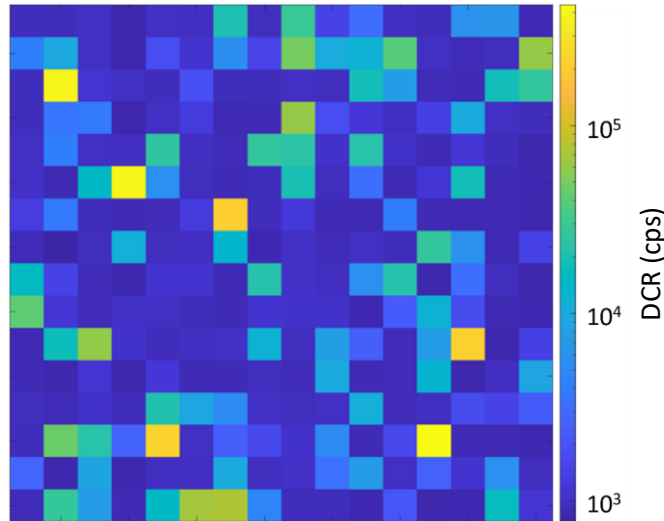
→ DNL = 250 fs rms (0.04 LSB)



→ INL = 22 ps rms (3.6 LSB)



# Characterization results: dark count rate



**Median DCR = 1 kcps @ operating temperature ( $\sim 45^\circ\text{C}$ )**  
→ Temperature increase due to **500 mW power consumption**

# Conclusions

## High-performance NLOS SPAD array:

- $16 \times 16$  pixels
- **Sub-ns gating**
- State-of-the-art IRF:  
**FWHM < 75 ps, 62 ps on average**
- 16 integrated high-resolution TDCs

## Integrated in a portable camera:

- $10 \times 7 \times 5 \text{ cm}^3$
- **USB 3.0 connection** + single 5 V power supply
- **Up to 160 Mevents/s sustained throughput**
- SM1 or C-mount thread for filters and lenses

→ **NLOS measurements ongoing at the University of Wisconsin-Madison**



This work was partially supported by “DARPA REVEAL: Scene Recovery using an extended Plenoptic Function”, grant HR0011-16-C-0025





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