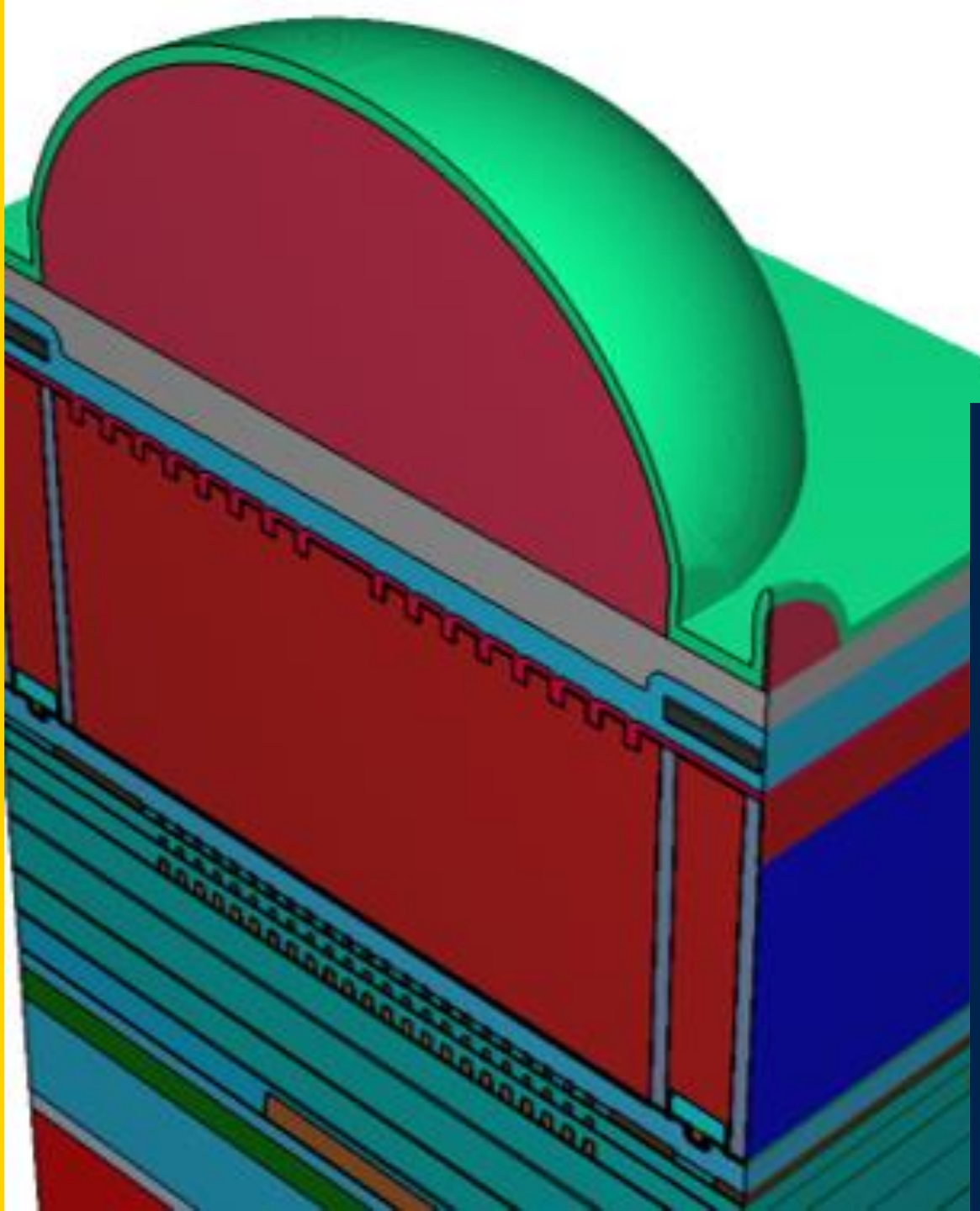

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A low power, high dynamic range SPAD for sustainable sensing

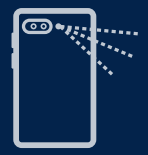
Sara Pellegrini and Bruce Rae

International SPAD Sensor Workshop

13th June 2022

Optical sensing solutions application domains

Personal Electronics



Camera assist

AR / VR

Industrial & Robotics

Obstacle detection

Machine vision

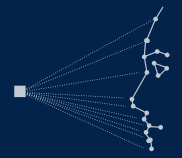
Automotive

In-cabin monitoring

LiDAR

Computer & Peripherals

Presence detection



Security

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ST pioneer and leader in Time-of-Flight (ToF)

ST is #1 Worldwide ToF sensor supplier

ToF Pixel Expertise SPAD/FPD	**Advanced Photonics** **CMOS Process** (40nm/3D)	**Embedded ToF Processing & Depth ISP**
Micro-Optics & Supply Chain	**Illumination Expertise** & Supply-chain	**Advanced Packaging know-how** & manufacturing

4 Generations
of all-in-one ToF solution deployed in the past 5 years

>170 phones with FlightSense™
Above 15 smartphone OEMs

>Hundreds other customers
Hundreds non wireless end-products in the market

>45,000
Evaluation kits deployed

>1Bu
ToF units shipped. Mastering end-to-end supply chain

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Unlimited Applications


Lighting


Laptops


Printers


Tablets

Smart home


Cleaning robots


Service Robots


Drones


Toys

ATM

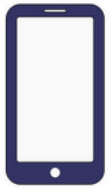

Projectors


AR/VR


Faucets


Public Parking


Lockers


Phones


Wearable & IoT


Dispensers


White Goods

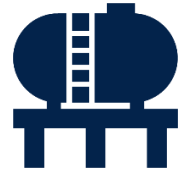

Medical


Farming


Logistics


Trucks


Warehouse


Tanks


Vending machines

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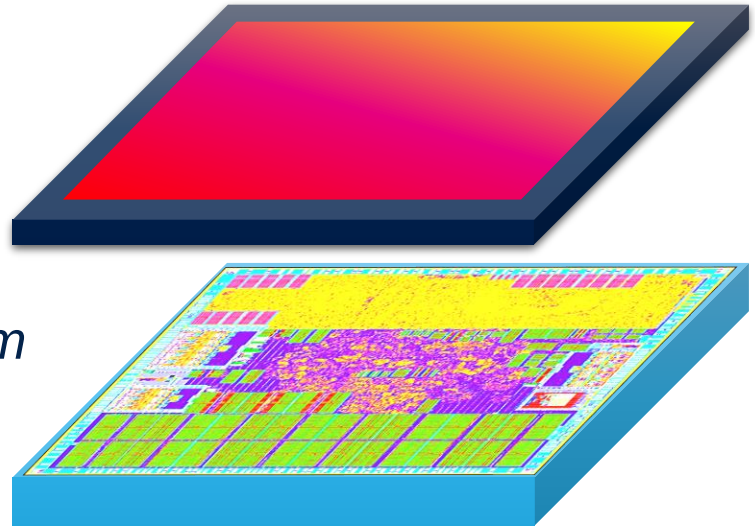
Wafer stacked CMOS image sensor

Pixel Array

Top tier

Bottom tier



Pixel custom technology

- ► Optimised breakdown voltage
- ► Low DCR and high PDE in the near IR
- ► High dynamic range

Innovative pixel-level top to bottom connection

Low power processing

Integrating both low noise analogue and high speed, low power, digital logic

Advanced digital & analog CMOS

- ► High density & low power digital for efficient TDC
- ► Pixel-wide quench circuit implementation

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IMG140B-TOP technology | features

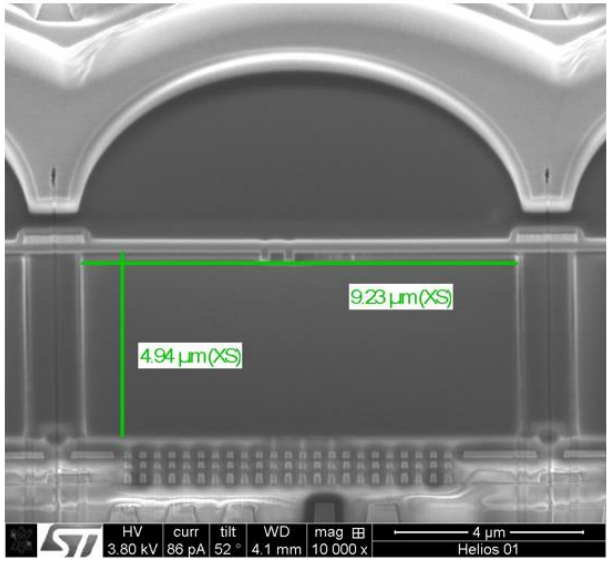
FEATURES

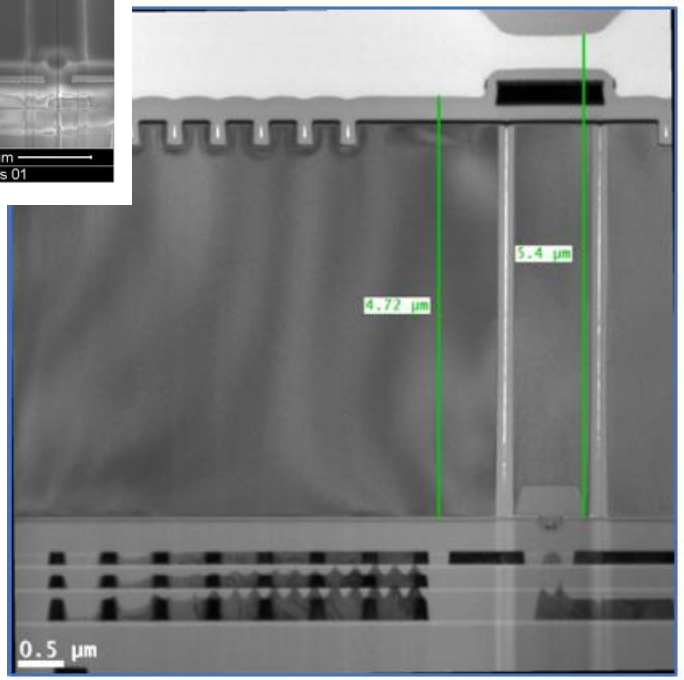
TOP tier process

- SPAD photodiode
- 4.5 µm epitaxy for SPAD
- DTI for optical and electrical isolation
- Quench Resistor
- BSI Tungsten for shielding
- Microlens
- Structuration for QE enhancement

BOTTOM tier process

- 40nm CMOS
- Low power
- Dual gate oxide
- 7 metals levels
- Aligned with C40SPAD to allow IP reuse





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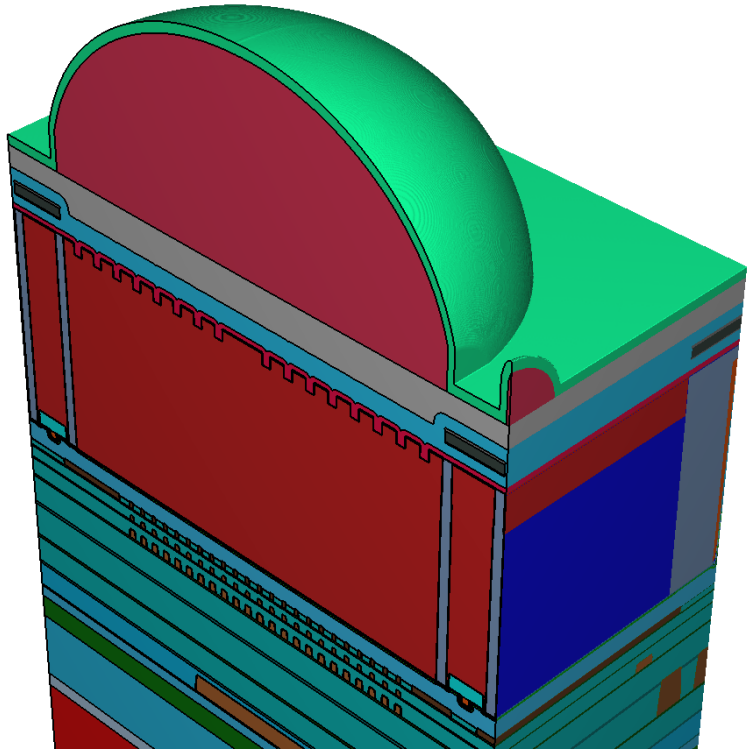
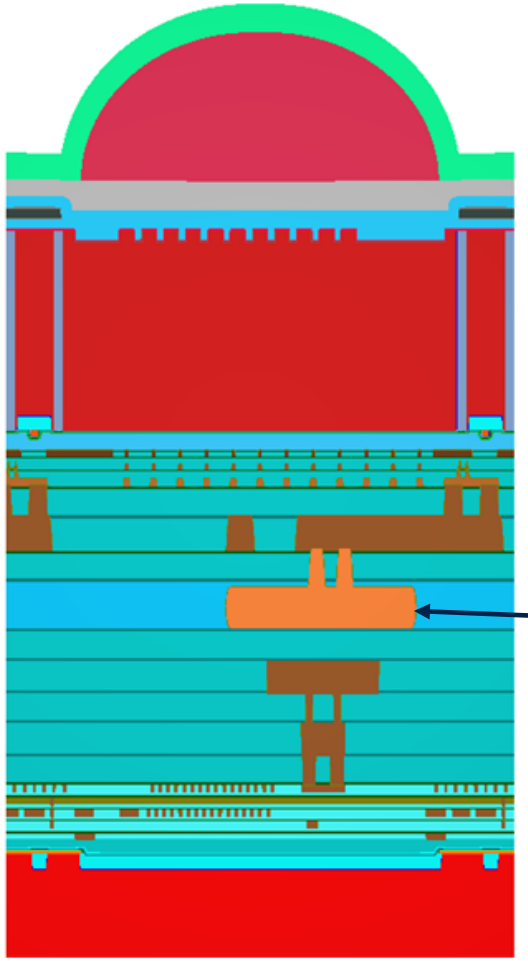
The best of two worlds wafer stacked sensor

SPAD dedicated technology

- Bottom tier quench circuit for high FF
- Large collecting volume to maximise PDE





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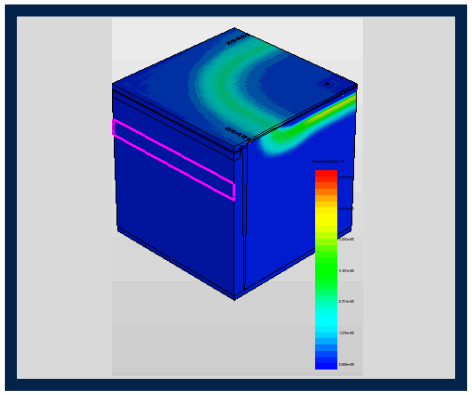
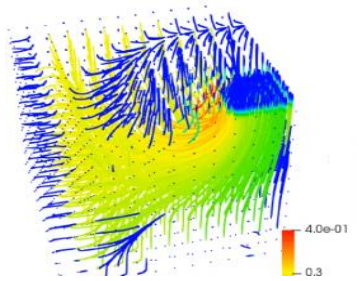
Electro-optical simulations

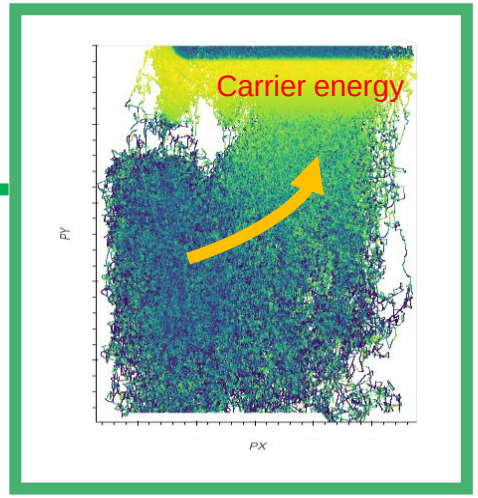
TCAD: Process/ Device simulations



Monte Carlo

McIntyre

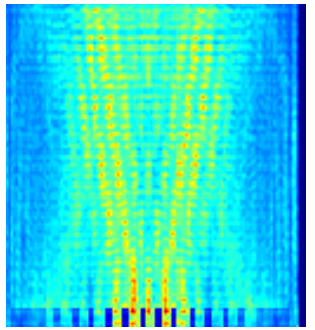




Breakdown Probability

Optical Absorption

3D Finite-Difference Time Domain simulations



Photon detection probability

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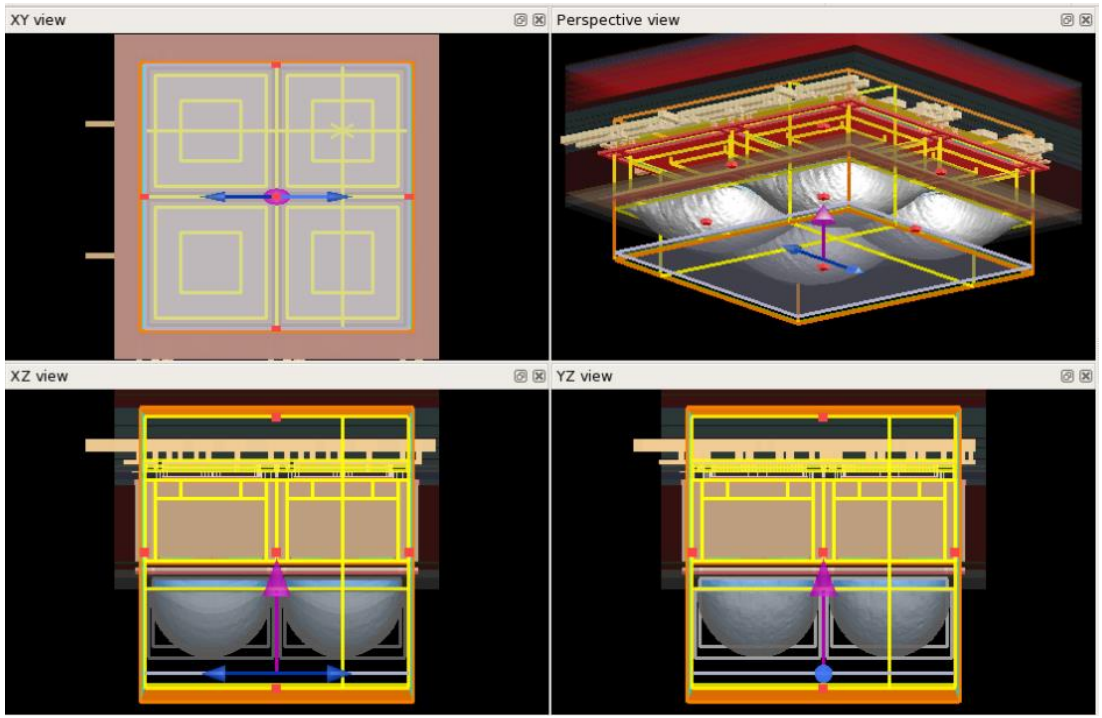
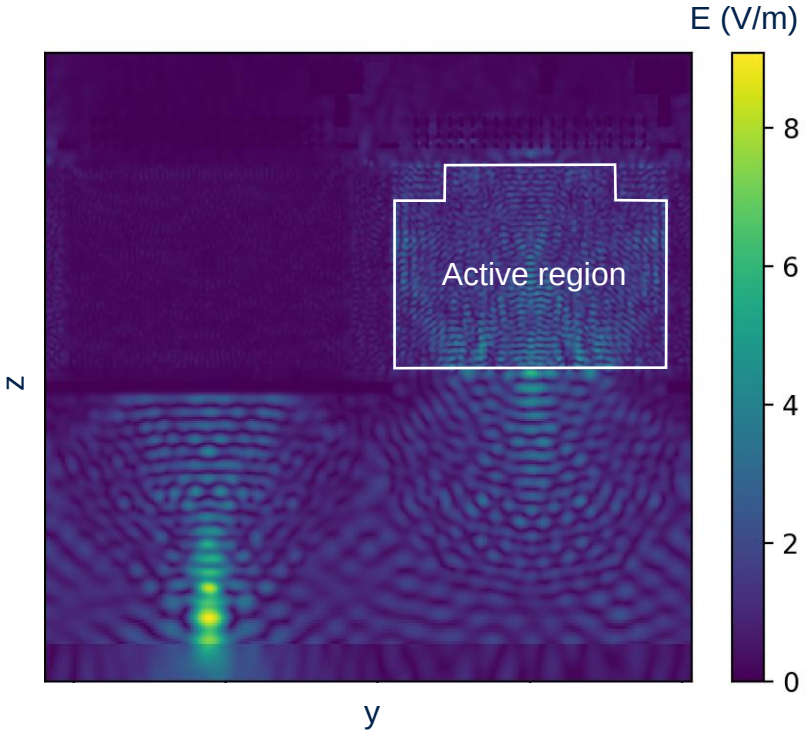
Optical simulations: methodology

3D model of SPAD pixels:



Use 3D electromagnetic FDTD algorithm to solve Maxwell equations (Lumerical software)

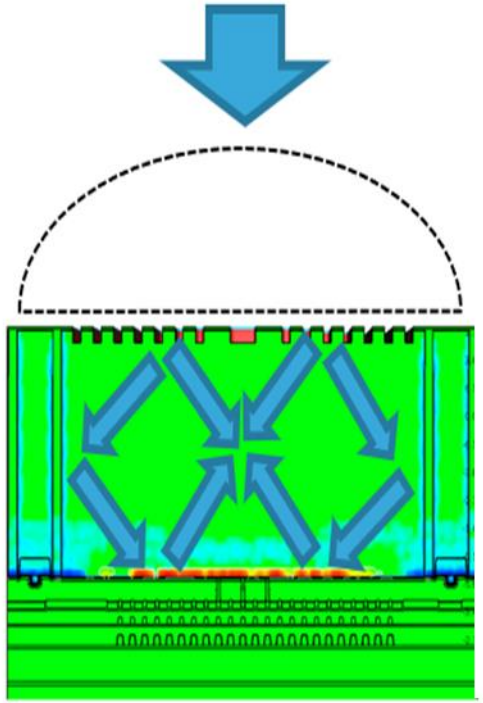
Electromagnetic fields inside pixel

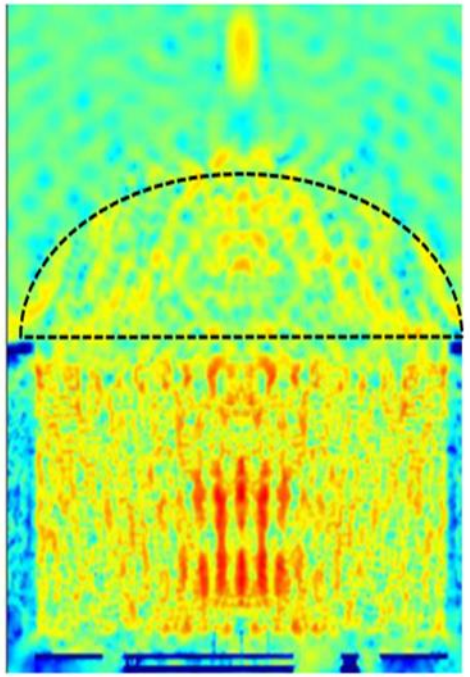


Extract optical absorption and crosstalk

Structuration design and simulation

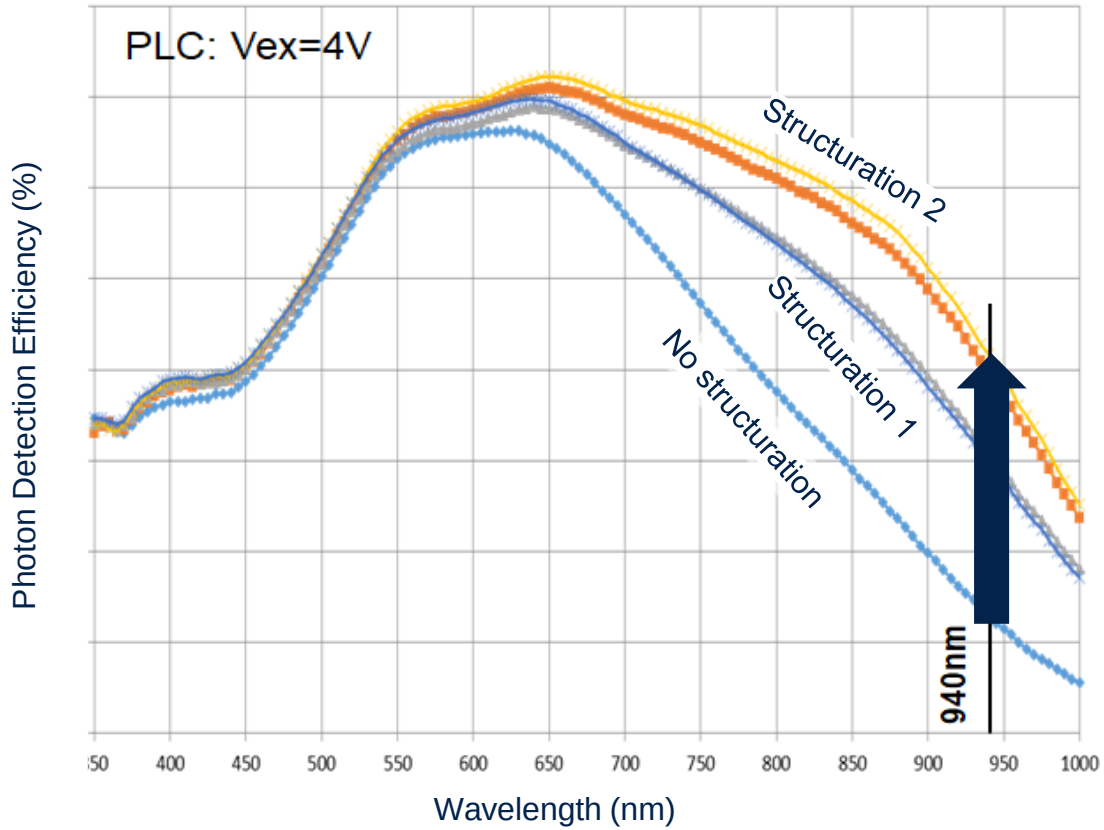
3D architecture with structuration: multiple reflections
➔ path length x N (with N>>2)





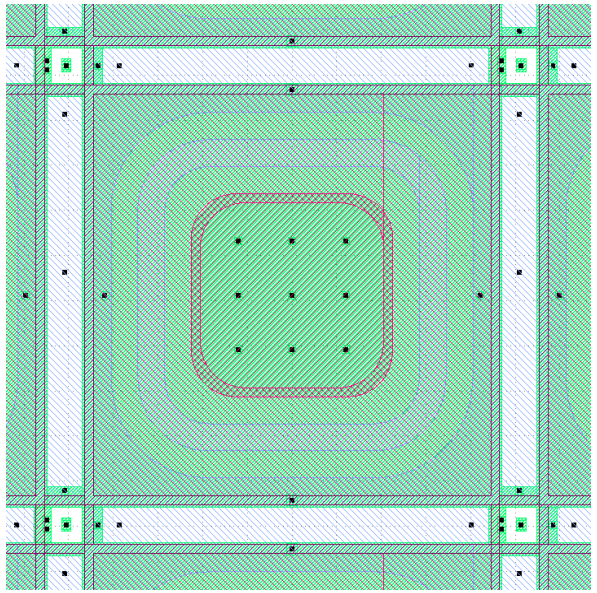
Structuration impact

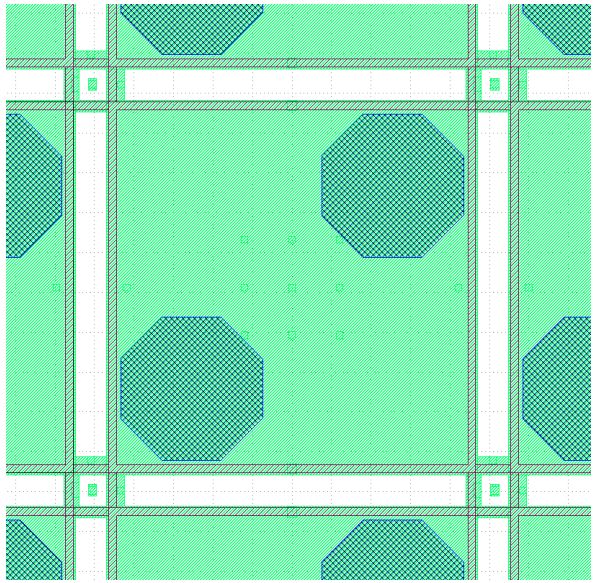
3D architecture with structuration: multiple reflections
➔ Photon detection efficiency improvement

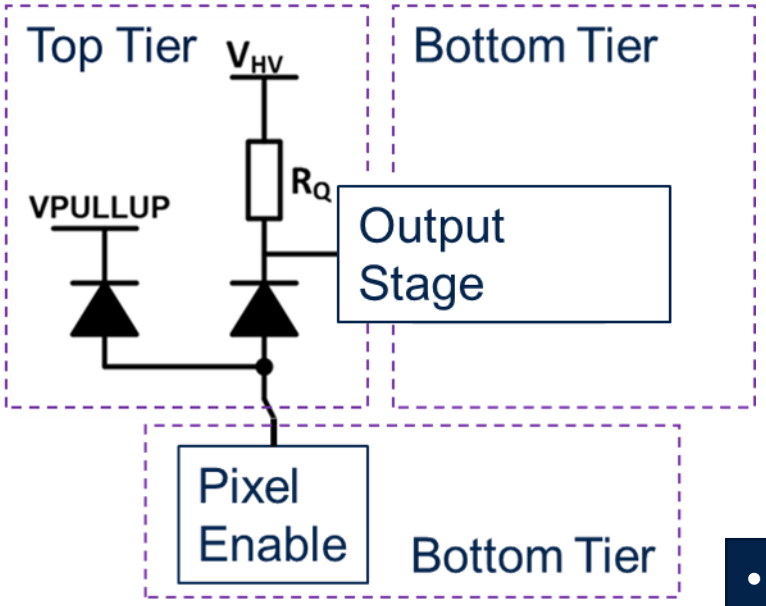


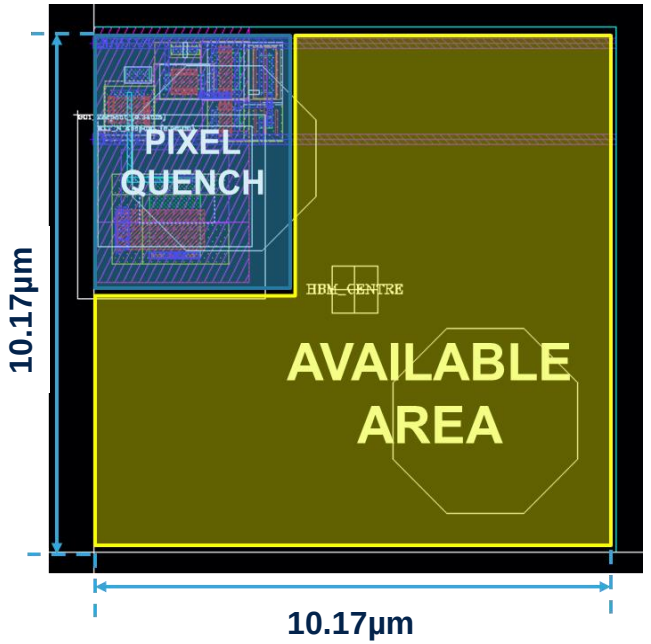
~3x increase in PDE

3D40SPAD - Pixel









- Pixel quench circuit occupies <25% of available area in bottom tier
- GO1 compatible pixel output voltage
- Positive Vbd compatible with efficient on-chip charge pumping

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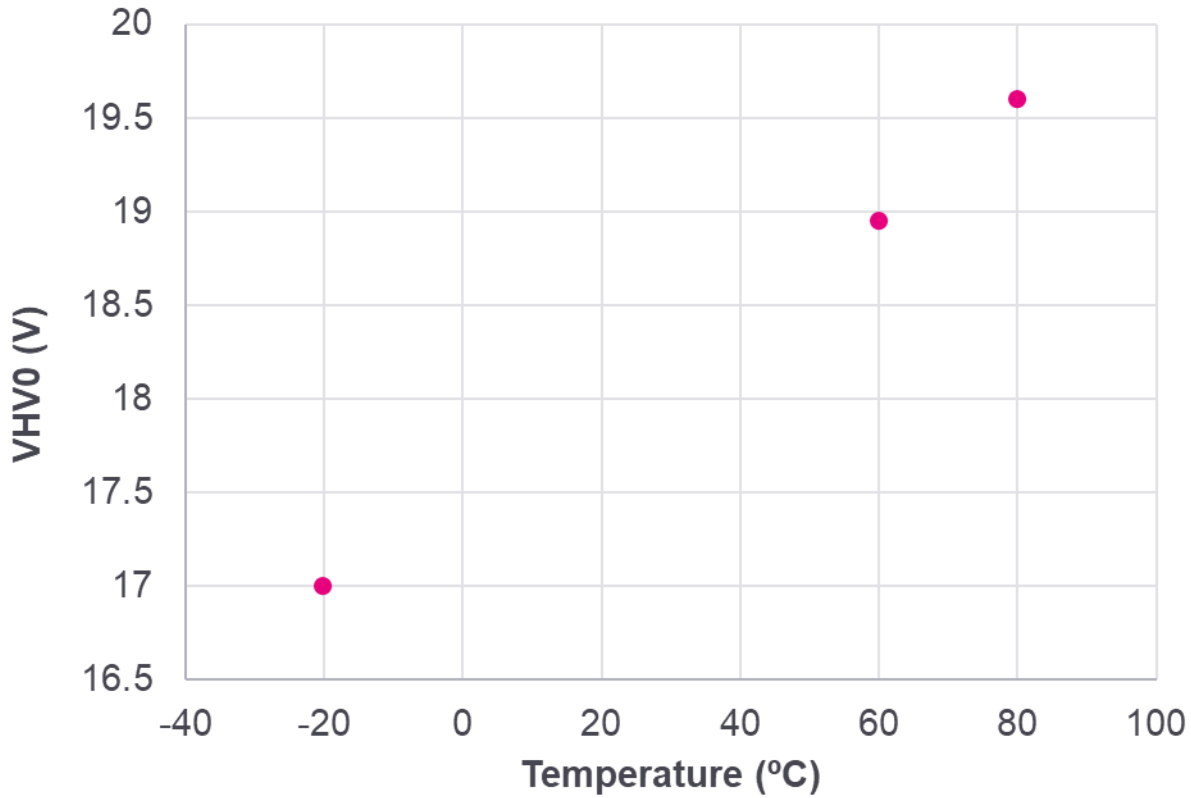
Breakdown Voltage vs Temperature

Diode junction engineered to minimise Vbd ➔ minimal power consumption

VHV0			
Temp [°C]	-20	60	80
VHV0 [V]	**17.0**	**18.9**	**19.6**

VHV0 is the minimum voltage for which the SPAD pixel produces an output
VHV0 = Vbd + Vout_thresh



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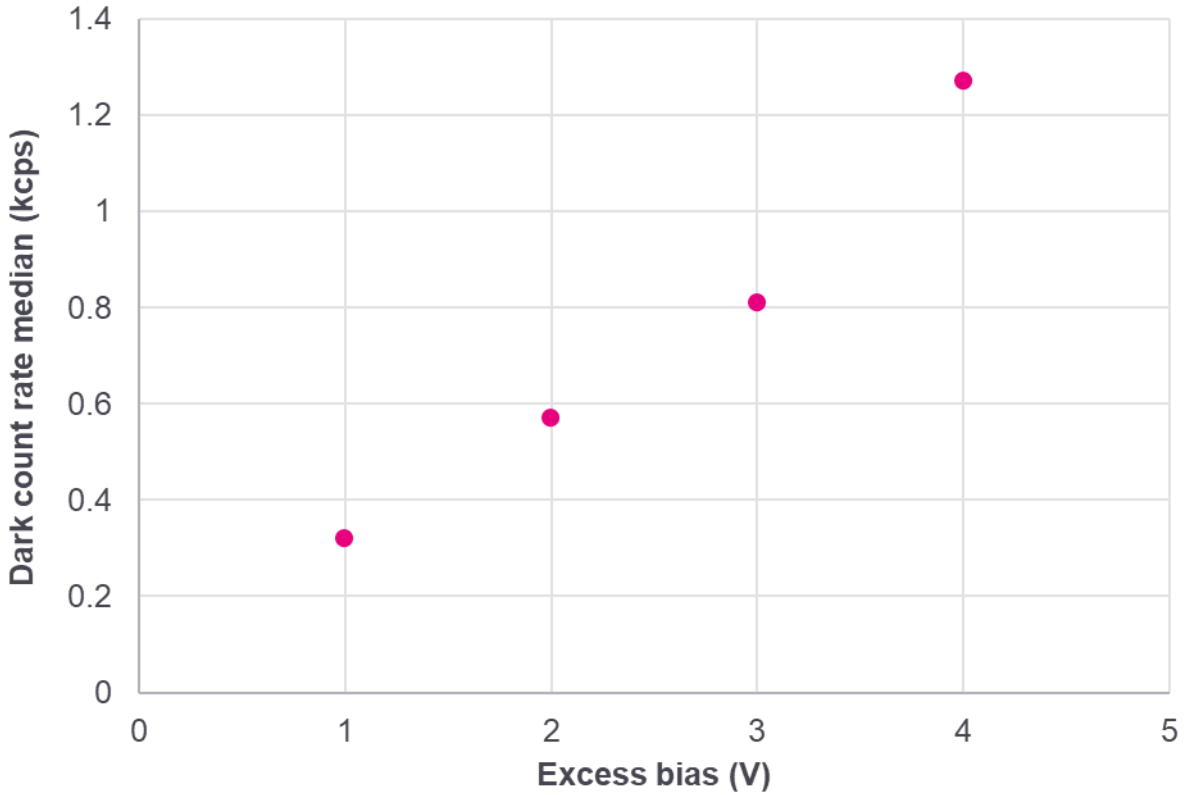
Dark count rate @ 60°C

Dark count rate				
Vexcess [V]	1	2	3	4
DCR Med [kcps]	**0.32**	**0.57**	**0.81**	**1.27**



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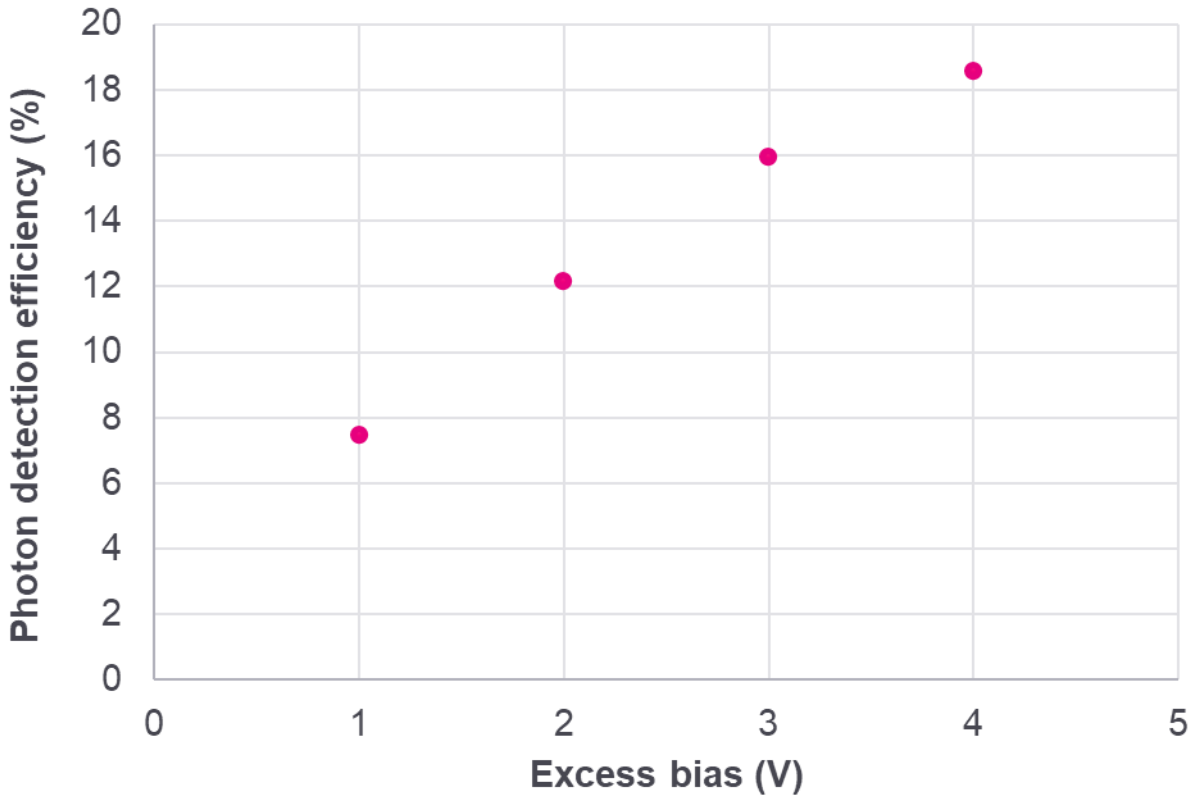
Photon detection efficiency @ 60°C



Photon Detection Efficiency				
Vexcess [V]	1	2	3	4
PDE Median [%]	**7.5**	**12.1**	**15.9**	**18.6**

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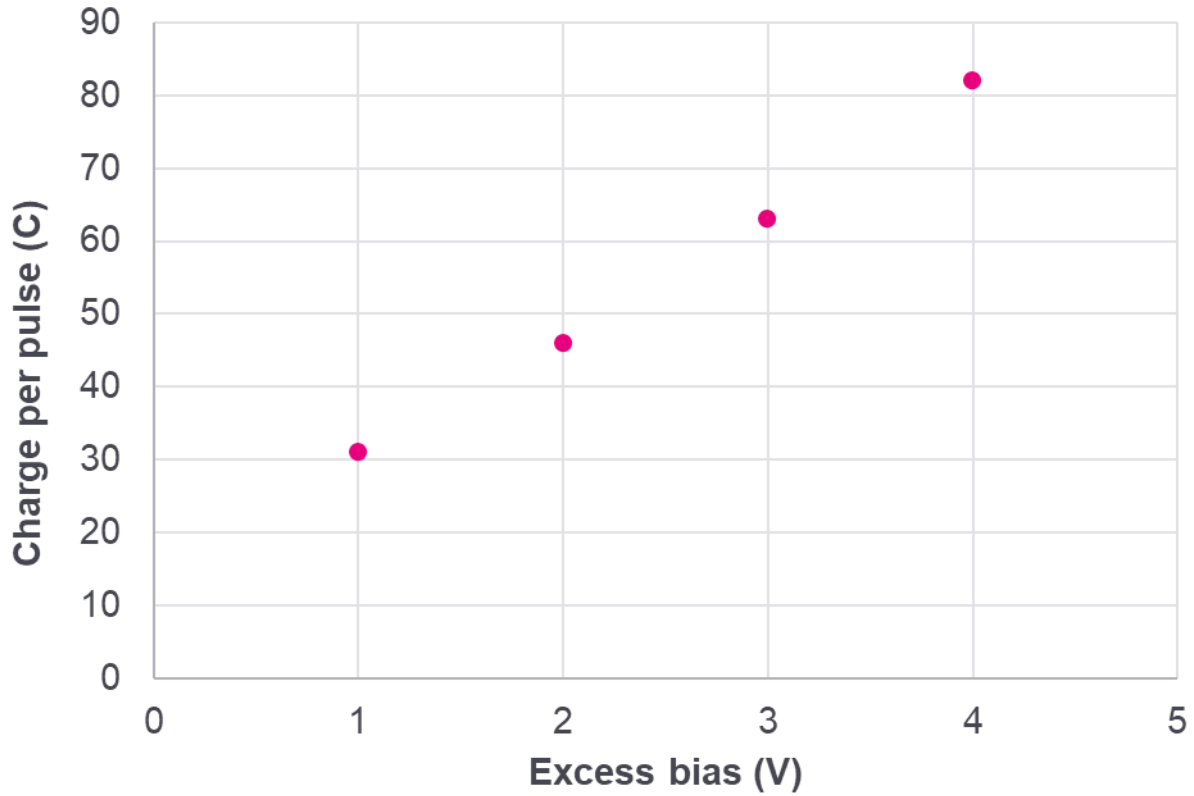
Charge per pulse vs V excess (@ 60°C)

Low charge per pulse @ low VHV enables high resolution array and/or low array power consumption
➔ In-line with ST sustainability strategy



Charge per pulse				
Vexcess [V]	1	2	3	4
Charge per pulse [fC]	**31**	**46**	**63**	**82**

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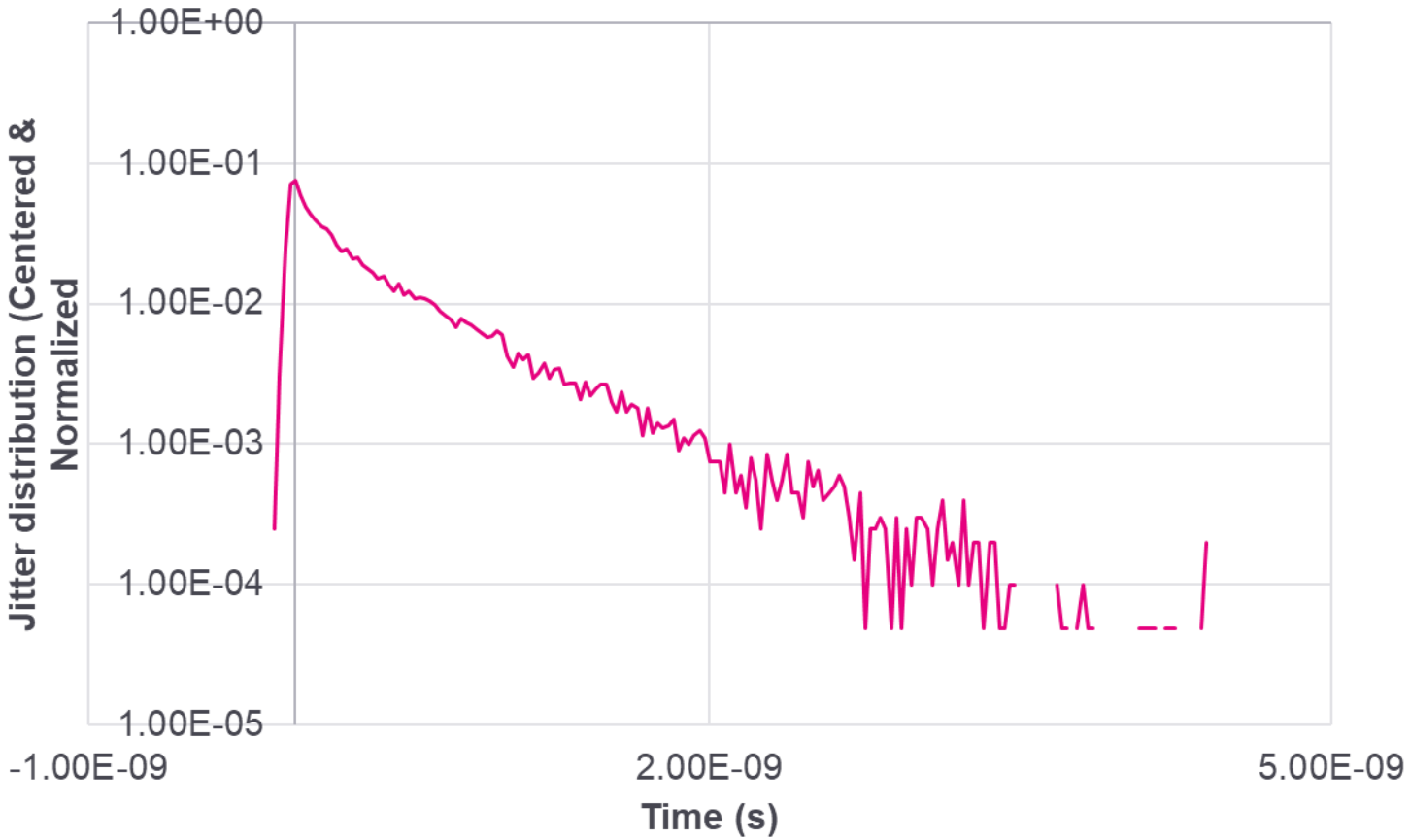
Timing jitter @ 60°C



Timing Jitter	
Vexcess [V]	3
FWHM [ps]	**169**
Pop < 90% [ns]	**1.3**

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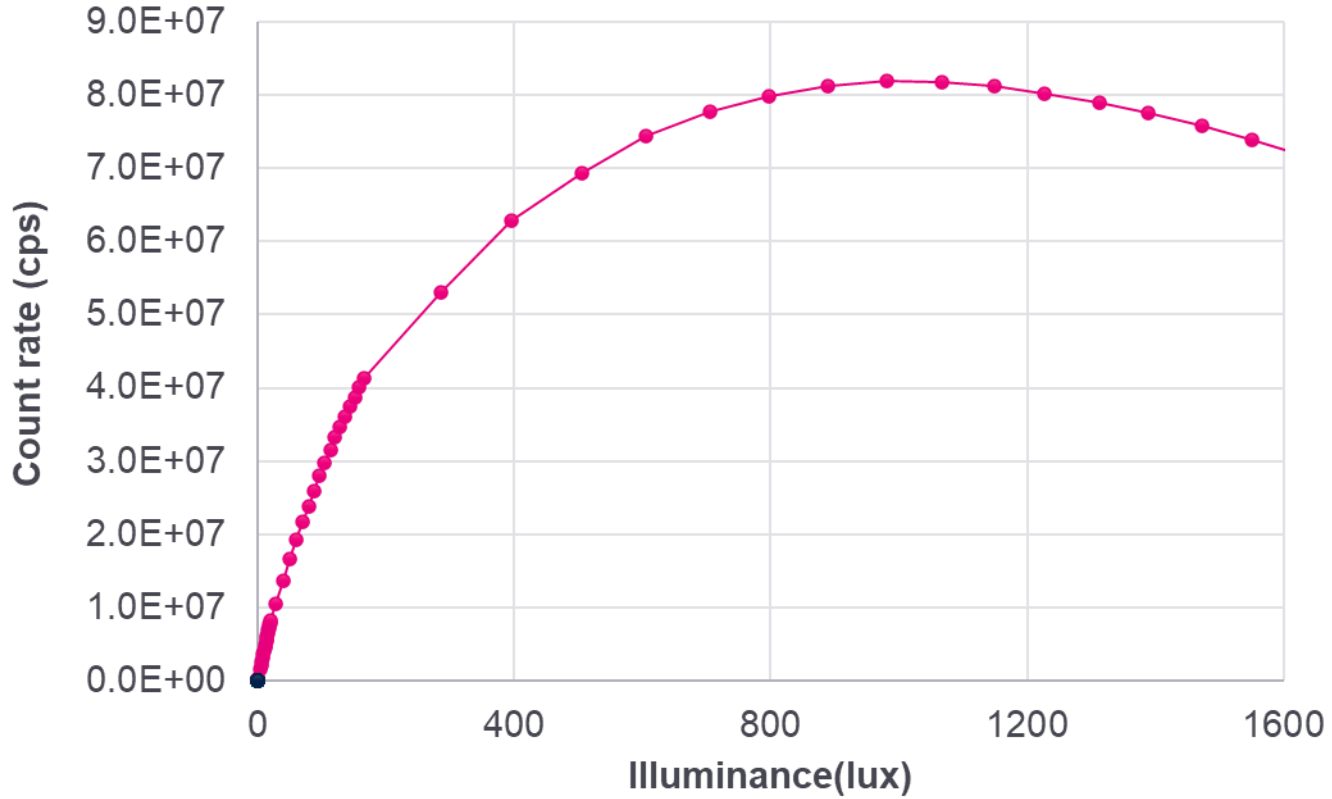
Dynamic range @ 60°C

High QE diode requires high dynamic range pixel ➔ maximise system benefit



Dead Time / Max Count Rate	
Vexcess [V]	3
Max Count Rate [Mcps]	**82**
Dead Time – 1/MCR [ns]	**12.2**
Dead Time – 1/(e*MCR) [ns]	**4.5**

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Access to our advanced imaging technologies through foundry model

ST Imaging manufacturing & engineering know-how

Billions imaging devices shipped

World-class 12” wafer fabs

Recognized expertise across Imaging value chain & ecosystem

Premium services beyond traditional foundries

Access to differentiating technologies

Reliable partner, flexible business model

Benefit from broad imaging IP portfolio and expertise

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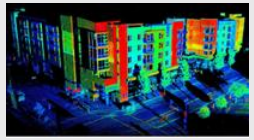
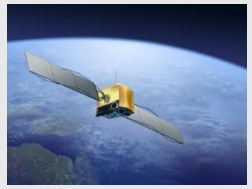
Where to find us

LiDAR

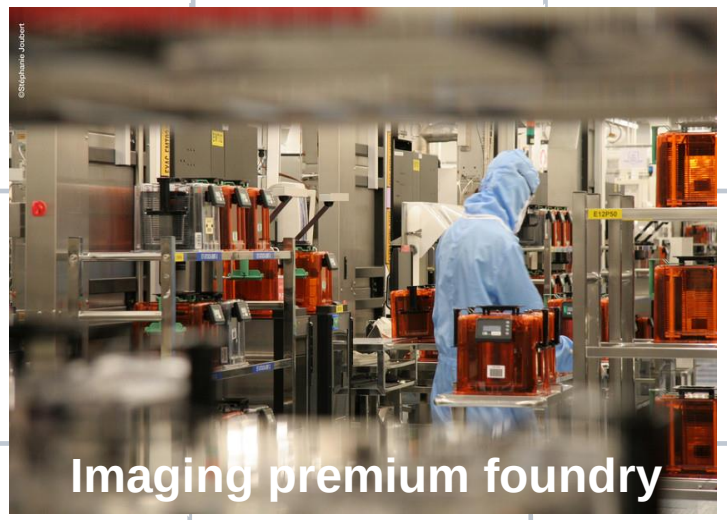


ROIC & Thermal IR

Space & Defence



Machine Vision



Cinematography

DSLR

X-Ray

Medical

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We are creators and makers of technology

One of the world's largest semiconductor companies

48,000 employees of which **8,400** in R&D

$12.8 B revenues in 2021

Over **80** sales & marketing offices serving over **200,000** customers across the globe

13 manufacturing sites

Signatory of the United Nations Global Compact (UNGC)
Member of the Responsible Business Alliance (RBA)

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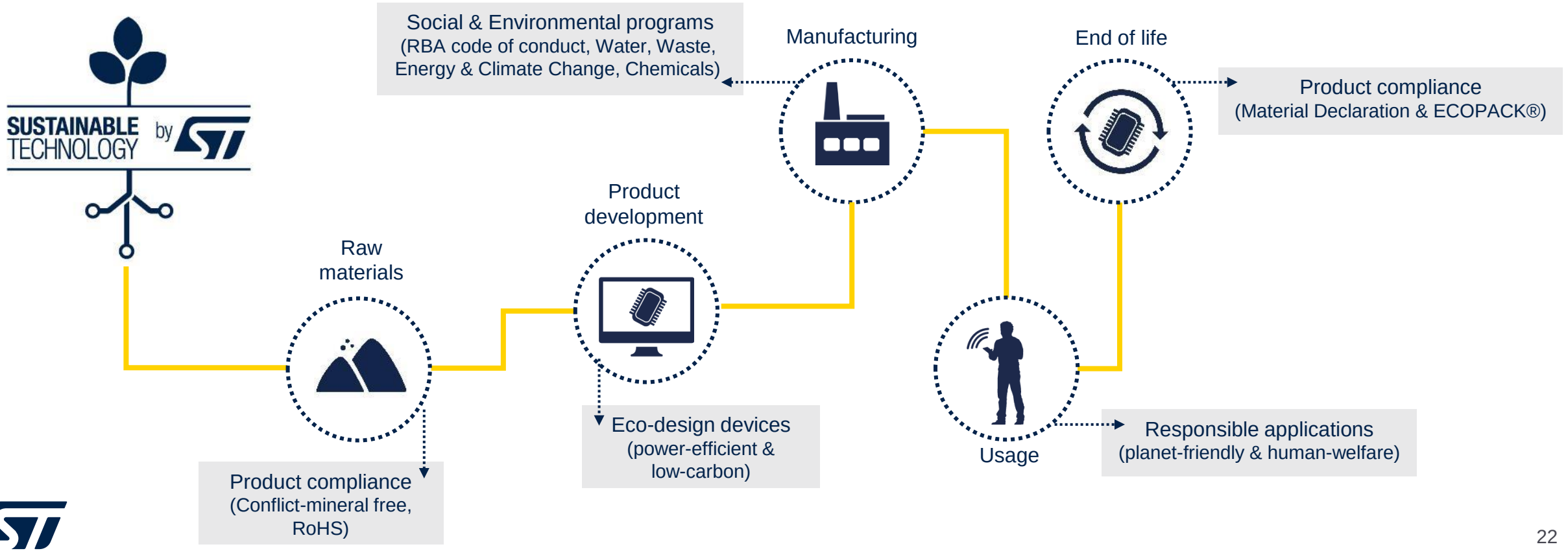
As of December 31, 2021

Sustainable technology

Our Sustainable Technology program aims to develop responsible products which:
- **improve our social and environmental footprint at every stage of the product life**
- **have the greatest positive impact on the planet and people in the end-application**



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We will be carbon neutral by our 40th anniversary

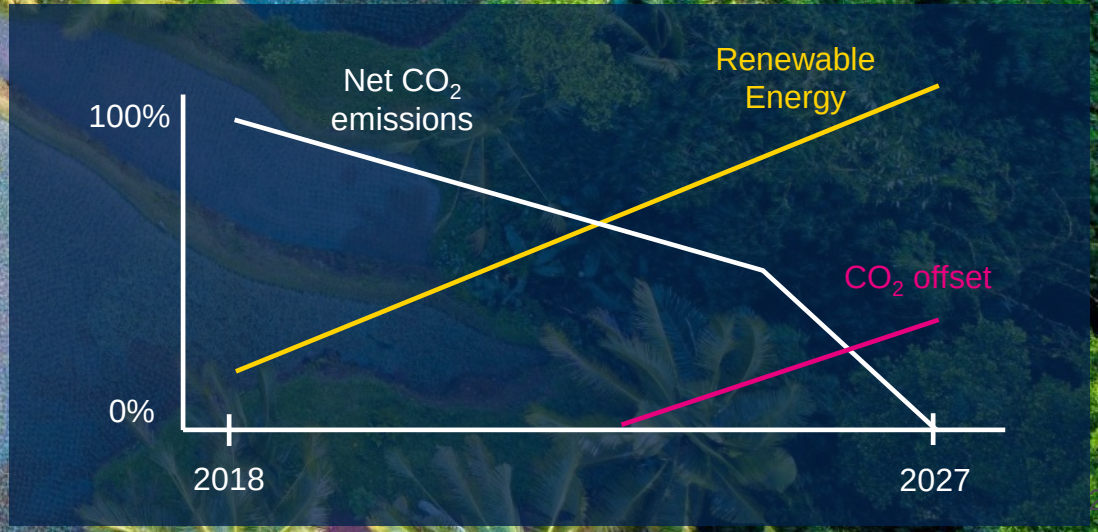
Milestones

- Compliance with the 1.5°C scenario by 2025 – recognized by SBTi
- Carbon neutral by 2027
- Sourcing 100% renewable energy by 2027

- Collaborative programs and partnerships for carbon neutrality throughout our ecosystems

SCIENCE BASED TARGETS
DRIVING AMBITIOUS CORPORATE CLIMATE ACTION

CARBON NEUTRAL



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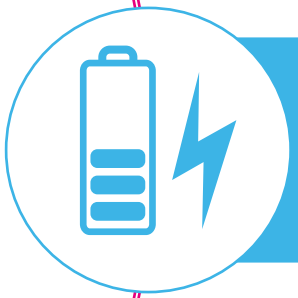
Take aways

Optimised diode breakdown voltage



Low charge per pulse

High dynamic range taking full advantage of high PDE diode

Acknowledgements

Imaging Division team in Edinburgh (UK) and Technology R&D team in Crolles (France) at STMicroelectronics

Silicon Imager Laboratory at CEA LETI

This work was funded by the Electronic Components and Systems for European Leadership Joint Undertaking (ECSEL JU) in collaboration with the European Union's H2020 Framework Programme under grant agreement No 826600.

Thank you!

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