CMOS SPAD-Based LiDAR Sensors with Zoom Histogramming TDC Architectures

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Abstract As self-driving cars and mobile metaverse devices have been developed intensively, LiDAR sensors have emerged because they can offer precise depth images in real-time. They employ mainly two technologies; direct time-of-flight (dToF) techniques based on single-photon avalanche diodes (SPAD) support long-range detection and high background resilience, while indirect ToF (iToF) counterparts provide high spatial resolution and low depth noise without a complicated time-to-digital converter (TDC). In this paper, we present flash LiDAR sensors with three zoom histogramming TDCs (hTDC) combining both dToF and iToF techniques for utilizing their advantages simultaneously. Binary and quaternary searching algorithms are introduced to minimize memory size in the hTDC, and analog counters are employed to realize an area- and energy-efficient LiDAR sensor. The overall architecture, detailed circuit implementation, and measurement results are shown clearly.

Keywords: LiDAR sensor, histogramming TDC, successive approximation, quaternary searching, analog counter

1. On-chip Histogramming TDC Architecture

Data rates of LiDAR sensors are much larger than those of color image sensors with the same spatial resolution and frame rate because ToF values from the whole array in every laser emission of a few μs should be recorded. An on-chip digital signal processor (DSP) or hTDCs have been integrated into LiDAR sensors to compress ToF data and directly estimate depth information [1-4]. However, a large number of memories corresponding to the number of time bins are also burdensome to integrate hTDCs into pixels in flash LiDAR sensors. To address this issue, two-step hTDCs have been reported [5-8]. In this paper, three hTDC architectures inspired by the SAR ADC are presented.

2. Successive Approximation (SA) hTDC

The SA hTDC decides one bit of the ToF value at each step in the binary search manner [6]. The entire time bin is divided into two, up and down bins, and the numbers of SPAD pulses generated in both bins are compared with each other. A winning bin in the comparison is selected as the next time period to be searched. This process is recursively conducted until all ToF values are determined. A single up-down counter is required, minimizing the memory size. The iToF technique is also incorporated to improve the depth resolution.

3. Quaternary Searching hTDC

The proposed SA hTDC has been successfully integrated into each pixel with a single up-down counter at the expense of a long conversion time. Moreover, it suffers from background light especially in the first step because the first period is half of the whole duration, which is quite long. To overcome these issues, we propose the quaternary search hTDC dividing the bins by four in each step, doubling the frame rate [7]. Since the time bin width is reduced by half, the signal-to-background ratio is also enhanced by a factor of two and exponentially improved in consecutive steps. The four-phase iToF calculation can ignore background light in the fine TDC operation as well. Fabricated in a 110-nm BSI, 30-fps 80×60 depth images can be obtained under a 30-klux background light condition.

4. SA hTDC with Analog Counters

Our both hTDCs consist of digital up-down counters that consume large power with high-speed clock frequencies over 300 MHz. The power dissipation is proportional to the intensity of background light, which is unsuitable for low-power LiDAR sensors. We devise analog counters to replace the digital counterparts for an area- and energy-efficient SA hTDC architecture [8]. In addition, each pixel creates its own ramp signal by using the same analog counter, compensating for its PVT variation. Compared with the digital counter, the proposed analog counter consumes 3300× lower power and occupies 16× smaller area, realizing a dToF sensor with 100×80 pixel array fabricated in a 110-nm BSI process.

References

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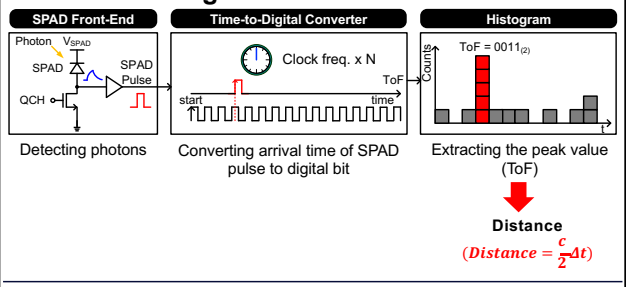
Block Diagram of SPAD dToF Sensor



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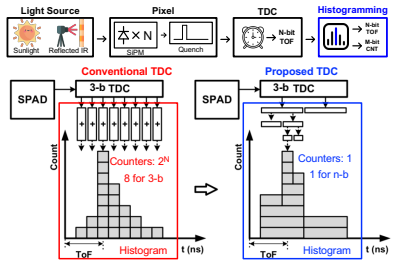
SA hTDC Architecture



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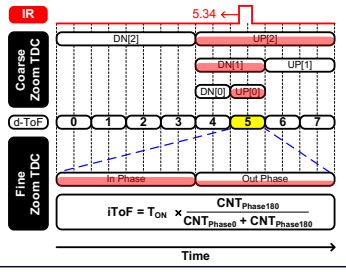
Two-Step Zoom hTDC



SAR coarse TDC

+

iToF fine TDC

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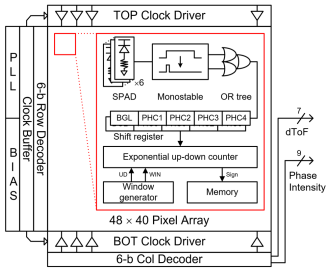
Overall Architecture



- In-pixel zoom histogramming TDC
  - dToF coarse TDC
  - iToF fine phase domain TDC for zoomed-in ToF value
- Exponential counter for binary search with fast operating speed
- Window generator for managing time bins

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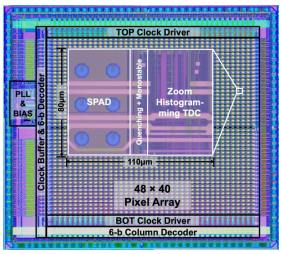
Chip Photograph



Process	110nm CIS CMOS
Pixel Array	48 x 40
Pixel Size	110 x 80 μm²
PWR Consumption	840 mW
Chip Size	5900 x 5240 μm²
ZH-TDC	4000 μm²
TDC Depth	Coarse 7-b / Fine 6-b
TDC resolution	Coarse 5 ns / Fine 90 ps

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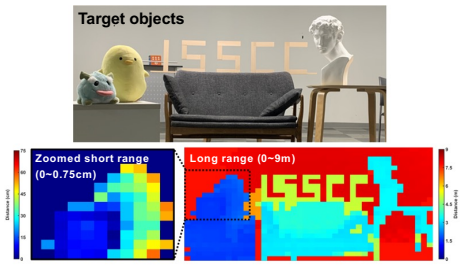
Depth Image



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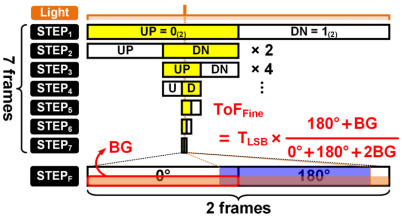
Issues in Zoom hTDC Architecture



- Synthesis of 9 sub-frames: low frame rate, motion artifact
- Low signal to background ratio (SBR)
- Slow SBR improvement
- Phase detection error by background light
  → Need to have another background sub-frame

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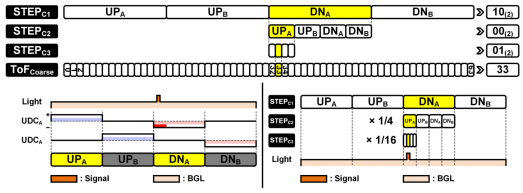
Quaternary Search hTDC



- The whole range is divided by four.
- Even and odd bins are compared to determine ToF[MSB].
- Both counters are compared to determine ToF[MSB-1].

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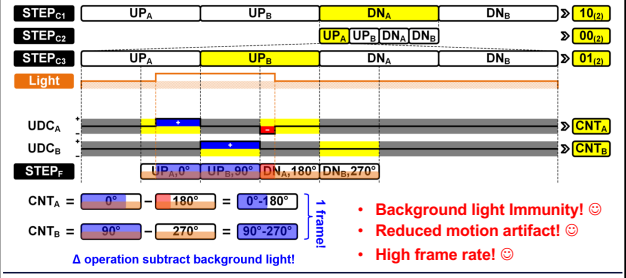
Time-Gated Δ-Intensity Phase Detection



- **Background light Immunity!** ☺
- **Reduced motion artifact!** ☺
- **High frame rate!** ☺

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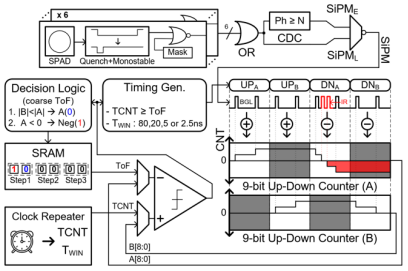
Pixel Architecture



- 6 SPADs w/ AFE & masking mem.
- Coincidence detection circuit
- Two 9-b UDC for quaternary search
- Timing generator for time bin management
- Clock repeater shared by four neighbor pixels

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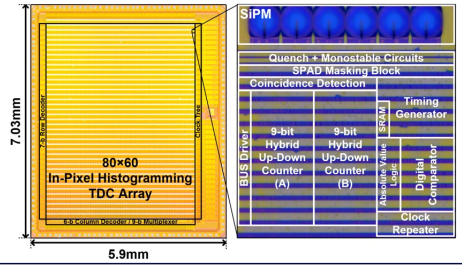
Fabricated Prototype



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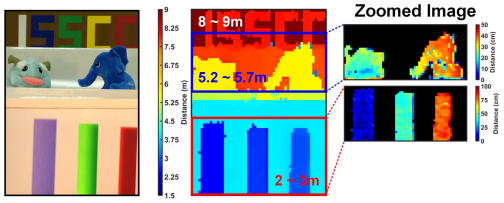
Depth Image in a Short Range



Captured in 30fps w/ 30klux background light

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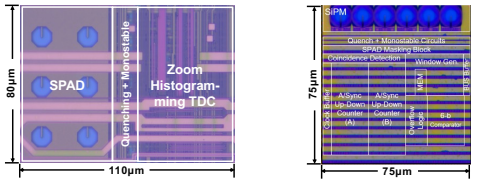
Other Issues in Previous hTDCs



Large pixel size
Large power consumption
⇩
Limited spatial resolution! ☹

⇨ Solution: Analog counter replacing area- and power-hungry digital counter

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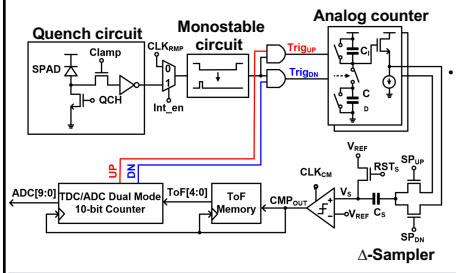
Zoom hTDC Architecture w/ Analog Counter



- TDC/ADC Dual Mode 10-bit Counter
  - TDC Mode: Timing Generator
  - ADC Mode: 10-bit Counter

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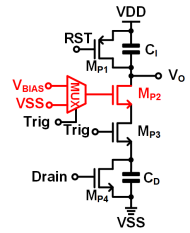
Proposed Analog Counter

Proposed charge injecting AC



- High linearity ☺
  - Output independent ΔVo
  - Use the cascode stage of M_{P2} without the op-amp
- Small area ☺
- Low power consumption ☺
- Step-tunability ☺
- Low leakage on output node ☺

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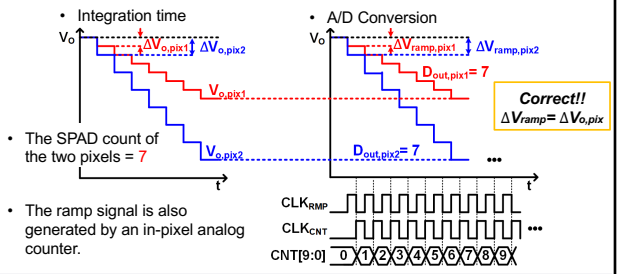
Self-Calibrated A/D Conversion

- Integration time
- A/D Conversion
- The SPAD count of the two pixels = 7
- The ramp signal is also generated by an in-pixel analog counter.



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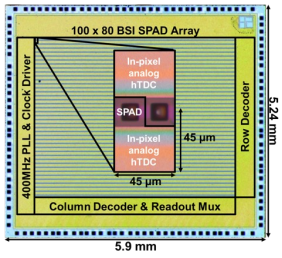
Chip Micrograph



Process	110nm BSI
Pixel array	100×80
Pixel pitch	45 μm
Chip power	Digital: 477 mW Analog: 50 mW
Chip size	5.9×5.2 mm^2
TDC Type	In-pixel SA analog hTDC
TDC area	1038 μm^2
Histogram area	72 μm^2

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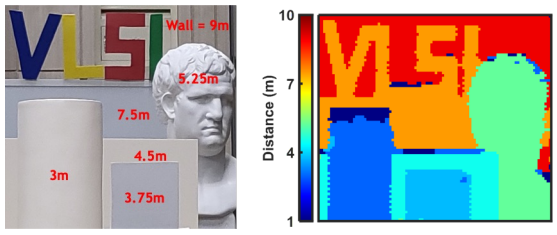
Indoor Depth Image



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