The most energy-efficient image sensor architecture: case study for automotive and time-of-flight sensors

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Abstract This paper presents the most energy-efficient image sensor architecture for different applications. As a case study, two applications of automotive image sensors and indirect time-of-flight (ToF) image sensors are investigated. From the measurement and simulation results, automotive image sensors for autonomous driving applications will be more efficient when the image signal processor (ISP) is implemented on the host side. To the contrary, ToF image sensors show significantly better energy-efficiency with hardware depth ISP on the sensor side, compared to the off-chip software depth ISP.

Keywords: CMOS image sensor, sensor architecture, automotive sensor, time-of-flight

1. Introduction

CMOS image sensors (CIS) with the active pixel sensor (APS) technology have been considerably developed for the past 20 years, especially for pixel pitch and pixel count. Starting from 0.3 mega-pixels with 5.6-μm pitch, recent CIS have 200 mega-pixel CIS with 0.56-μm, as shown in Fig. 1.

The leading market for CIS industry has been mobile color image sensors, which are mounted on the smartphones for photo taking and video recording. However, by the aid of prolific property and functionality such as infrared (IR) sensing, depth sensing, and higher dynamic range (DR), the applications of CIS are expanded to other applications such as automotive, surveillance, and AR/VR.

The number of cameras in a system tends to increase. In case of mobile phones, more cameras in the back and front side are adopted to satisfy various photo-taking experience. For example, Galaxy S22 Ultra have totally five cameras: four for rear-facing and one for front-facing camera [2]. For vehicles supporting advanced driver assistance system (ADAS) and autonomous driving (AD), more cameras are required according to the level of vehicle autonomy. At least eight cameras are included for level-3, and 11 cameras or more will be needed for level-5 [3].

For the depth cameras based on time-of-flight (ToF) sensors, totally different type of back-end processing is needed, due to the difference between depth processing and color processing. Therefore, increased number of cameras and a new image processing would add substantial burden on the whole imaging system.

In this paper, we will evaluate power, performance, and cost for different image sensor systems, to find out the most optimal and efficient sensor architecture. The best sensor architecture will depend on different applications. Hence, we select two examples for a case study: automotive and ToF camera systems.

2. Image sensor system overview

Fig. 2 shows a typical imaging system architecture. The system is composed of a lens and three electrical parts: sensor core, image signal processor (ISP) and central processing unit (CPU). Sensor core generates raw image, which could be raw Bayer image of color image sensors, unprocessed IR image of IR sensors, or raw phase data of ToF sensors. The raw image can be obtained by converting incoming light signal into electrical signal by pixel array, and then converting analog signal of pixel to digital codes. Some front-end signal processing may be performed in the raw image domain such as dark level compensation and defect pixel identification. In the ISP, raw image data are processed by a series of functional blocks. The necessary processing blocks will be different from purposes of the sensors. In Fig. 2, the sub-blocks in the ISP are categorized into three generic functions: pre-processing, image enhancement and calibration/correction (the order of the blocks can be switched). The pre-processing would be defect correction, DR merger and color interpolation for color processing, whereas it would include tap shuffling and depth calculation for depth processing. The image enhancement block may include noise reduction, luminance/chrominance correction in the color domain, and depth noise reduction and depth unfolding in the depth domain, to name a few. Calibration and

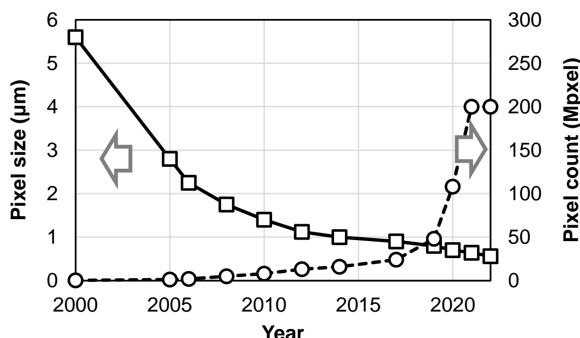

Fig. 1. Evolution of CMOS image sensor (redrawn from [1]).

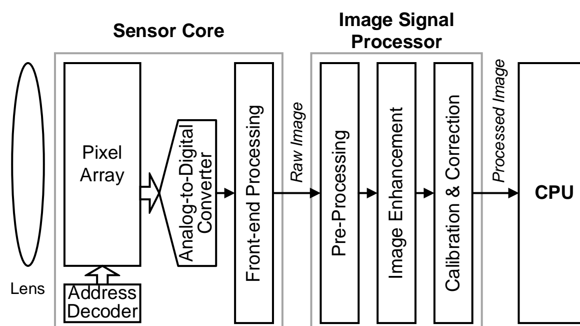

Fig. 2. Typical imaging system architecture.

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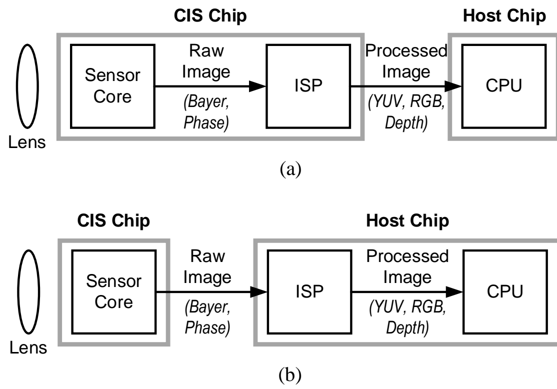

Fig. 3. Two typical image sensor architectures: (a) with an on-chip ISP and (b) with an off-chip ISP.

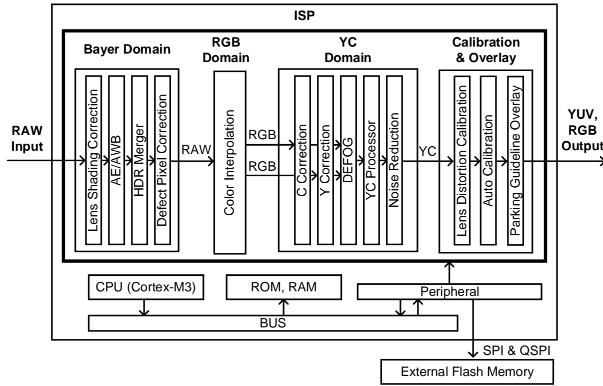

Fig. 4. Example of the ISP architecture for automotive CIS.

correction are lens distortion correction, distance calibration and so on. After the input raw image goes through all ISP blocks, the processed image will be outputted to CPU.

Usually, two of the above three components are integrated together on the same chip die, to form a type of system-on-chip (SoC). As shown in Fig. 3, there could be two types of SoC. Fig. 3(a) shows a CIS SoC, where sensor core and ISP are merged together. ISP can be merged with CPU into a host chip as shown in Fig. 3(b). There are pros and cons for each type of architecture. The most optimized architecture should be selected for the specific system requirements of each application.

3. Case study

A. Automotive image sensor

One of the most important characteristics of the automotive cameras is high dynamic range (HDR), which requires more than 100 dB [4]. To satisfy this requirement, image sensors capture several images at different time points with different exposure times (staggered HDR) [5] and/or at different locations with different areas (split photodiode) [6]. Multiple raw data per each pixel should be processed to be merged into one to expand DR. Fig. 4 shows a typical ISP architecture for automotive image sensors. HDR merger block is located in a Bayer domain. Other color processing and image enhancement blocks are very similar to those of the mobile phone camera system.

To compare different sensor architectures, we used 1.2-Mp automotive CIS with 3.0-µm CornerPixel in a 2-stack process (pixels on the 65-nm top chip and analog/digital circuits on the 28-nm bottom chip processes) [7]. The CIS chip was operated in two configurations with on-chip ISP and off-chip ISP. To emulate off-chip ISP, we used SW-ISP to compare image performance. For fair comparison, SW-ISP functions are set

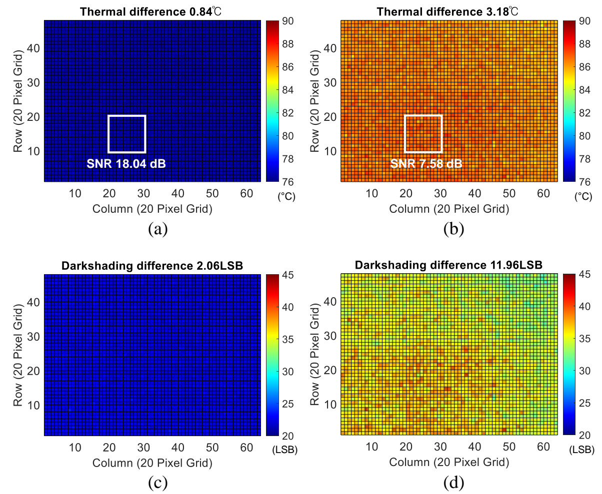

Fig. 5. Measurement results. Thermal maps of (a) off-chip ISP and (b) on-chip ISP cases, respectively. Dark level maps of (c) off-chip ISP and (d) on-chip ISP cases, respectively.

similarly to the on-chip ISP's. The test conditions are 8× analog gain, 1× digital gain, 3× ISP gain, and 33.3-ms exposure time. The measurement results are shown in Fig. 5 with two metrics: junction temperature and dark shading. In the plots of Fig. 5, full 1280×960-pixel array is grouped by 20×20 unit-pixel grid, to draw 64×48 array map. Fig. 5(a) and (b) show thermal maps for off-chip ISP and on-chip ISP cases, respectively. As on-chip ISP on the bottom die consumes more power and increases heat, CIS with on-chip ISP should have larger junction temperature, as observed in Fig. 5(a) and (b); average temperatures are 76.2 °C for off-chip and 84.6 °C for on-chip ISP cases. The junction temperature difference of 8.4 °C amounts to doubling temperature of pixel dark current [8], which will increase dark level by more than 2× with on-chip ISP on.

Thermal imbalance by the on-chip ISP causes worse thermal difference: 3.18 °C for on-chip ISP and 0.84 °C for off-chip ISP. Furthermore, this thermal imbalance increases temporal noise and dark shot noise locally, which degrades local SNR by more than 10 dB: 7.58 dB for on-chip ISP and 18.04 dB for off-chip ISP. Junction temperature increases dark level (please see Fig. 5(c) and (d)). The averaged dark level for off-chip and on-chip ISP cases are 22.30 LSB and 35.37 LSB, respectively. Local heat on the bottom chip by on-chip ISP leads to dark level imbalance (i.e., dark shading); this can be observed by dark shading of 2.06 LSB and 11.96 LSB for off-chip ISP and on-chip ISP cases, respectively.

Table 1 summarized comparison between the two cases for

Table 1. Performance summary and comparison: 1.2-Mp automotive CIS with and without on-chip ISP.

	CIS with off-chip ISP	CIS with on-chip ISP
ISP power consumption	~43 mW (estimated)	86.1 mW
Junction temperature	76.2 ℃	84.6 ℃
Thermal difference	0.84 ℃	3.18 ℃
Dark shading	2.06 LSB	11.96 LSB
ISP gate-count	-	11.6 M g/c
ISP functionality	More versatile	Limited
Data interface speed	848 Mbps (1.2Mp 20b raw data)	339 Mbps (1.2Mp 8b YUV data)
Camera module cost	Lower	Higher (heat sink, more capacitors high-current PMIC)

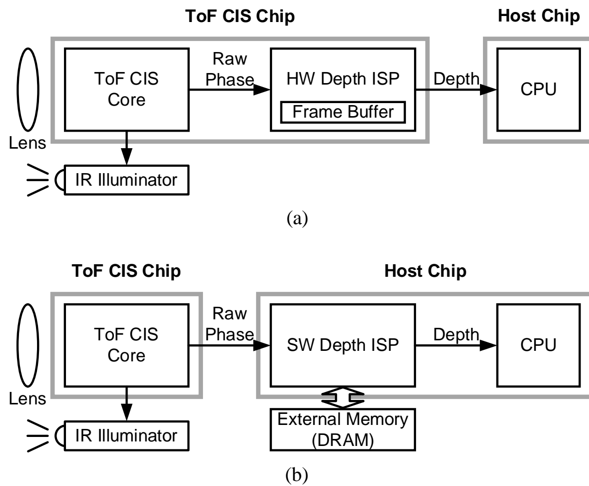

Fig. 6. Two typical ToF sensor architecture. (a) ToF sensor with an on-chip ISP and (b) ToF sensor with an off-chip ISP.

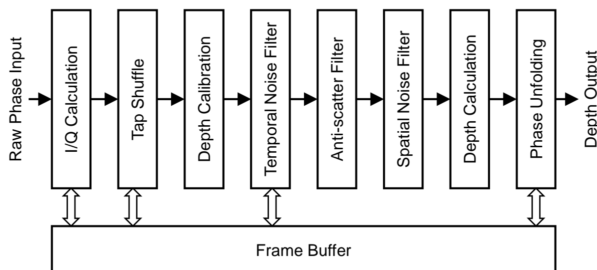

Fig. 7. Example of the depth ISP architecture for indirect-ToF image sensors.

1.2-Mp automotive CIS. For ISP power consumption, on-chip ISP power comes from measurement result, but off-chip ISP power is estimated considering better process node (14-nm CMOS), which is a normal practice for a host SoC chip. It is evident that off-chip ISP is more beneficial than on-chip ISP, in terms of sensor power consumption, sensor performance and more versatile ISP functionality. The benefit of on-chip ISP is lower data interface speed. However, considering additional cost in camera module for heat sink, more capacitors and higher-current power management integrated circuits (PMIC) for on-chip ISP, the benefit of off-chip ISP is more obvious. This benefit will be more conspicuous for the self-driving automotive systems, which requires more cameras with higher pixel resolution.

B. ToF image sensor

The two versions of ToF camera system architecture are presented in Fig. 6. Different from the automotive CIS, the sensor core should control external IR illuminator, and the raw data from the sensor core are phase-sampled data [9]. Depth ISP is entirely different from color ISP. Fig. 7 shows a simplified depth ISP architecture for the indirect-ToF image sensors. Some basic signal processing such as tap shuffling for tap mismatch removal is performed as pre-processing [10], followed by depth calculation and noise reduction filters. Phase unfolding and distance calibration are essential for the indirect-ToF sensors, which will be executed at the latter part of the ISP chain. Depth ISP sub-blocks in Fig. 7 will be one of the examples, and they could be different for ToF sensors from different sensor suppliers. It is because pixel structures are quite distinct from sensor suppliers, and the output format and the required back-end processing are closely related to the pixel structure (e.g., number of taps, 3T/4T APS). This is the reason why the unified depth ISP architecture is not proposed yet, and depth ISPs are more likely implemented in software.

Table 2. Performance summary and comparison: ToF CIS with and without on-chip ISP.

	ToF with off-chip ISP	ToF with on-chip ISP
Depth performance	Depth accuracy: < 1% Depth noise: < 1%	Depth accuracy: < 1% Depth noise: < 1%
ISP power consumption	2.0 W	0.3 W
ISP gate-count	N/A (SW-ISP)	22.0 M g/c
ISP functionality	Could be better	Acceptable
Frame rate	20 fps (VGA depth)	30 fps (VGA depth)
Data interface speed	508.7 Mbps (0.3Mp 120fps raw data)	127.2 Mbps (0.3Mp 30fps depth data)

Performance and power between on- and off-chip depth ISP are compared using the 1.2-Mp ToF image sensor [8]. The depth ISP generates VGA (640×480) depth map from 1280×960 ToF pixel array with 2×2 binning. The necessary ISP sub-blocks in Fig. 7 are implemented in SW-ISP on the Snapdragon 865 hardware development kit (HDK) platform [11] to emulate off-chip depth ISP. On-chip ISP is modeled to be implemented with hard-wired logic and frame buffer. The target depth performance for both cases is depth accuracy and depth noise within 1%, for fair comparison.

Table 2 compares ToF with off-chip and on-chip depth ISPs. ISP power consumptions are significantly different: 2.0 W and 0.3 W, for off-chip SW-ISP and on-chip HW-ISP, respectively. This huge difference comes from the fact that SW-ISP requires power overhead for the CPU core. CPU-based processing will be favorable for general purpose computation, but not good for power-efficient computation. The on-chip ISP requires additional 22 M gate-count on the sensor including frame buffer memory, and the maximum resolution may be limited due to silicon area burden, especially for frame memory. However, frame rate would be faster for on-chip HW-ISP because off-chip SW-ISP requires large latency from CPU and memory access, which is not optimal for low-cost depth processing. Lower data rate is another advantage for the on-chip ISP case.

All in all, for indirect ToF sensors, on-chip HW-ISP is better than off-chip SW-ISP, considering power efficiency. If the required depth resolution is larger and depth processing becomes more common from different sensor suppliers, which can be implemented in a unified HW-ISP on the host side, off-chip ISP may be a better choice. However, the resolution racing of ToF sensors does not occur yet, and would be relatively slow, compared to those of mobile and automotive image sensors. Thus, on-chip HW-ISP will be accepted more than off-chip SW-ISP.

4. Conclusion

We studied the most power-efficient sensor system architectures for automotive and ToF applications. For automotive CIS, which has well-established general ISP chains, off-chip HW-ISP will give more advantages than on-chip ISP. Considering fast growing trend for image resolution in automotive CIS, off-chip HW-ISP should be the most optimal solution. Moreover, eco-system in automotive imaging is being established by adopting ISP on the host side. To the contrary, for the indirect-ToF image sensors, the benefit of the on-chip HW-

ISP will be more apparent than off-chip SW-ISP; this is due to lower resolution and non-common ISP chain in the indirect-ToF sensors. Therefore, selecting the most optimal image sensor architecture will depend on common ISP chain readiness, and additional area and power in a given sensor resolution.

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