Light-induced reliability issue of NMOS using in CMOS image sensor and single-photon avalanche diode

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Abstract We present the NMOS reliability issue of increased off-current after white-light illumination. Experimental results suggest that light-induce hot electrons generated interface trap states. Enlarged off-current activated the parasitic bipolar-junction transistor. This reliability issue could be prevented with inversion layer forming in channel under a proper bias condition.

Keywords: light-induced reliability, transistor degradation, parasitic BJT action, CMOS image sensor, single-photon avalanche diode (SPAD)

1. Introduction

In complementary metal-oxide-semiconductor image sensor (CIS) technology, photodiodes have been integrated with readout/control circuit, such as in a four-transistor active pixel sensor (4T-APS) [1] and single photon avalanche diodes (SPAD) with quenching circuits [2]. To pursue large field of view (FOV) and high pixel resolution, the design of in-pixel circuit has been widely adopted with the cost of reduced fill factor. Micro-lens have been deployed to compensate fill factor by focusing light into the sensing area [3]. As a result, the maximum ambient light intensity received by a pixel could be 50 times higher [4]. With such strong light illumination, the light-induced reliability issue has to be addressed..

2. Experimental Method

To study light-induced reliability issue in N-type metal-oxide-semiconductor field effect transistor (NMOS), we measured drain current (I_d) as a function of gate voltage (V_g) in dark before and after certain stress. The drain voltage (V_d) was fixed at 1.5 V and the gate voltage Vg was swept from 0 to 3 V. We considered two parameters in stress condition. The first, the illumination of light sources was either continuous wave (CW) or in pulsed mode. The second, the gate bias Vg (0 – 3 V)was applied either with a constant voltage (DC mode) or with a 1-kHz square wave (AC mode). There were two testing devices. input/output (I/O) and core NMOS transistors having the same channel width/length W/L of 4/0.45 μm. Xenon lamp was used as light source without optical filter.

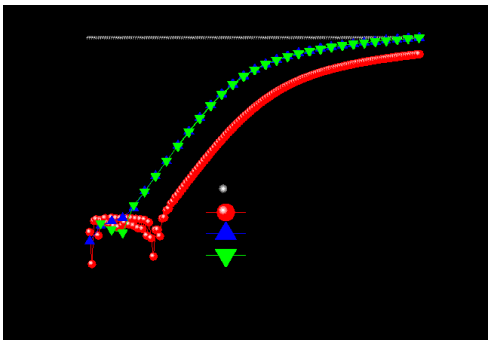

Fig. 1. I_d-V_g curves in dark after and before stress sweeping V_g from 0 V to 1.5 V under CW illumination on I/O and core NMOS transistors for 4 hours.

3. Result and Discussion

We stressed the two NMOS with 2000 I_d-V_g measurements under CW illumination in 4 hours. Figure 1 shows the I_d-V_g curves before and after stress and indicates that the drain current of I/O NMOS increases to over 1 mA even in off-state. In contrast, this degradation does not appear in core NMOS. To clarify this reliability issue in I/O NMOS, we further performed three kinds of stress conditions for five minutes as follows:

1. Vg of dc voltage under CW illumination.
2. Vg in DC mode under pulsed illumination.
3. Vg in AC mode under pulsed illumination.

Figure 2(a) illustrates, with stress condition 1, I_{off} does not increase until V_g biased at 0.2 V. The degradation increased I_{off} from ~20 to ~200 pA. In addition, the degradation was not recoverable and could get worse with longer stress time as we observed. With stress condition 2, shown as Fig. 2(b), the degradation begins at larger V_g of 0.6 V. By changing the illumination from CW to pulsed mode, degradation threshold of NMOS appears at the higher V_g and a much worse I_{off} was obtained. The reason could be attributed to the increased

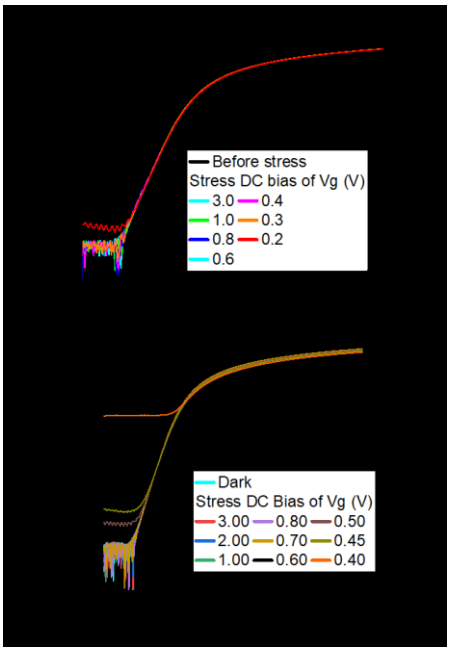

Fig. 2. I_d-V_g curves in dark after DC stress bias of different V_g and V_d = 1.5 V under (a) CW and (b) pulsed illumination.

interface trap density. Since electron-hole pairs generated by high energy photon so the excess hot electrons could be vertically accelerated by the electric field and then hit SiO_2/Si interface to induce surface states. It is known that in CMOS technology, to decrease dangling bond/surface traps in gate oxide, hydrogenation process transfers dangling bonds into stable Si-H bonds. The weak Si-H bonding could be broken by hot electrons so the interface traps emerge [5-6]. As we have seen, the light-induced I_{off} increase did not occur at high Vg. Because the high V_g induced an inversion layer in the channel, the inversion charges could act as a protection layer. Figure 3(a) schematically shows the NMOS in linear region. Photo-generated hot electrons cannot energetically approach channel/oxide interface but can only flow to the drain because of the presence of inversion layer. With decreasing V_g in Fig. 3(b) as the NMOS in saturation region, the pinch-off effect drives the inversion charges away from the drain side. The SiO_2/Si interface is then exposed to the hot electrons damage. In addition, in terms of the illumination mode, we observed that the degradation intensified with the pulsed mode photons. Under CW-mode illumination, a steady photocurrent along the channel serves as the protection layer although not as effectively as the inversion charges do. The pulsed mode illumination prolongs the total time before forming a steady photocurrent so the hot-electron damage becomes more serious. The high density of interface traps appears in the overlap region of drain and gate. The band bending enhances I_{off} probably due to trap-assisted tunneling current [7].

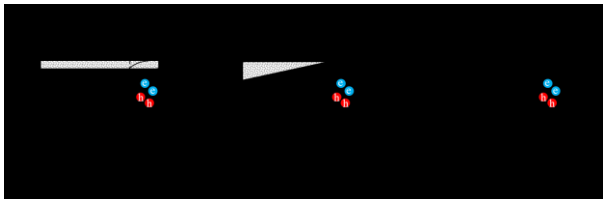

Fig. 3. Hot electrons damage mechanism in (a) linear, (b) saturation, and (c) cut-off states under CW illumination and energy band diagram at channel near drain.

The worst case occurred with stress condition 3, in which both light illumination and gate were operated in the pulsed mode. Because the depletion of inversion layer is faster than the formation of steady photocurrent, the interface exposed to hot-electron damage intensifies with the AC-mode gate bias. Figure 4(a) shows that I_{off} increase even at V_g of 2.5 V and I_d-V_g curve does not have any switch characteristic for V_g of 2.1 V indicating a serious interface degradation. For V_g lower than 2.1 V, even the on-current (I_{on}) increases. The NMOS transistor cannot work because I_{on} is equal to I_{off} after stress so the corresponding circuit function could be serious affected.

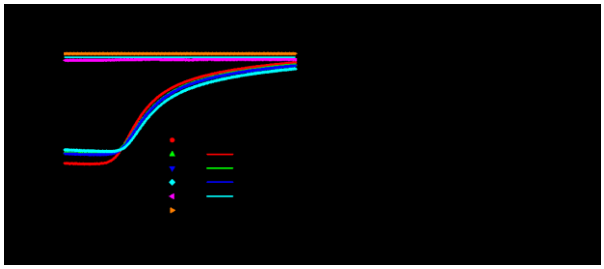

Fig. 4. (a) I_d-V_g curves in dark after applying AC-mode gate volage under pulsed mode illumination, and (b) NMOS parasitic BJT schematic. R_b is the parasitic bulk resistance.

In fact, the enlarged I_{off} current could activate the parasitic bipolar junction transistor (BJT) as shown in Fig. 4(b). I_{off} flows from drain to bulk/substrate and makes the voltage drop crossing on R_b so V_b is not bias on 0 V. As a result, V_{sb} (V_b-V_s) becomes positive and high enough to turn on the parasitic P-N junction between source and bulk as well as the parasitic BJT.

4. Conclusion

Under white-light illumination, the density of interface traps increased, when photo-generated hot electrons were accelerated by vertical electric field to surface. Enlarged I_{off} could activate the parasitic BJT and it formed a new leakage current path. We observed the worst case occurred with stress condition 3 and this reliability issue caused the corresponding circuit function to be affected. However, inversion charges could protect channel/oxide interface, especially when NMOS operated in linear region. Therefore, the light-induced reliability issue only observed on I/O devices rather than core devices, because core devices had lower threshold voltage.

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