An Area Efficient Readout Circuit for CMOS Image Sensor with Lateral Overflow Integration Capacitor

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Abstract A lateral overflow integration capacitor (LOFIC) CMOS image sensor (CIS) can realize high dynamic range (HDR) imaging with low conversion gain (LCG) signal for large full well capacity and with high conversion gain (HCG) signal for small dark noise. However, the LOFIC CIS requires 2-channel readout circuits for LCG and HCG signals whose signal polarities are inverted. In order to provide cost efficient LOFIC CIS, a 1-channel readout circuit which can process both HCG and LCG signals is presented in this paper. The combination circuit of an inverting amplifier for HCG signal and a non-inverting attenuator for LCG signal can reduce the area of the readout circuit by half compared to the conventional 2-channel readout circuit. The readout circuit is fabricated with a 0.18μm CMOS process with MIM capacitor, achieving the readout noise of 130μV_{rms} in the HCG mode and the signal range 1.3V in the LCG mode.
Keywords: CMOS image sensor, LOFIC, HDR, readout circuit, small area.

1. Introduction

CMOS image sensors (CISs) utilized under extreme-illumination conditions such as outdoors require high dynamic range (HDR) imaging technology to avoid underexposure and overexposure of various objects in a scene. Many approaches have been proposed for HDR imaging, and a CIS with lateral overflow integration capacitor (LOFIC) [1-3] is one solution. The LOFIC-CIS realizes large full well capacity at low conversion gain (LCG) mode and small dark noise at high conversion gain (HCG) mode. However, the LOFIC-CIS requires 2-channel readout circuits [4] because the polarities of LCG and HCG signals are inverted. In order to provide low-cost LOFIC-CIS, we propose an area-efficient double sampling (DS) circuit which can process both HCG and LCG signals with an inverting amplifier [5] and a non-inverting attenuator [6].

2. Proposed readout circuit

Figure 1(a) shows a circuit diagram of a baseline 2-channel DS circuit. Figure 2 shows a timing diagram of the DS circuits. During the HCG mode when Φ1 is turned on, a pixel reset level V_{RH} is input to the DS circuit followed by a signal level V_{SH}. The inverted difference given by $V_{OUT}=C_S/C_F\times(V_{RH}-V_{SH})$ is output to an analog/digital converter (ADC). During the LCG mode when Φ2 is turned on, a pixel signal level V_{SL} is input followed by a reset level V_{RL}. The non-inverted difference given by $V_{OUT}=C_C/(C_C+C_{ATN})\times(V_{RH}-V_{SH})$ is output to the ADC. Thus, this baseline DS circuit can output the same polarity signals to the ADC regardless of the order of the reset and signal levels in the HCG and LCG mode. Figure1(b) shows a DS circuit whose area is reduced sharing the ADC. Figure 1(c) shows a proposed DS circuit in which the clamp capacitor Cc in the attenuator is merged with the sampling capacitor of the ADC ($C_{S,ADC}$).The total capacitance of these DS circuits is summarized in Table.1 to roughly estimate the circuit area because the area of the capacitor is dominant in the circuit layout. The area of the proposed DS circuit can be reduced around 50% compared to the baseline circuit. Besides, readout noise at the LCG mode is reduced from 652.6μVrms to 452.9μVrms since the buffer is omitted.

3. Measurement Results

In order to verify the concept of the proposed DS circuit, a test circuit shown in figure 3 is fabricated with 0.18μm CMOS process with MIM capacitor. For simplicity, the ADC is replaced with a voltage follower. Figure 4 shows a photograph of the fabricated test chip. The layout size of the DS circuit is 6.02μm width and 977μm height. 160 dummy columns are also implemented to replicate layout constraints of column parallel readout circuit for the CIS.

Figure 5 shows measured input and output characteristics of the HCG and LCG mode of the proposed DS circuit, where the gain ratio of the HCG and LCG mode was 10. The horizontal axis and the vertical axis show the voltage difference (Vr-Vs) and output voltage from the DS circuit, respectively. The input signal ranges for the case of 0.85V ADC input range were 0.15V at the HCG mode and 1.3V at the LCG mode. The readout noise was 130.6μV at the HCG mode and 452.9μV at the LCG mode. If the proposed DS circuit is utilized with the LOFIC pixel whose conversion gain is 160μV/e- at HCG and 10μV/e- at LCG [2], the DR of the CIS will be 104dB. The performance summary of this test chip is summarized in Table.2.

5. Conclusion

The area-efficient DS circuit for the LOFIC-CIS is proposed and the area is reduced by 50% compared to the baseline circuit. Since the maximum input signal at the LCG mode and the readout noise at the HCG mode are respectively 1.3V and 130.6μV, the proposed circuit is applicable for the LOFIC CIS over 100dB DR.

Acknowledgements

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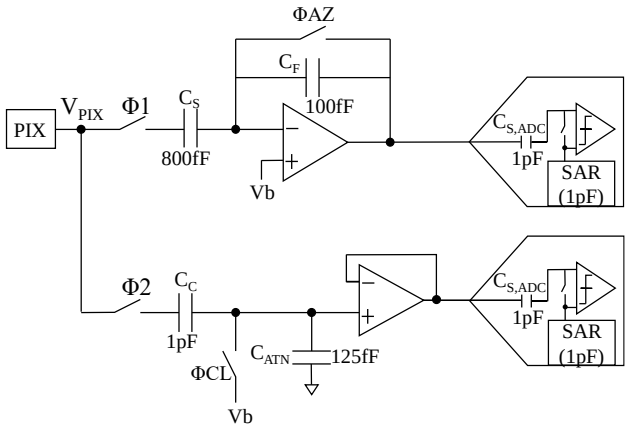

Fig.1(a) a baseline DS circuit

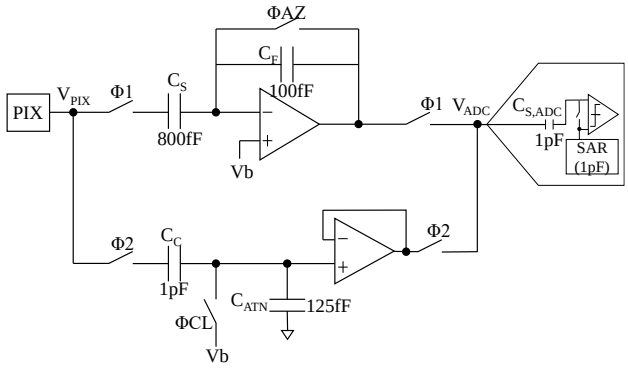

Fig.1(b) a DS circuit with shared ADC

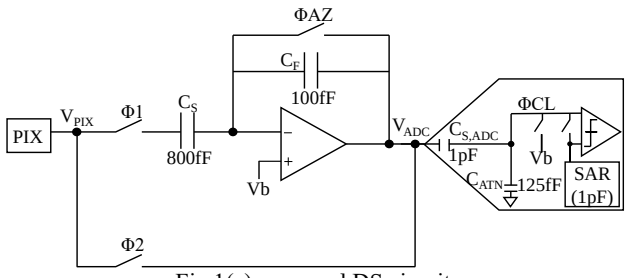

Fig.1(c) proposed DS circuit

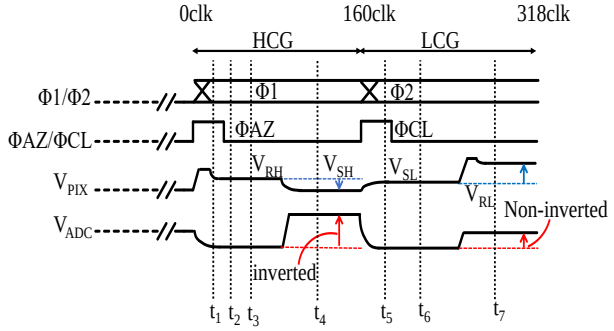

Fig.2 timing diagram of the DS circuit

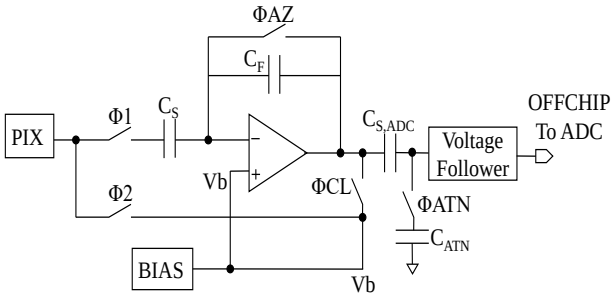

Fig.3 test chip of the proposed DS circuit

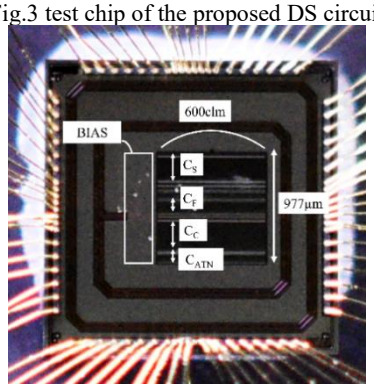

Fig.4. a photograph of the fabricated test chip

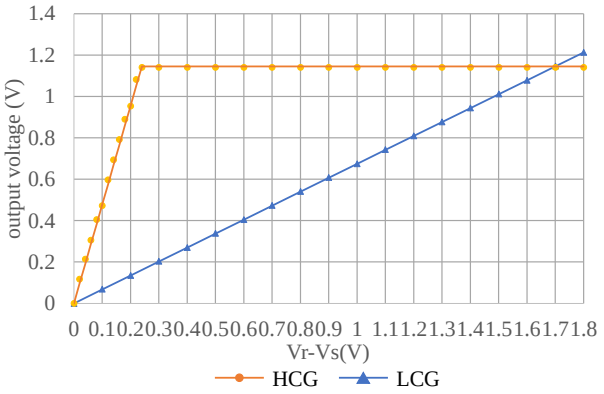

Fig.5 input and output characteristics of the proposed DS circuit

Circuit type	Total capacitance (fF)	LCG Noise (μVrms)
Baseline	6025 (100%)	652.6
ADC shared	4025 (66.8%)	652.6
proposed	3025 (50.2%)	491.4

Table.1 total capacitance of DS circuits

Process	0.18μm 1P5M CMOS with MIM	
Supply voltage	2.6 V~3.0 V	
Temperature range	0~60 ℃	
Column pitch	6.02 μm	
#Columns	160	
	HCG	LCG
Measurement noise	130.6 μVrms	452.9 μVrms
Signal range	0.15 V	1.3 V
Power consumption	23μW @2.8V	

Table.2 performance summary of this test chip