A Variable-Resolution SAR ADC with 10-bit Image Capturing Mode and 5-bit Feature Extraction Mode

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Abstract As the development of the Internet of Things and the Trillion Sensor Universe, the amount of information collected by CMOS image sensors will be drastically increased, and an image recognition based on deep learning is getting more important to process the big imaging data. However, the data captured by conventional image sensors is redundant for the deep learning because features of the imaging data is extracted in the deep neural networks. In this paper, a column successive approximation register (SAR) analog/digital converter (ADC), that converts the pixel output signal into 10-bit digital signal during an image capturing mode and into 5-bit digital signal during a feature extraction mode, is proposed for an image sensor which can generate the imaging data and the feature data. The power consumption during the 5-bit feature mode is reduced by 99.76 % compared to the imaging mode by turning-off the preamps in the comparator. The 640-column parallel ADC was manufactured in a 0.18μm CMOS process, achieving ±1.51 LSB and ±0.12 LSB DNL for the 10-bit imaging mode and 5-bit feature mode.

Keywords: CMOS image sensor, big data, Trillion Sensor Universe, Deep learning, Image recognition, Low Power Consumption, A/D convert

1. Introduction

As the development of the Internet of Things[1] and the Trillion Sensor Universe, the amount of information collected by CMOS image sensors (CISs) will be drastically increased, and an image recognition based on deep learning is getting more important to process the big imaging data. However, the data captured by conventional image sensors is redundant for the deep learning because features of the imaging data is extracted in the deep neural networks. In order to reduce the redundancy in the image recognition system, an image sensor capable of analog convolution using crystalline oxide semiconductor FET was proposed [2] . A CIS which can generate horizontal edge is also proposed, and it is found that the bit-resolution for the image classification with a convolutional neural network can be reduced to 3-bit [3]. In this paper, a variable bit-resolution ADC for the feature extractable image sensor is proposed.

2. Variable bit-resolution SAR ADC

Figure. 1 shows a proposed SAR ADC, in which the bit-resolution can be changed according to the operation mode to save the power consumption during the feature extraction mode. The ADC consists of a comparator that is composed of preamps A1, A2, and a latch, and a SAR DAC that is composed of switches and capacitors.

In the image capturing mode, the voltage difference between signal and reset of J-th row pixel is converted to 10-bit digital signal as shown in Fig. 2(a). First, all switches in the DAC are switched to V_{ref_hi}, and the comparator is reset when ΦAZ1, ΦAZ2, and ΦLATCH are turned-on. When ΦAZ1 is turned-off, the voltage stored in C_S is given by $V_{Cs} = V_{RST} - e_1$, where e_1 is reset noise of A1. When ΦAZ2 is turned-off, the voltage stored in C_C is given by $V_{Cc} = e_2 - (1 + A_1)e_1$, where A_1 and e_2 are respectively gain of A1 and reset noise of A2. After the photo electron transfer during ΦTG high, the ADC input voltage drops to $V_{PIX} = V_{RST} - \Delta V_{SIG}$. The input to the latch is then given by $V_{latchin} = A_1A_2\left(-\Delta V_{SIG} - \frac{e_2}{A_1} + \frac{e_3}{A_1A_2}\right)$. Thus, the pixel reset noise is removed and the comparator reset noise is surpressed by the gain of preamps.

In the feature extraction mode, the voltage difference between signal of (J-1)-th row and signal of J-th row is converted to 5-bit digital signal as shown in Fig. 2(b), in which the preamps are turned-off and the latch is swithced to dynamic type by turning the current source off to save the current consumption. The J-th row signal is readout follwing to the (J-1)-th row signal so that the latch input signal is given by $V_{latchin} = \{\Delta V_{SIG}(J-1) - \Delta V_{SIG}(J)\} - \{V_{RST}(J-1) - V_{RST}(J)\} + e_3$. Even though the pixel reset noise and the comparator reset noise are also readout in addition to the vertical pixel signal difference, the noise is acceptable for image recognition with horizontal edge signal. Since the latch input singal rises or drops according to the pixel signals, offset voltage is added to the SAR DAC. During Φ3 is turned-on for the sampling of (J-1)-th row pixel signal in C_S, only the MSB DAC capacitor (32C) is switched to V_{ref_lo}. After Φ3 is turned-off, the 32C is switched to V_{ref_hi} to convert both the positive and negative input voltage to the ADC.

The ADC input range are respectively given by 1.0V at the image mode and ±0.5V at the feature mode when $V_{ref\_hi} - V_{ref\_lo} = 1.0$.

3. Simulation and Measurement results

The proposed SAR ADC is fabricated with 0.18μm CMOS process. Figure. 3 shows the photograph of the test chip, in which 640-column ADCs are implemented. According to SPICE simulation results, current consumption of an ADC is 24.1μA at the image mode and is reduced to 57.0nA at the feature mode. Figure. 4 shows the measured input and output characteristics. It is noted that the nonlinearity is caused by capacitance error in the split capacitor. Except for the split capacitor error, the DNL was ±1.51 LSB at the image mode and ±0.12 LSB at the feature mode. Figure. 5 shows an output image when ramp signal was input the ADC. The ADC characteriscs are summarized in Table 1.

4. Conclusion

The variable bit-resolution ADC for the feature extractable CMOS image sensor is proposed. The ADC converts the pixel signal to 10-bit digital signal at the image mode with current consumption 24.1μA and coverts the vertical adjacent pixel signal difference to 5-bit digital signal at the feature mode with low current consumption 57.0nA. The ADC can also convert the positive and negative input signal during the feature mode by the change of the control sequence. The 640-column parallel ADC fabricated with a 0.18μm CMOS process achieved ± 1.51 LSB

DNL at the 10-bit image mode and ± 0.12 LSB DNL at the 5-bit feature mode.

Acknowledgments

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References

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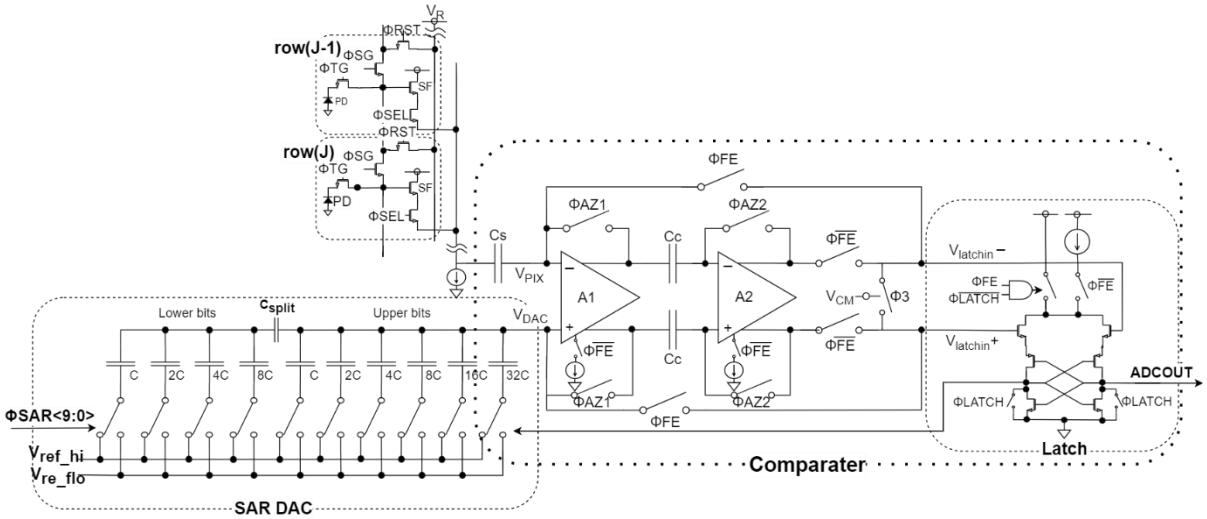
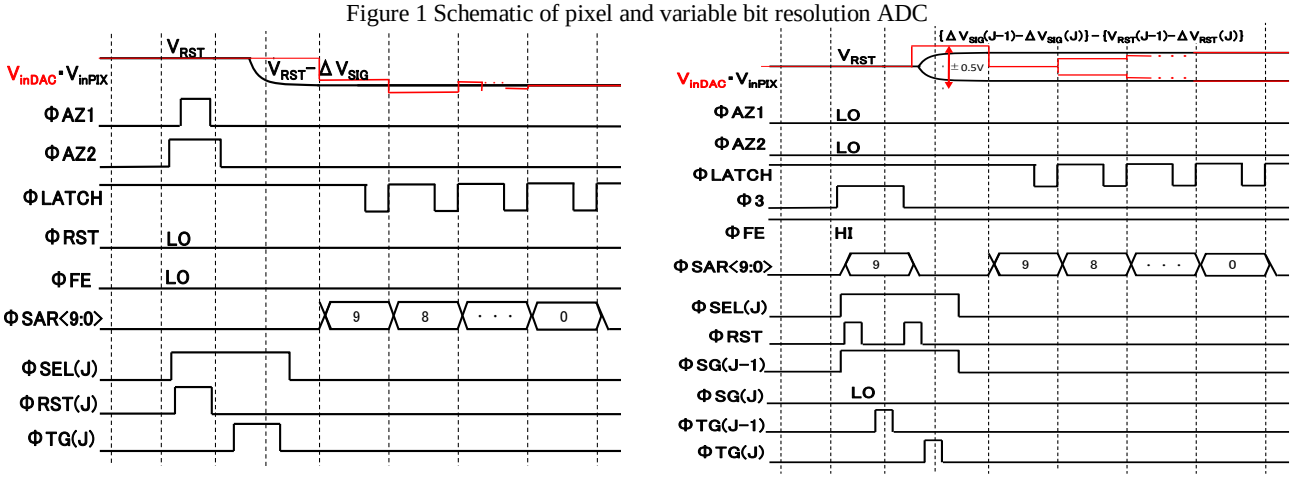


Figure 1 Schematic of pixel and variable bit resolution ADC



(a)Image capturing mode (b)Feature extraction mode

Figure 2 Timing diagram

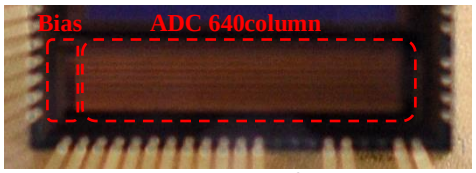
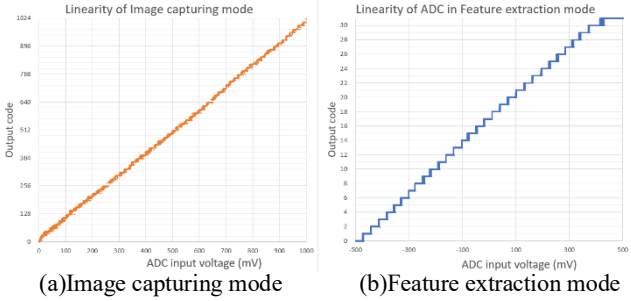
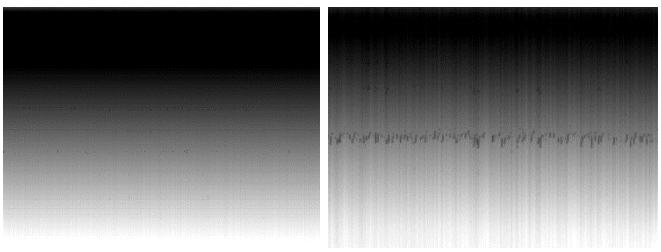


Figure 3 Photograph of the test chip



(a)Image capturing mode (b)Feature extraction mode

Figure 4 Input/Output Characteristics



(a)Image capturing mode (b)Feature extraction mode

Figure 5 Output image by ramp signal

Table 1 Summary of ADC characteristics

Mode	Image capturing	Feature extraction
Procces	0.18um 1.5M CMOS	
Number of pixels	640[H]	
Column pitch	5.6um	
Resolution	10bit	5bit
DNL	±1.51 LSB	±0.12 LSB
Power consumpition	24.1uA	57.0nA