A 9-shared 3x3 Nonacell Image Sensor with 0.64µm unit pixels for Read Noise and Low-illuminance SNR enhancement

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Abstract

A 0.64µm pitch 108 mega pixels CMOS image sensor has been demonstrated and the advanced nonacell structure is used to maximize low-light performance. In this work, a new 9 charge-sum (9S) method is employed, and operation method and parameters for determining signal to noise ratio (SNR) are compared with the conventional 3 charge-sum 3 voltage-average (3S3A). The image characteristics have been examined as the binning method, the enhancement of the device performance due to the generated signal and conversion gain effect have been quantitatively analyzed. Compared to 3S3A, read noise of 9S is reduced by 45%, and improved SNR value is confirmed at low-light operating condition.

Keywords: CMOS image sensor, Nonacell, binning method, charge-sum, read noise, SNR.

Introduction

In recent years, CMOS image sensors (CIS) have attracted great attentions as a mobile application since it is considered as one of the important feature in selecting mobile devices. For this reason, CIS performance improvement is continuously required, and various efforts are underway to improve quality [1]. The demand for high resolution is increasing for instance, however, the pixel size should be shrank due to the limitation of optical format of the lens module [2]. The sub-micron pixel was mass-produced for the first in 2018 [3], and recently, 0.64µm pixel is the smallest one under mass production [4]. However, as the pixel size shrinks down, characteristics such as full well capacity (FWC), sensitivity, and signal-to-noise ratio (SNR) are inevitably degraded. As a way to solve this problem, a pixel summation method such as 2x2, 3x3, and etc. has been proposed and is widely used.

3x3 nona binning is firstly introduced with 0.8µm pixel [5], and it can switch full and binning resolution of 108Mp and 12Mp, respectively. By merging 9 photo-diodes (PDs), especially in low illuminance condition, it improves sensitivity. However, the previous 3x3 nonacell suffered from relatively poor image quality in low illumination condition due to high read noise. In this work, the noise characteristics according to the 3x3 binning method are analyzed in the nonacell structure, and the low-light SNR improvement with new 9 charge sum method is proposed and demonstrated in 0.64µm pixel.

Pixel architecture

In the previous work [5], three 1x3 shared pixel units are merged to generate a 3x3 pixel with the same color. In nona-binning mode, we used 3 charge-sum 3 voltage-average mode (denoted by 3S3A), which indicates that signal electrons in shared 3 PDs are added in the floating diffusion (FD), and the three vertical outputs are averaged at the voltage domain. In this work, on the other hand, 9 charge-sum (denoted by 9S) for nona-binning is adopted, and the main difference of the 9S between 3S3A is the number of 9 PDs commonly shared to the FD node. The physical structures are compared in Fig. 1(a) and (b).

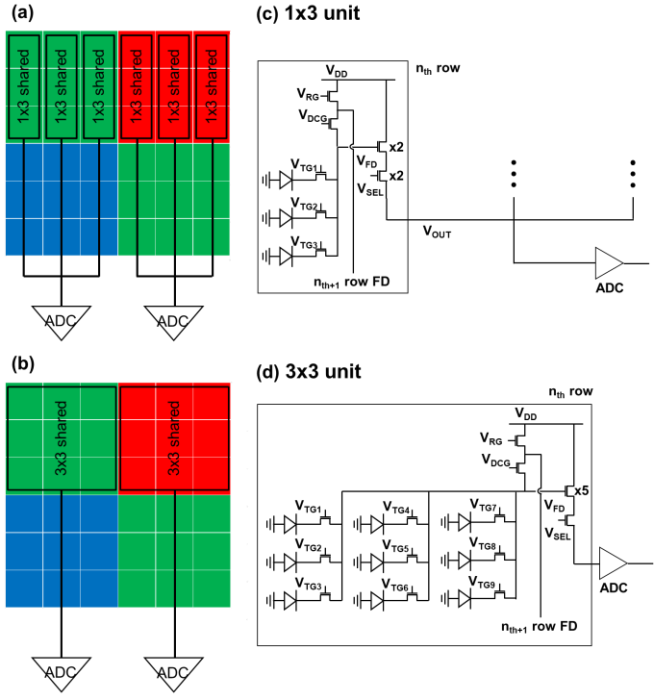

Fig. 1 Nonacell structures with (a) 1x3, (b) 3x3 shared pixels are compared, and the pixel schematic is shown in (c), (d) respectively.

Since 9 pixels share the same FD, the FWC in binning mode that affects the SNR of high-illumination condition is determined by the FD dynamic range, not the PD's FWC. Therefore, it is important to increase FD capacitance so that it can take as many electrons as possible. In order to make FD capacitance larger, a technique of simultaneously using the capacitance of the adjacent FD node is controlled by reset (RG) and dual conversion gain (DCG) transistors.

TABLE I
3-sum 3-average vs 9-sum mode

	Unit	Full	3S3A	9S
	lsb/e-	$C.G$	$⅓{\cdot}C.G$	$C.G$
Signal	lsb	S	$3S$	$9S$
Shot noise	lsb	$\sqrt{S}$	$\sqrt{3S}/\sqrt{3}$	$\sqrt{9S}$
SF noise	lsb	N_{SF}	$N_{SF}/\sqrt{3}$	N_{SF}
ADC noise	lsb	N_{ADC}	N_{ADC}	N_{ADC}
S/N ratio	-	$\frac{S}{\sqrt{S+N_{SF}^2+N_{ADC}^2}}$	$\frac{9S}{\sqrt{9S+3N_{SF}^2+9N_{ADC}^2}}$	$\frac{9S}{\sqrt{9S+N_{SF}^2+N_{ADC}^2}}$

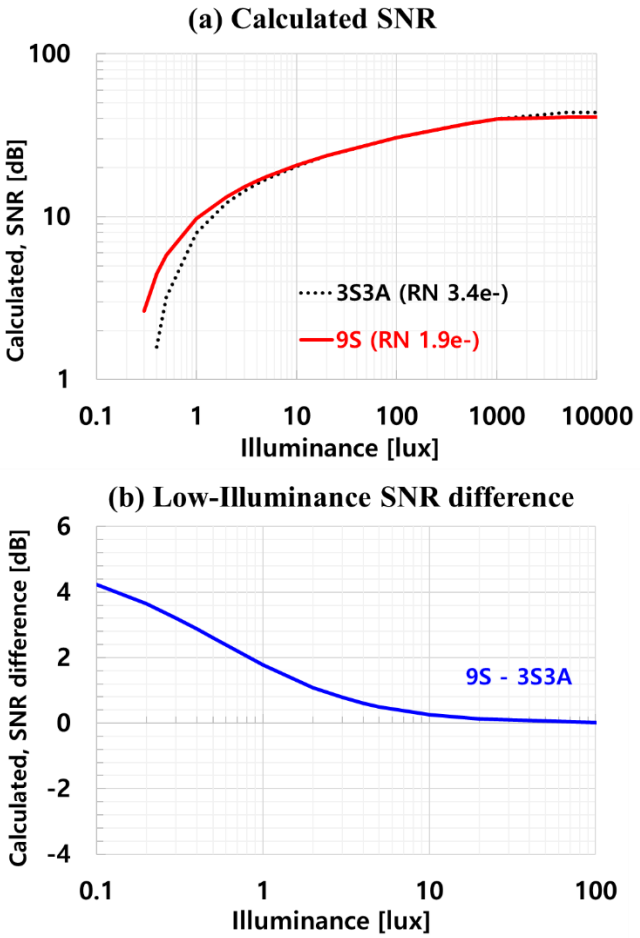

Fig. 2 Calculated SNR difference between 9S and conventional 3S3A as a function of illuminance and the same pixel size is assumed.

In the mode where FD capacitance is largely used, the FD node is connected to adjacent 9-shared FD node and total 18-pixels are connected with a single node. Using this method, FD capacitance is increased more than 4 times compared with 9-shared FD capacitance, and the circuit schematic is shown in Fig. 1(c) and (d).

The characteristics of the 9S and conventional 3S3A mode are simply compared in Table I. The conversion gain decreases to 1/3 due to a result of the average, even though the physical FD capacitance is the same. As a consequence, the input referred noise (unit of electron, to be specific) of 3S3A is 3 times larger than that of 9S. In order to compare the SNR between 9S and 3S3A, the signal and noise are analyzed by dividing them in the unit of lsb. Photon shot noise of 9S is relatively large due to its signal, and the dark noise of 3S3A is less than 9S mode since 3S3A averages noise. The signal level takes over the total noise in low-illumination condition (N>>S), and as a consequence, SNR of 9S is superior to that of 3S3A. Fig. 2 shows the differences of SNR between 9S and conventional 3S3A as a function of illuminance. Notice that, for illuminance <10 lux, SNR of 9S is higher than that of 3S3A as we discussed.

Result and discussion

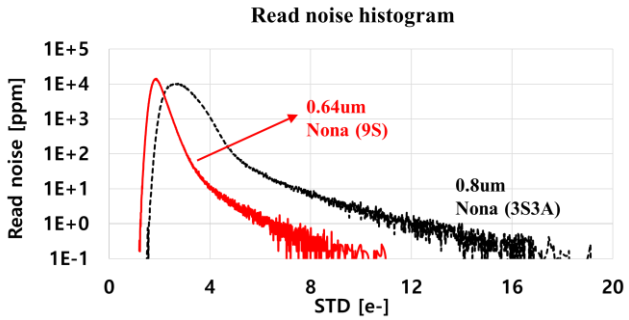

Fig. 3 The read noise histogram, and 0.64μm for 9S and 0.8μm for 3S3A are compared.

The 9-shared pixel structure has advantages in the placement of transistors, such as source follower (SF), RG, DCG, SEL transistors, in the pixel. As the number of shared pixels increased, there is an additional space for transistors, which is used to apply multi-finger SF. By using multi-finger SF, the channel area of SF is increased, and the width increases as much as it is used in parallel to maximize trans-conductance. As consequence, random telegraph noise of 0.64μm pixel is similar to that of 0.8μm one, even though pixel pitch is reduced down to 0.64μm. Furthermore, it is confirmed that the read noise is reduced from 3.4 to 1.9e-, and the histogram is shown in Fig. 3. Note that read noise in electron unit is increased due to the effect of reducing conversion gain affected by averaging, and it can be represented by $N/\sqrt{3}$ and $\sqrt{3}N$ for lsb and electron units, respectively, where N denotes full mode noise.

The measured characteristics of 9S mode are compared with those of conventional 3S3A as shown in Table II, and we can clearly notice that 9S mode is superior to conventional 3S3A one. SNR characteristic, especially in low illuminance (1lux), is improved due to the read noise. FWC, dark current, and white spot which are key factors in CIS performance remained at the same level as previously published studies [4].

TABLE II
Comparison of pixel characteristics.

	Unit	Tetra	Nona	
		0.64μm	0.8μm	0.64μm
Linear FWC	e-	*6,000*	*6,000*	*6,000*
Dark current	e-/s	*1.1*	*1.5*	*1.1*
Read Noise	e-	*1.4*	*3.4*	*1.9*
RTS	ppm	*4*	*2*	*0*
White spot	ppm	*15*	*10*	*10*
1lux SNR	dB/μm^2	*4.3*	*3.3*	*4.1*

White spot : # of pixels≥160lsb @1-frame, gain x16, 200msec, Tj=60℃

RTS: # of pixels≥30lsb @difference between 2-frame, gain x8, 0msec, Tj=60℃

Read noise : 20-frame, gain x16, 33msec, Ta=25℃

Conclusion

In conclusion, we have demonstrated the read noise and SNR characteristics of 9S CMOS image sensor with 0.64μm

unit pixels. A new binning scheme has been introduced to improve SNR at low illuminance, and the 9S and conventional 3S3A are compared in terms of conversion gain, noise, and SNR. The proposed 9 charge sum binning method can dramatically improve read noise, and a 3x3 nonacell structure that can provide image quality equivalent to big pixels at low illumination condition and high resolution at high illumination condition has been completed.

References

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