A Study on Two Step Reset LOFIC Pixel to Reduce SNR Gap

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I. Introduction

High dynamic range (HDR) CMOS image sensors (CISs) are expected for machine vision purpose under extreme illumination conditions such as outdoor. An image sensor that has lateral overflow integration capacitor (LOFIC) [1] is one solution to realize the HDR-CIS. The LOFIC pixel is composed of typical 4 transistors, an overflow capacitor (CS) and a switching gate (SG). During high conversion gain (HCG) mode when SG is turned off, dark signal integrated in a photodiode (PD) is readout with low noise because of reset noise cancellation by correlated double sampling (CDS). However, during low conversion gain (LCG) mode when SG is turned on, bright signal integrated in the PD and CS is readout with larger noise because the reset noise is not cancelled by differential double sampling (DDS). The noise gap results in signal to noise ratio (SNR) drop at the conjunction point between HCG and LCG signals [2].

In this paper, a pixel circuit, which reduces the LCG reset noise without additional transistors in the pixel, is presented.

II. Overview of pixel circuit with Two Step Reset

Figure 1 shows a schematic of pixel array and peripheral circuits of the proposed LOFIC-CIS. A pixel is same as the conventional LOFIC-CIS which consists of a PD, a transfer gate (TG), a source follower transistor (SF), a select gate (SEL), a switching gate (SG), a sampling capacitor (CS) and a pixel reset gate (RST). In the conventional LOFIC-CIS, the reset noise hold in the CS after RST is turned off given by 643 μV_{rms} when CS = 10 fF, resulting in the SNR drop. A column reset circuit which consists of column reset gate (RST') and a column reset sampling capacitor (CS') are also located outside the pixel array. In this proposed LOFIC-CIS, RST and RST' are sequentially turned off to reduce the LCG reset noise, and this pixel circuit is named two step reset (TSR) pixel.

As shown in Fig. 2(a), readout operation timing is the same as the conventional LOFIC-CIS except for the LCG reset period. During the LCG reset period, both RST and RST' are turned on to reset floating diffusion node (FD) and the CS (t_1). The capacitance of the CS' is 1 pF that is 100× larger than that of CS so that temporal noise frozen on the RD node after RST' is turned-off is given by 64.3 μV_{rms} (t_2). The RST is then turned off (t_3). As long as RST is an ideal switch, the reset noise hold on CS will be 64.3 μV_{rms} because the RD node is high impedance. However, the charge injected to the CS flow to the RD node due to voltage drop difference between the CS and the RD node during the on-to-off transition time of RST gate as shown in Fig. 2(b), resulting in larger reset noise hold in the CS.

In order to reduce the reset noise in the CS, asymmetric structured RST is presented as shown in Fig. 3. With the tapered channel [3] shown in Fig. 3(a) and a half-buried channel shown in Fig. 3(b), the charge flow into CS is decreased. The voltage difference between the CS and the RD node when RST is turned off is thus decreased, so that the temporal noise caused by the current flow from the RD node to the CS is suppressed.

III. Simulation Results

Figure 4 shows transient noise SPICE simulation results of the TSR pixel. In order to confirm the noise caused by charge flow during the on-to-off transition time of RST, the fall time t_f is swept from 1 ps to 10 ns. The horizontal and vertical axes show t_f and the noise amount, respectively. When t_f is long, the noise of the TSR pixel is comparable to that of the conventional pixel, in which the theoretical reset noise is 643 μV_{rms}. However, when t_f is short, the noise of the TSR pixel is decreased from that of the conventional pixel, because the charge injected to the CS cannot fully flow into RD in the short time period. When t_f = 100 ps that is our target for RST clock driver, the reset noise is 375.2 μV_{rms} that is reduced by 28.3% compared to the conventional LOFIC-CIS.

The effect of the asymmetric structure RST is also feasibility studied with TCAD device simulations. Figure 5 shows the potential profile of the RST at the instance when RST is turned off. While potential shape in the channel of the normal structure RST is symmetric, the potential level in the CS is higher than that in the RD node. This difference of potential levels suggests that charge injected to small CS increases the potential level of the CS and charges flow to the RD node during the on-to-off transition. On the other hand, the potential level in the CS is close to that in the RD node with the asymmetric structure RST because the potential slope in the channel transfers the most of the charge to the large RD

node, and the increase of the CS potential is small. Since the potential difference between the CS and the RD node is small, it is expected that the current flow from the RD to the CS is suppressed and the reset noise is reduced.

IV. Evaluation result of a test chip

To verify the reset noise of the proposed TSR pixel, a test chip was fabricated with a 0.18 μm CMOS process. Figure 6 shows a photo of the test chip, in which $160(\mathrm{H}) \times 4(\mathrm{V})$ pixels without PDs are implemented. Instead of the asymmetric RST with the tapered and half-buried channel structure, a simple asymmetric RST with additional contacts to the RD node shown in Fig. 7 is implemented due to fabrication process limitation. Since resistance value to the RD node is half of that to the CS, larger number of charges is expected to be injected to the RD node.

Figure 8 shows measurement setup of the test chip. A test chip (DUT), an 12-bit ADC and a FPGA are mounted on a PCB board. The power supply voltage V_{dd} and the pixel reset voltage V_R are provided by external power sources. The digitized DUT output with the ADC is transferred to the PC via USB and analyzed. Figure 9 shows the reset noise readout chain in the test chip, in which $v_{n,rst}$, $v_{n,SF}$, $v_{n,RO}$ and $v_{n,ADC}$ are respectively pixel reset noise, SF noise, readcout circuit noise and ADC noise. The measured noise with CDS operation is given by

$$v_{n,CDS}^2 = v_{n,SF}^2 + v_{n,RO}^2 + v_{n,ADC}^2, \tag{1}$$

where the pixel reset noise $v_{n,rst}$ is cancelled. On the other hand, the measured noise with DDS operation is given by

$$v_{n,DDS}^2 = 2v_{n,rst}^2 + v_{n,SF}^2 + v_{n,RO}^2 + v_{n,ADC}^2, \tag{2}$$

where the pixel reset noise is doubled due to uncorrelated reset noise. Therefore, the pixel reset noise is evaluated with measurement results at CDS operation and at DDS operation, which is given by

$$v_{n,rst} = \sqrt{\frac{v_{n,DDS}^2 - v_{n,CDS}^2}{2}}. \tag{3}$$

The pixel reset noise is summarized in Table I. In the case of the conventional pixel, the measured reset noise is 1028 μV_{rms}, even though it is larger than theretical value of 643 μV_{rms}. In the case of the TSR pixel with a normal structure RST, the measured reset noise is 734 μV_{rms} that is reduced by 28.6% compared to the conventional pixel. The noise reduction ratio is comparable to the simulation result. In the case of the TSR pixel with the asymmetric structure RST, the measured reset noise is further reduced to 607 μV_{rms}, that is 41.0% lower than that of the conventional pixel. This result suggests that the reset noise is reduced by suppressing the injection charge flow from the CS to the RD node. Therefore, it is expected that the TSR pixel with asymmetric RST composed the tapered and half-buried channel can reduce the reset noise further because the number of charge injected to the CS will be lower than that of the simple asymmetric RST implemented.

V. Summary and future work

In order to realize a LOFIC CIS with small SNR drop at the conjunction point between HCG and LCG signals, the TSR pixel circuit, which reduces pixel reset noise without additional transistors in a pixel has been proposed. The LCG reset is conducted by two-step with the additional reset transistor RST' and the reset sampling capacitor CS' located outside the array. The temporal noise on the reset drain RD is frozen with large CS', and the reset noise on the CS is suppressed as long as the charge injected to the CS does not flow to the RD node during the on-to-off transition of RST.

SPICE noise simulation results show that the pixel reset noise is suppressed by 28.3% at t_f = 100 ps. In order to further reduce the noise, the asymmetric RST with tapered and half-buried channel is proposed. According to TCAD simulation result, it is confirmed that the potential difference between the CS and the RD node is reduced. It is expected that results in reduction of injection charge flow form the CS to the RD node.

The test chip of the TSR pixel with a simple asymmetric RST is fabricated with 0.18μm CMOS process. Evaluation results show that the pixel reset noise is reduced by 41.0%.

As future work, we will fabricate a prototype chip of the TSR LOFIC-CIS with the asymmetric RST with tapered and half-buried channel.

VI. Acknowledgments

The VLSI chip in this study has been fabricated in the chip fabrication program of through the activities of VDEC, the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation. This work was also supported through the activities of VDEC, The University of Tokyo, in collaboration with Cadence Design Systems, with NIHON SYNOPSYS G.K. and with Mentor Graphics.

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[1] S. Sugawa, N. Akahane, S. Adachi, K. Mori, T. Ishiuchi, and K. Mizobuchi, "A 100 db dynamic range cmos image sensor using a lateral overflow integration capacitor," in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.* IEEE, 2005, pp. 352–603.

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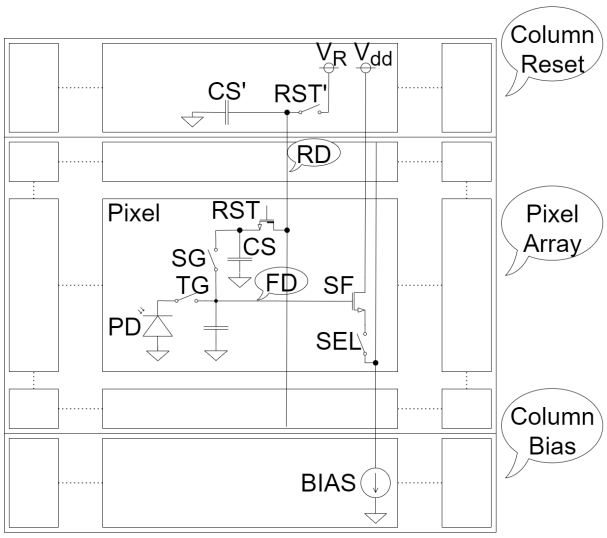
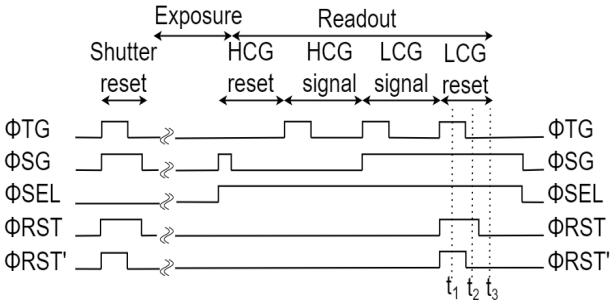
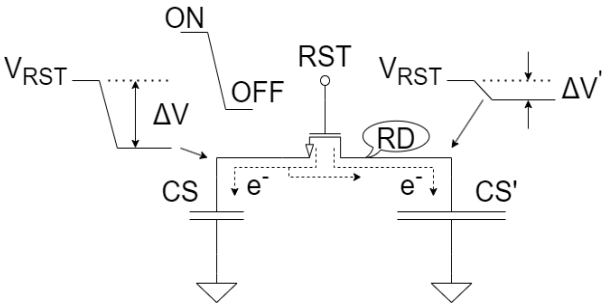


Fig. 1. Schematic diagram of the proposed LOFIC-CIS



(a) Timing diagram of the proposed LOFIC-CIS

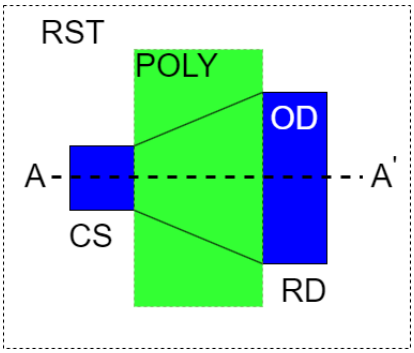


(b) Injected charge to the CS flows to the RD node due to voltage drop difference

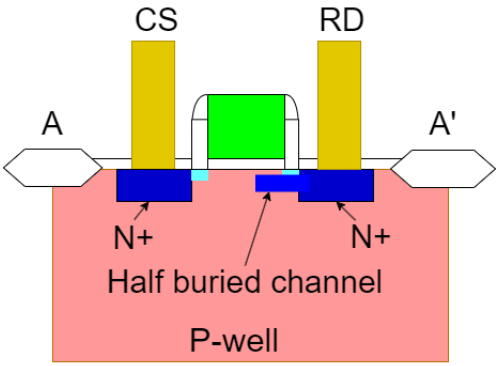
Fig. 2. Timing diagram and injected charge flow

TABLE I
EVALUATION RESULT OF PIXEL RESET NOIES.

	Conventional	TSR (normal)	TSR (asymmetric)
Noise	1028 μV_{rms}	734 μV_{rms}	607 μV_{rms}



(a) Top view of tapered channel



(b) A-A' cross-sectional view of half-buried channel

Fig. 3. Asymmetric structured RST

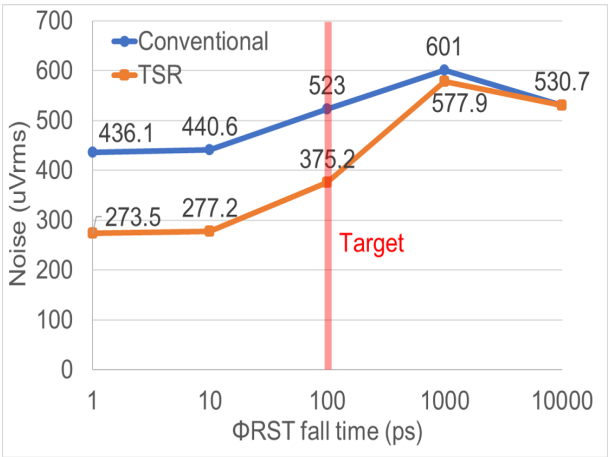


Fig. 4. Transient noise SPICE simulation results

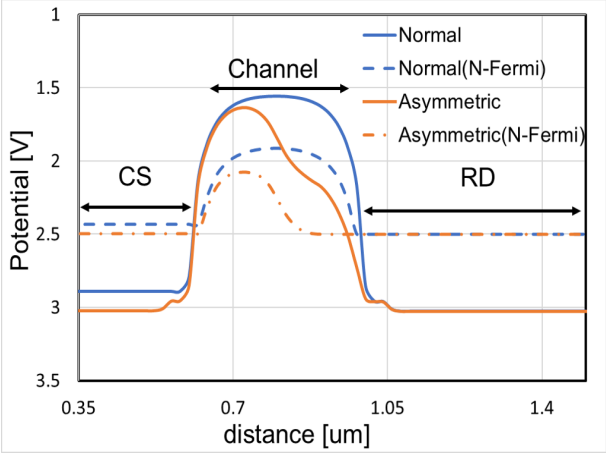


Fig. 5. TCAD device simulation result of asymmetric strcutured RST

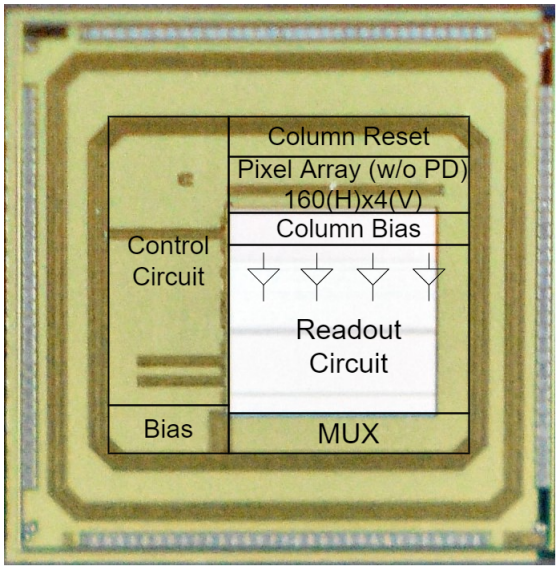


Fig. 6. A photo of the test chip

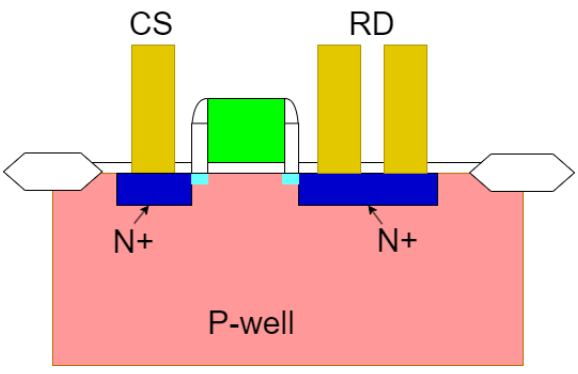


Fig. 7. Alternative simple asymmetric RST with double contacts to the RD node

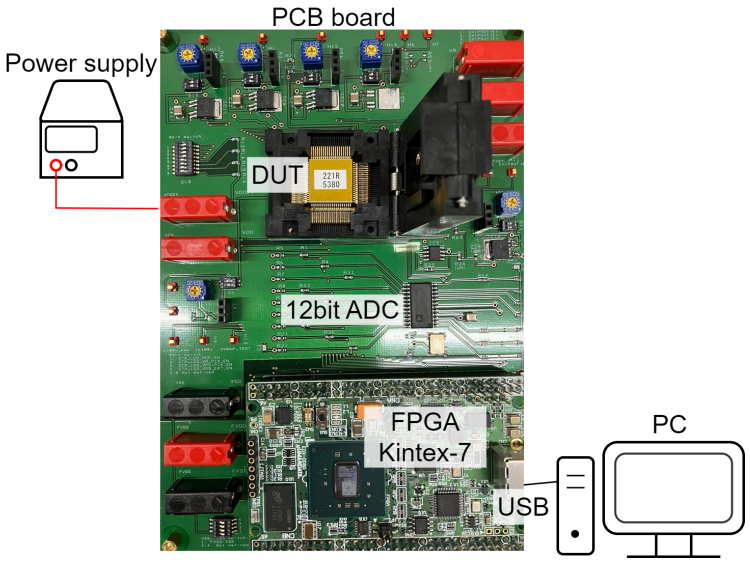


Fig. 8. Measurement setup of the test chip

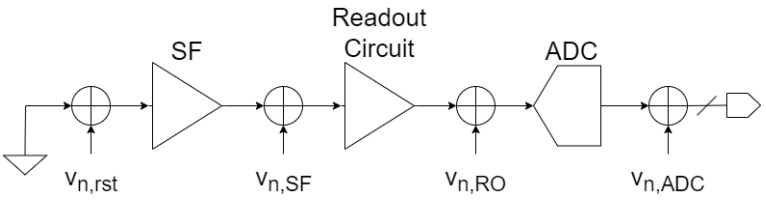


Fig. 9. Reset noise readout chain of the test chip measurement