Self-Powered Ambient Light Sensor Using Energy Harvesting Pixels and Zero Power Communication

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INTRODUCTION

As CMOS technology improves, more efficient devices can be created achieving functionality with ever decreasing power budgets. This has moved to the point where some devices are so low power that they are able to harvest what they require from their surroundings. These energy harvesting sensors can be implemented in a wider system providing functionality with very little power cost. We present one such system, an energy harvesting (EH) ambient light sensor (ALS). This device is a 3D stacked chip where the top tier consists of an array of PV cells to harvest energy from the ambient light and a photodiode sensing cell to provide the ALS measurement. Having both power generation and sensing functionality contained within the same array is possible with deep trench isolation (DTI). The full thickness trench isolation allows each PV cell to be isolated from one another and then connected in series allowing for high voltage generation without the use of charge pumps [1]. By using a back side illuminated process (BSI) both the quantum efficiency (QE) and fill factor are improved. In this case, 3 PV cells are connected in series providing 1.2V to power the device forming the basis for a self-powered ambient light sensor. This sort of sensor has uses in many applications in consumer electronics that already use an ALS and have limited battery power such as wearables and small IoT devices.

POWER BUDGET DERIVATION

Since the ALS has no other voltage source, its power budget is defined by the amount of energy the PV cells can harvest at minimum irradiance. The amount of energy available from ambient light is dependent on the spectra of its source. When defining the power budget for the device, a worst-case of fluorescent light was used. This is because fluorescent light has lower power density compared to other light sources like solar and LED. By integrating the irradiance over the range of wavelengths within the fluorescent light spectra [2], the total power density was found to be 40.4W/m^2. This means that 100 lux of fluorescent light produces 0.297 W/m. The efficiency of the harvesting cells is 10% [3] at low light levels (≈100 lux). The top tier area is defined as 2mm by 2mm with the sensing PV being 10um x 10um.

$$P = F * A$$

P is the power generated, F is the power density of the light source, and A is the cell area. Therefore, the power budget for the chip is 120nW for 100lux of fluorescent light.

ANALOGUE DESIGN

As shown in figure 1, the analogue circuitry on chip is responsible for taking the photodetector measurement of the ambient light and digitising it so it can be serially communicated off-chip. The photodetector itself is forward biased which allows for a higher sensing dynamic range. In this configuration, a voltage signal which is logarithmically dependent on the light level is output and can directly be fed directly into the ADC. The approach to the analogue design on chip was to reduce the power consumption as much as possible which often meant omitting parts that were not strictly necessary to the functionality of the ALS. By having a forward biased photodetector directly connected into the ADC there was no need for a buffer or sample and hold circuitry. Another measure taken to reduce power consumption was to lower the frequency of the clock generated on chip which coupled with using longer transistors meant a reduction in leakage currents.

The 3 PVs in series that make up the supply voltage each produce 0.413V at minimum irradiance of 0.33W/m^2. This figure increases to 0.627V at maximum irradiance of 250W/m^2. The voltage reference generator used was not a bandgap reference circuit as the minimum supply voltage was too low at 1.2V. Therefore, the current and voltage references are derived from the power supply voltage. This means the voltage reference generator output is dependent on light level but the dynamic range of the light incident on the device is high enough that this dependency is acceptable.

The ADC used in this design is a successive approximation register (SAR) ADC using a dynamic latch comparator. This was implemented because the comparator has low static power consumption as it only consumes power during comparisons. When idle, the comparator consumes negligible power. To conserve power, the ADC maximum sampling frequency is 36Hz.

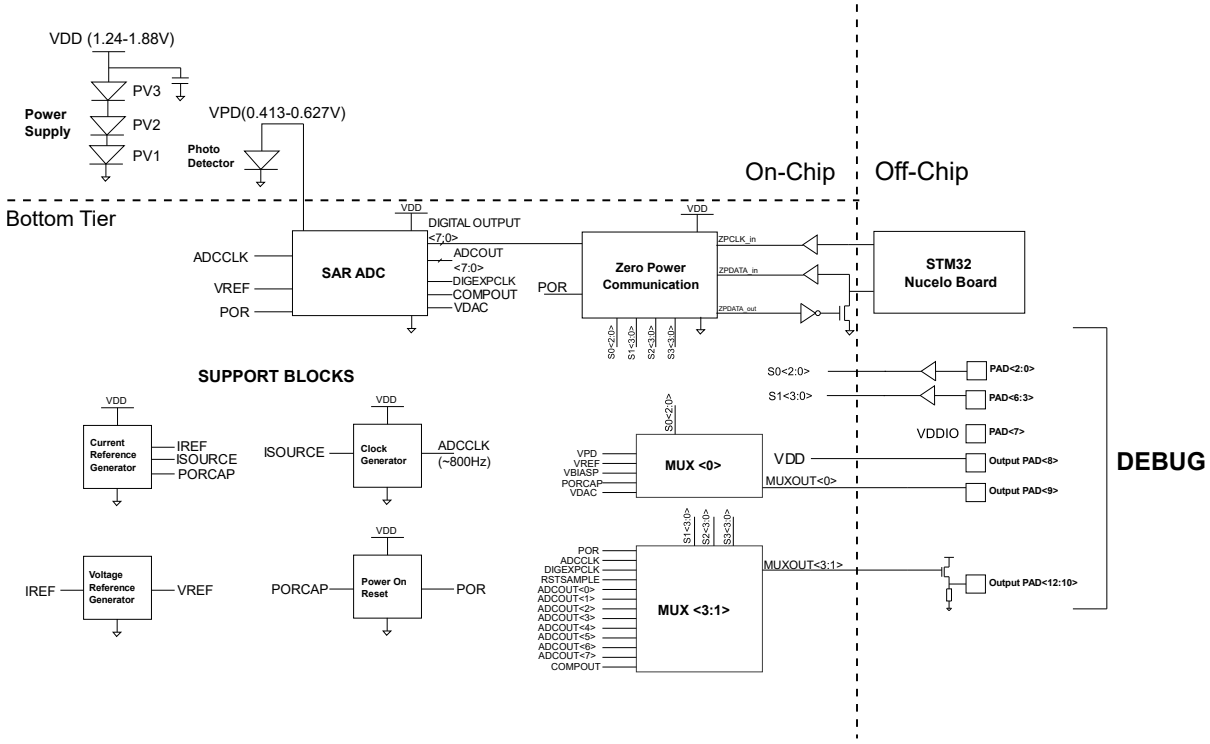

Figure 1: Chip block diagram. Debug pads included for testing.

ZERO POWER COMMUNICATION

The purpose of the digital circuitry in the design is to take the parallel digital output of the ADC, serialise it and then communicate that result off chip. Before this design was created, interfacing with ultra-low power chips was done either very slowly or with custom circuitry on both sides. The aim of this design was to use readily available hardware like an STM32 microcontroller and still be able to communicate with an ultra-low power device at reasonable speeds. Conventionally, I2C or SPI would be used for this task however the power budget restrictions make these protocols unfeasible. The pull-up resistors used in I2C consume power constantly with static leakage that can easily exceed the limited power supply of the low power systems an EH ALS may be included in. SPI requires at least 4 wires to interface between 2 devices, one of which is charged up by the secondary device.

Assuming this MISO wire has 20pF capacitance, if half of the entire chip power budget was used only for charging this wire, with the bits sent consisting of 0s half the time and 1s the other half then the maximum transfer speeds achievable with SPI would be 27.5kbps. Essentially, these existing protocols are not energy efficient enough to be used in realistic ultra-low power systems. MBus [4] was created to address these concerns but requires a considerable protocol overhead and a daisy chained topology that is incompatible with most existing devices.

Therefore, a novel communication bus and protocol has been developed based on I2C that consists of a push-pull clock and active open drain data wires shown in figure 2. This new active open drain configuration replaces pull-up resistors with an inverter connected to the main device. This inverter has much lower static leakage and is used to pull-up the data line. The secondary device can either leave this line high to send a 1 or pull it down to send a 0. The point is that the secondary device does not need to expend energy charging up the data line and so this new protocol is called Zero Power Communication (ZPC). It allows system designers to skew the energy requirement for communication away from the ultra-low power chip and towards a main device supplying both the clock and charging up the data line. An additional benefit to using an inverter as a pull-up mechanism is that it can vary the amount of current that flows through it on the fly. This gives the ability to change pull-up strength dynamically meaning more control over the speed and power consumption of communication. Being able to dynamically change the communication speeds allows for more aggressive power domaining which is important in low-power applications. The ZPC block triggers entirely off the externally provided clock line which means that communication can happen at much faster speeds than the on-chip clock allows.

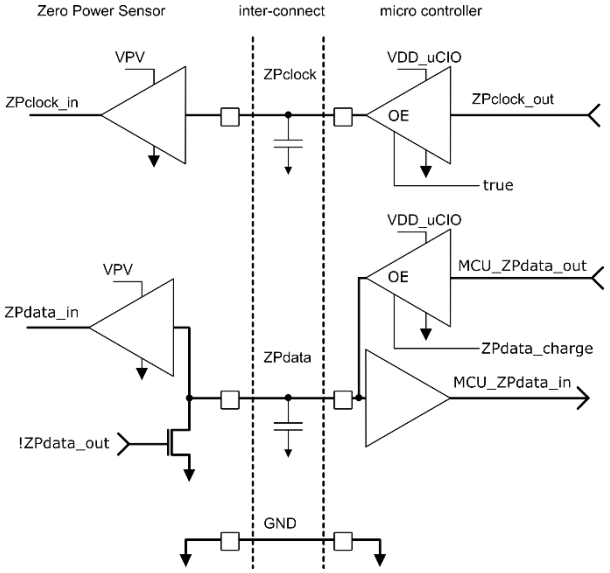

Figure 2: Zero Power Communication Bus

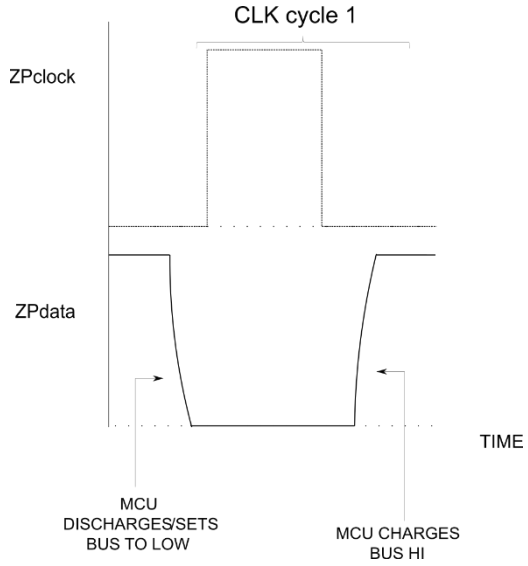

Figure 3: Control bit timing

As shown in figure 3, if the data line is low on the positive edge of the clock, then the secondary device cannot communicate back and so this is defined as a control bit. The control bit is important to both structure the message sent but also define the lengths of fields within it. The novelty of the protocol is that these field lengths can change on a message-to-message basis based on how many successive control bits there are in different parts of the message: the first set of control bits define the length of the payload field, the next set define the length of the device address field, and the final set define the length of the register address field.

In the presented design, there are 2 modes of communication: addressing and non-addressing modes. In the addressing mode, all 3 of the payload, device address, and register address fields are present whereas in the non-addressing mode, the message only contains the payload field and the associated control bits. This is a way of reducing protocol overhead for the most common communication case for an EH ALS – reading out the ambient light measurement. Using the non-addressing mode only a single control bit needs to be sent to the sensor in order to read back an 8 bit ambient light measurement.

By using the control bits to indicate the lengths of each field provides an inherent error checking since both devices are informed of the field lengths before the message arrives. An error in communication cannot be detected using I2C without writing and reading back which consumes valuable power. The ability to change field lengths on a per message basis feeds into the aggressive power domaining now available to system designers: by changing what each number of successive control bits mean in terms of field lengths, common messages can be sent with optimal energy efficiency by resizing the message and having as few wasted bits as possible. Combined with control over how much current is used to pull-up the data line, this protocol promises the most flexibility in communication for the purpose of power efficiency.

RESULTS

At minimum irradiance (0.33W/m^2) the analogue blocks have been simulated to cumulatively consume 17.9nW. The sampling frequency of the ADC at minimum irradiance is 18Hz with the maximum DNL and INL being 1.05 and 1.37 respectively. Ideally both figures would be below 1 but since there are no consecutive code losses, the ADC performance is acceptable. The digital errors are due to variation in the current reference generator affecting voltage reference generator and thus the operation of the ADC. This is due to the variable voltage supply from the PV cells and the aforementioned dependencies of the current and voltage references on this supply.

At minimum irradiance, the ZPC block consumes 84nW with a ZPClock frequency of 50kHz. This figure was found by using accurate power analysis tools on the place and routed digital netlist. In total, the presented design should consume around 102nW at minimum irradiance. The uncertainty of the final power consumption figure is due to the fact that high to low level shifters will need to be implemented between the blocks as the analogue circuitry is in the GO2 domain whereas the ZPC block is in GO1. The ZPC block has been implemented on an FPGA and has been able to communicate with an STM32 MCU with speeds up to 6.8kbps. The bit error rate of ZPC is <1E-6 achieved through validation testing. Finally, the power consumption of ZPC is 8.4pJ/bit which is half the energy consumption of MBus – the current state of the art communication protocol in terms of energy efficiency.

ADC	Architecture	Power Consumption (W)	Output Resolution (bits)	Sample Rate (Hz)	Energy per Code (pJ)
A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Employing a 180nW 64dB SNR Passive ΔΣ ADC [5]	Sigma-Delta	180n	11	3k	5.45
A Low-Power Incremental Delta-Sigma ADC for CMOS Image Sensors [6]	Sigma-Delta	29.5u	10	20M	0.15
A 100nW 10-bit 400S/s SAR ADC for Ultra Low-Power Bio-Sensing Applications [7]	SAR	100n	10	400	25.0
A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- um CMOS for Medical Implant Devices [8]	SAR	53n	10	1k	5.30
SOLAS [9]	SAR	1.4n	6	20	11.67
MIMOSA [10]	Sigma-Delta	11.8n	8	36	40.97
AURORA (This work)	SAR	1.9n	8	20	11.88

Table 1 Comparison of EH and non-EH ADCs

CONCLUSION

The presented work is an example of how an energy harvesting sensor can both conserve power through careful analogue design and interface with conventional devices that do not have such constrained power budgets. It is a promising start but the design needs to be manufactured and characterised before its usefulness can be determined. Mainly, the linearity of the ADC needs to be checked as well as the bit error rate of ZPC. Using ZPC, designers can now offload the energy requirement of communication away from ultra-low power devices towards devices with larger power budgets but the energy for communication still needs to come from somewhere. It remains to be seen if the overall system efficiency of ZPC is an improvement on current methods.

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