A CMOS Image Sensor With 1.6us Conversion Time 10-bits Column-Parallel Hybrid ADC Using Self-Adaptive Charge-Injection Cell

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***Abstract*— This paper presents a 256x256 CIS using the proposed column-parallel hybrid SA-CI-SS ADCs fabricated in TSMC 40nm. The column ADC consumes a total power of 25.6uW@400KS/s at 1.5/1V (SH&Comp / digital&CI) operation. The achieved ENOB is 9.41-bit with a DNL/INL of -0.32/0.49LSB and -0.37/0.62LSB, respectively. The achieved nonuniformity of 256 column ADCs is within 0.22% (standard deviation) and 1.08% (peak-to-peak) with a test input range of 0.8V~1.7V. With a pitch of 4um, this work achieves a 10-bit conversion in 1.6us@25.6uW at a 40Mhz clocking clock and a state-of-the-art FoM of 0.25 um*fJ/c.-s.**

I. Introduction

In recent years, with the Internet of Things (IoT) being widely used in our daily life, the demand of CMOS image sensors (CIS) with high frame rate has also increased rapidly. Therefore, the conversion speed of the analog-to-digital converter (ADC) in the readout circuit of CIS is gradually becoming the bottleneck. The column-parallel single-slope (SS) ADCs [1] are widely adopted due to its small area for column-pitch implementation and high energy efficiency, but the operation speed decreases exponentially with an increased resolution. For high-resolution high frame-rate imaging applications, the required clock frequency is up to GHz range, which causes the burdens of clock distribution and power consumption. To omit the required high-frequency counting clock of SS ADC, several works have been reported [2-4]. The time-stretched (TS) SS ADC [2] implemented a two-step conversion with time residue expansion. However, the required V-T-V converter needs two large capacitors for expansion ratio implementation and thermal noise suppression with the area and power penalty. The time-to-digital converter (TDC) interpolation SS ADCs [3] implemented a delay-chain-generated multiple phase clock for TDC operation, but still needs the high-frequency counting and complex delay calibration. A capacitor array-assisted charge-injection (CI) SAR ADC [4] was reported using coarse-fine CI-arrays for conversion step and energy reduction, however, a complex calibration is required to satisfy the required matching and linearity performance. Moreover, the unit charge of Vth-based CI-cell is sensitive to PVT variation and needs extra reference voltages for CI.

II. Proposed Column-Parallel Hybrid ADC

To address the mentioned issues, this paper presents a column-parallel hybrid ADC using self-adaptive (SA) CI-cell and SS conversion. Compared to the pure SS ADC, the proposed hybrid architecture effectively reduces the conversion cycles (for 10-bit resolution) from 1024 to 64 with a coarse-fine operation, which achieves a significant power reduction by using a 10x slower counting clock of 40Mhz. Compared to the reported CI SAR ADC, the proposed hybrid architecture using SA CI-cell achieves a high conversion linearity in a small area without need of CDAC and weighting calibration. Compared to the conventional Vth-based CI-cell using MOSFET threshold voltage (Vth) [4] for unit-charge control, which suffers from the PVT variation and slow settling, the proposed SA CI-cell achieves a high-speed constant unit-charge injection amount using a feedback circuit and self-adaptive operation. By applying a ramping reference on portion of sampling capacitance for residue's fine SS conversion, the coarse-fine weighting is guaranteed by a local capacitance matching without calibration. To reduce the power consumption and area further, a global double-data-rate (DDR) 6-bit gray code counter is also implemented for SS operation.

A. Chip architecture Overview

Fig. 1 shows the chip architecture of the prototyped CIS and the block and critical timing diagrams of the proposed column-parallel hybrid CI/SS ADC. The column-ADC consists of the sample/hold circuit, SA CI-cell, dual-mode comparator, and CI/SS SRAM for data storage. In the coarse asynchronous CI phase, after the pixel signal (V_{sig}) sampling on the top plate (V_{top}) of sampling capacitor C_T ($=C_L+C_R$), the Vtop is steply ramped down by periodically transferring a constant unit charge Q_{ci} from C_T to C_{ci}. When $V_{top} < V_{ref}$, the comparator output (Valid) triggers and latches the counting code on CI SRAM from the global gray counter operating at a 40MHz counting clock. Then, in

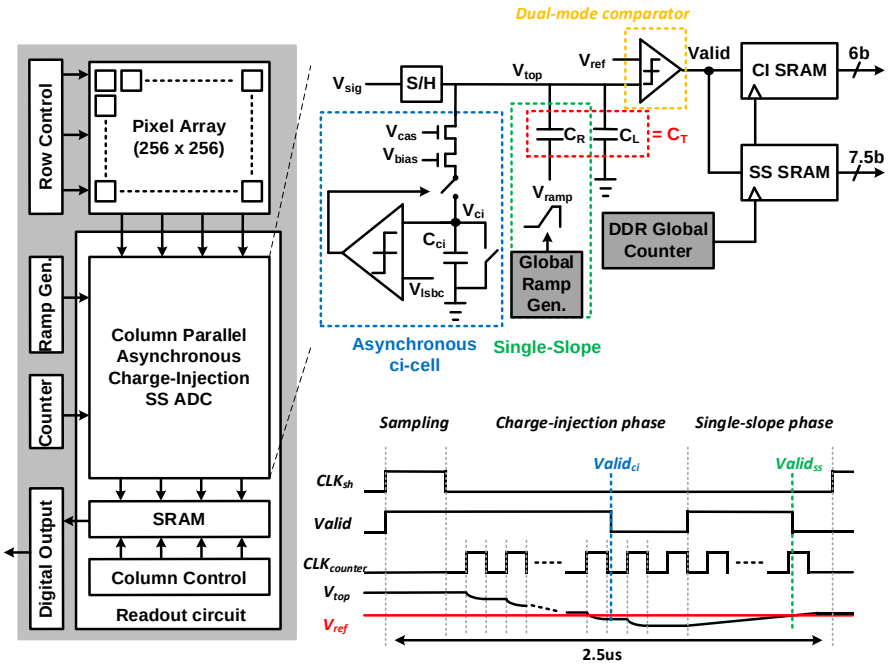

Fig. 1. CIS prototype architecture and the proposed column-parallel hybrid CI/SS ADC.

the fine SS conversion phase, the residue on V_{top} is ramped up by applying a V_{ramp} on the bottom plate of C_R from the global ramp generator. Similarly, when $V_{top} > V_{ref}$, the comparator output triggers and latches the counting code on SS SRAM. With the proposed CI/SS hybrid architecture, the prototyped ADC can finish a 10-bits conversion in 1.6us by reusing a 6-bits DDR gray counter operated at 40MHz.

B. The Proposed SA CI operation

Fig. 2 shows the comparison of the V_{th}-based and proposed SA CI operations. At the beginning with T_{pre} = high, CT is pre-charged to V_{ref}. For each toggling period of "EN" and "inject", a unit charge on CT is transferred to Cci by "EN=1" and then discarded by "inject=1". In the conventional V_{th}-based CI operation, the unit charge is defined as $Q_{ci.Vth} = C_{ci}*\Delta V_{ci}$, where $\Delta V_{ci.Vth} = V_{bias} - V_{th.Mci}$ and is PVT-sensitive and time-variant from the subthreshold settling behavior. The settling accuracy requirement limits the achievable conversion speed, and a complex calibration is necessary for PVT variation. To address the mentioned issues, this work proposes a self-adaptive asynchronous CI-cell using comparator and feedback mechanism to realize a constant unit charge injection amount. The achieved voltage difference $\Delta V_{ci.SA} = V_{lsbc}$ and the corresponding unit charge $Q_{ci.SA}$ are PVT-insensitive, time-invariant, and well-controlled by the closed-loop operation.

The operation of SA CI is explained in detail as follows. During the reset phase with CLK_{ci} = low, the switch SW1 turns off and SW2 turns on to reset $V_{ci.SA}$ = 0. Simultaneously, an auto-zeroing operation (triggered by CLK_{az}) with C_{az} is applied on the

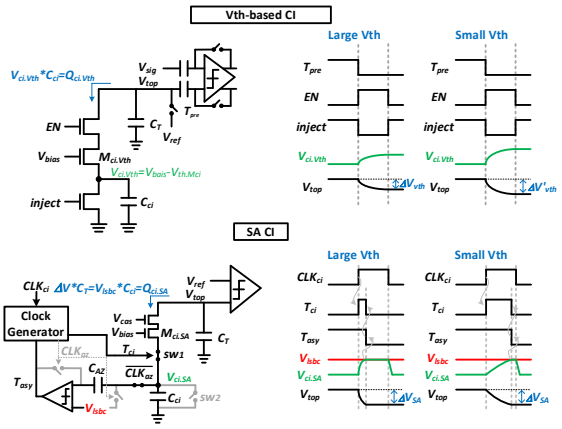

Fig. 2. Comparison of the conventional Vth-based and the proposed SA CI operations.

comparator to eliminate the static offset and reduce the column-to-column gain mismatches. Then in CI phase with CLK_{ci} = high, SW2 turns off and SW1 turns on, the signal charge on C_T is transferred to C_{ci} and increase $V_{ci.SA}$. When $V_{ci.SA} > V_{lsbc}$, the comparator output Tasy flips to pull down T_{ci} and turn off SW1 to finish the unit CI operation. By sensing the voltage difference $V_{ci.SA}$ using comparator instead of V_{th} of MOSFET, the CI operation is asynchronous and self-adaptive to provide a constant unit charge injection amount $Q_{ci.SA} = C_{ci} * V_{lsbc}$. The 5-bits coarse conversion is achieved by repeating the CI operation (Reset and CI phase) 32 times (at most) without consuming any conversion energy by utilizing the signal charge sampled on C_T, and without need of reference voltage. The cascode structure biased by V_{cas} and V_{bias} is implemented to guarantee a constant V_{ds} of

M_{ci} to reduce the $Q_{ci.SA}$ error from the signal-dependent parasitic capacitance of SW1 and improve linearity. The LSB weighting depends on the ratio of C_{ci}/C_T and V_{lsbc}/V_{swing} is configurable, where V_{swing} is the full swing of ADC input range.

C. Fine SS conversion implementation

Fig. 3 shows the fine SS conversion implementation with dual-mode comparator. After the coarse SA CI conversion, the residue on V_{top} is ramped up by applying a global V_{ramp} on C_R. The coarse-fine weighting is guaranteed by the local capacitance ratio matching of C_{ci}/C_R and the global reference voltage ratio of V_{lsbc}/V_{ramp}, which is immune to the column-to-column mismatch of sampling capacitor C_T and achieves a good uniformity without the need of calibration. For a better energy efficiency, a dual-mode comparator is implemented for the dynamic and static comparison operations of SA CI and SS conversions, respectively. Since the crossing point of comparisons in coarse and fine conversions are all at V_{ref}, there is no dynamic offset error. To cover the offset mismatch between dynamic and static comparison operations, 5-bit coarse and 6-bit fine conversions are implemented to get the 10-bit result with a 1-bit redundancy. The column fixed-pattern-noise (CFPN) from the column-to-column offset mismatch of dual-mode comparator can be easily cancelled out using a dark reference calibration.

III. Measurement Results and Conclusion

A 256x256 CIS using the proposed column-parallel hybrid SA-CI-SS ADCs is prototyped in TSMC 40nm. The column ADC consumes a total power of 25.6uW@400KS/s at 1.5/1V (SH&Comp / digital&CI) operation. Fig. 4 shows the measured dynamic and static performance. The achieved ENOB is 9.41-bit with a DNL/INL of -0.32/0.49LSB and -0.37/0.62LSB, respectively. Figure 5 shows the ADC array uniformity performance. The achieved nonuniformity of 256 column ADCs is within 0.22% (standard deviation) and 1.08% (peak-to-peak) with a test input range of 0.8V~1.7V. Figure 6 shows the captured images before and after dark calibration. It shows the CFPN of captured image is successfully cancelled out by a dark frame calibration. Table I shows the comparison table with the state-of-the-art works [1-4]. With a pitch of 4um, this work achieves a 10-bit conversion in 1.6us@25.6uW at a 40Mhz clocking clock and a state-of-the-art FoM of 0.25 um*fJ/c.-s.

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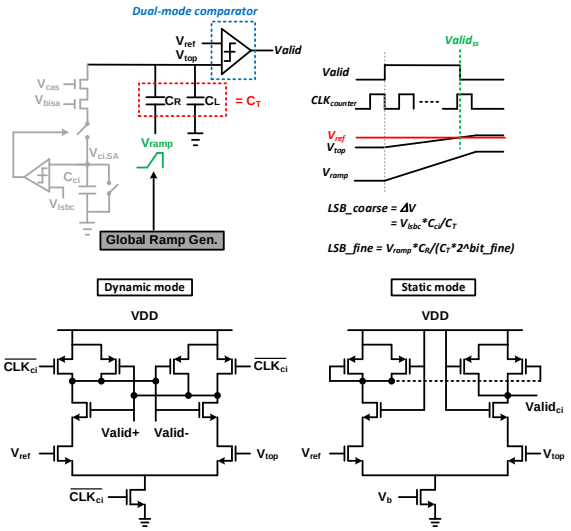

Fig. 3. Fine SS conversion using dual-mode comparator.

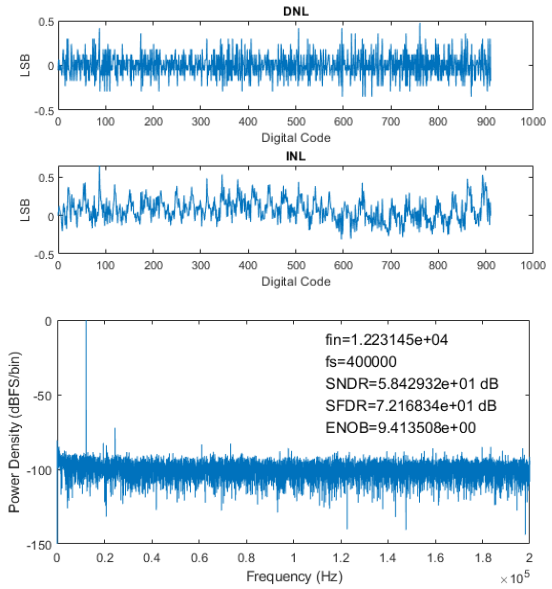

Fig. 4. Measurement results.

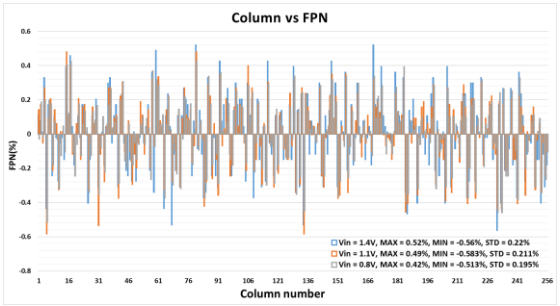

Fig. 5. The measured uniformity of ADC array with an input of 0.8~1.4V

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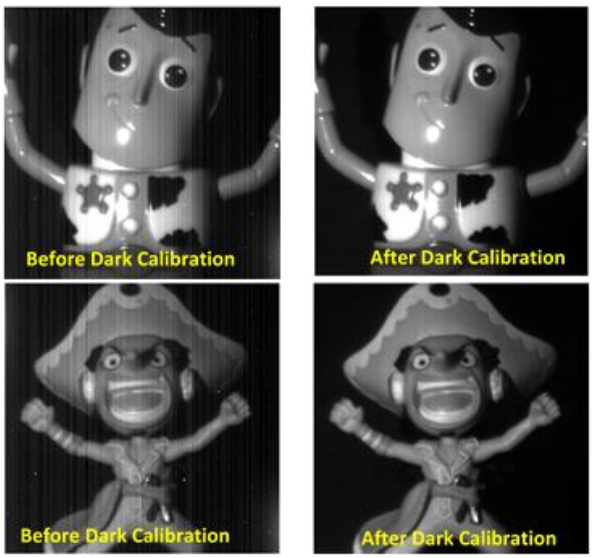

Fig. 6. Captured images before/after dark calibration

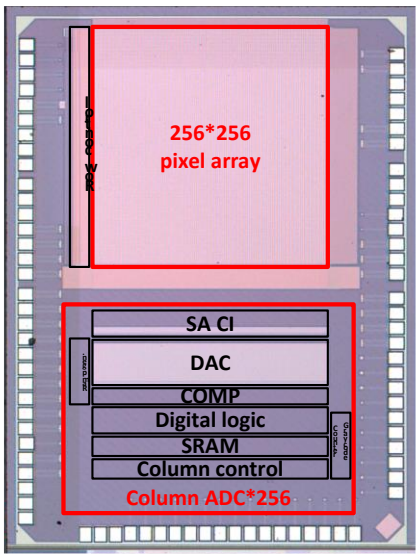

Fig. 7. Chip micrograph.

TABLE I
COMPARISON TABLE WITH STATE-OF-THE-ART WORKS.

	ISSCC 2011 [1]	ISSCC 2019 [2]	TCAS I 2019 [3]	JSSC 2019 [4]	This work
Technology	90nm	110nm	130nm	65nm	40nm
ADC technique	SS	SS/Time-stretched	SS/TDC	SAR/CI	CI/SS
Pixel array	8192*2160	640*480	1024*128	792*528	256*256
Frame-rate (fps)	120	500*	1776*	5.6	1563
1-H time (us)	3.9	4	4.4	370	2.5
Pixel supply (V)	2.9	3.3	3.3	1.7	2.5
ADC supply (V)	2.7/1.2	3.3/1.5	3.3/1.5	1.7	1.5/1
ADC input range (V)	-	0.8	1.5-2.9	0.5	1
Counter clk (MHz)	2376	100	250	-	40
Resolution (bits)	12	10	12	10	10
ADC pitch (um)	4.2	8	5.6	3.1	4
ADC power (uW)/Col	366	98.125	177	0.163*	25.6
FoM (um×pJ/c.-s.)	1.463	3.066	1.064	0.1825	0.25

* Calculated $\text{FoM} = \frac{\text{per column ADC power(uW)} \times \text{ADC pitch(um)} \times 1\text{-H time(us)}}{2^{\text{Resolution}}}$