Charge Demultiplexing for an Ultra-High-Speed Charge-Domain CMOS TDI Image Sensor with a multi-MHz Line Rate

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***Abstract*— Charge demultiplexing for an ultra-high-speed charge-domain CMOS time delay and integration (TDI) image sensor is presented. A proposed charge steering structure enables charges transferred through multiple TDI rows in a column to be demultiplexed to the corresponding sub-column sense nodes (SNs) for parallel processing. After charge demultiplexing, the signal charges in the sub-column SNs are converted in column readout circuits in parallel. This conversion operation is also performed simultaneously while charges in the next TDI rows are transferred and demultiplexed. In contrast to the slow, sequential operation of a conventional CMOS TDI imager, we show that our proprietary charge demultiplexing for parallel processing is a disruptive technology that can increase a CMOS TDI scan speed to an unprecedented level (i.e., multi-MHz) for highly demanding applications.**

I. Introduction

After the successful demonstration of charge-domain TDI imaging using a conventional CMOS technology [1], we have been rapidly displacing our traditional CCD TDI image sensors with CMOS counterparts in various applications such as industrial machine vision [2], DNA sequencing and Earth observation [3]. Especially for Earth observation, our imager is the first space-grade charge-domain CMOS TDI imager launched into orbit in the world to the best of our knowledge. One of the remaining applications that is not accessed with CMOS TDI yet is pattern defect inspection on semiconductor masks and wafers [4], in which ultra-high-speed (i.e., a MHz TDI scan rate) and ultra-high-sensitivity (i.e., a thousand TDI stages) imaging capabilities are essential.

In a conventional CMOS TDI imager, however, a pixel array is read out row by row. This sequential operation limits sensor speed. A maximum TDI scan rate in the current state-of-the-art imager is several hundred kHz [2]. In contrast to the traditional readout, higher speed operation can be achieved by processing multiple TDI rows in parallel. In this work, we present charge demultiplexing for parallel processing for an ultra-high-speed charge-domain CMOS TDI imager.

II. Charge Demultiplexing

Figure 1 shows the block diagram of a column slice of our proprietary charge demultiplexing CMOS TDI pixel array [5]. Here, a single column consists of the m number of active (denoted as white) TDI imaging pixels, out of which the n number of pixels is to be processed in parallel, and the corresponding n number of light-shielded (denoted as gray) sub-column output structures at the end of the pixel array. Not explicitly shown here, the output structure is located at both the top and bottom of the array for bi-directional scanning operation. Each of the sub-column output structures has a charge steering gate (CST) in addition to a typical pixel readout structure such as a SN, a reset, and a source follower.

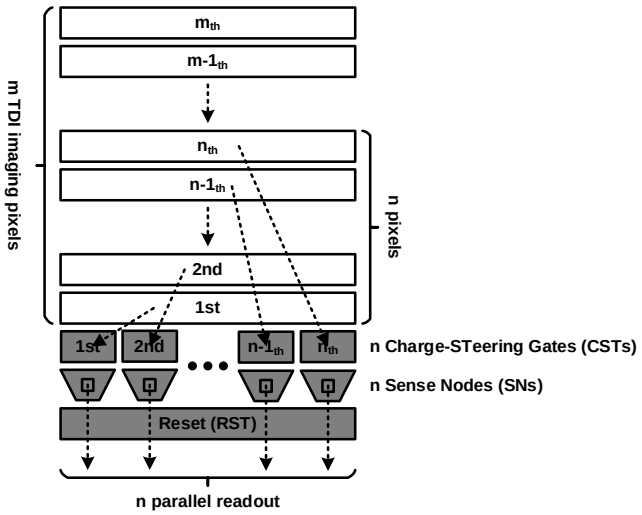


Figure 1. Block diagram of a column slice of the proposed charge demultiplexing TDI pixel array.

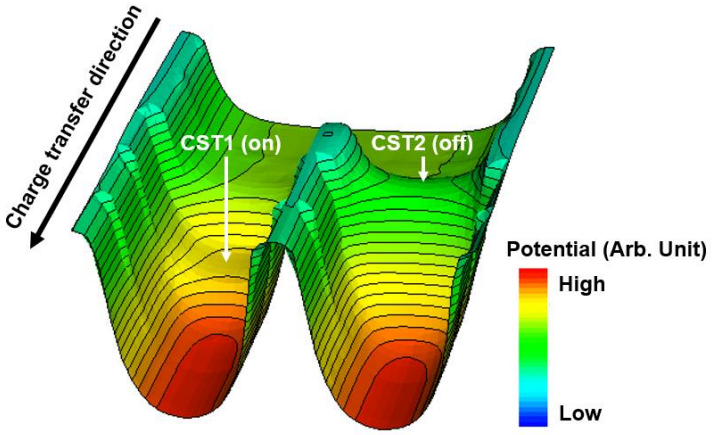


Figure 2. Surface plot of the computed electrostatic potential maximum for 2-row charge steering operation.

The proposed charge demultiplexing is achieved by an operation so-called 'charge steering' which enables each of charges transferred vertically through the n TDI rows in a column to be demultiplexed horizontally to each of the corresponding n sub-column SNs. For this operation, each of the n CSTs in a single row turns on in sequence. Therefore, the CST should be capable of transferring and blocking charge completely when it is ON and OFF, respectively. A surface plot of the computed electrostatic potential maximum of the charge steering structure for 2-row operation is presented in Figure 2. Here, charge is transferred through the CST1 clocked high while blocked by the CST2 clocked low due to a potential gradient and a barrier formed to transfer charge only through the CST1 along the charge transfer direction. As the CSTs are added in the light-shielded region and charge is not stored under it, they will not affect most of the imager performance parameters such as full well capacity, linearity and responsivity. However, the incomplete charge transfer (and also incomplete charge block) will manifest itself as row-to-row charge mixing which will degrade the along-track modular transfer function (MTF) in the TDI operation. This can be confirmed by charge transfer (and also block) efficiency measurements. The test results will be discussed in the next section.

After all charge demultiplexing operations are completed, the signal charges in the sub-column SNs are converted in the corresponding column readout circuits in parallel. This conversion operation is also performed simultaneously while charges accumulated in the next n number of TDI rows are transferred and demultiplexed. The operational timing diagram of 2-TDI row demultiplexing implemented in our test chip is provided in Figure 3(a) in comparison with the diagram of the traditional sequential timing shown in Figure 3(b). In both the diagrams, SHR and SHS are reset and signal sampling periods, respectively, and t1 is a line period. In Figure 3(a), t1 is also a row transfer time, t2 and t3 are transfer periods for the present 2 TDI rows and for the next 2 TDI rows, respectively, and t4 and t5 are AD conversion windows for the signals from the previous 2 TDI rows and from the present 2 TDI rows, respectively. In Figure 3(b), t2 is a row transfer time which is the same duration as t1 in Figure 3(a), which illustrates that the 1-line period is reduced by the proposed parallel processing.

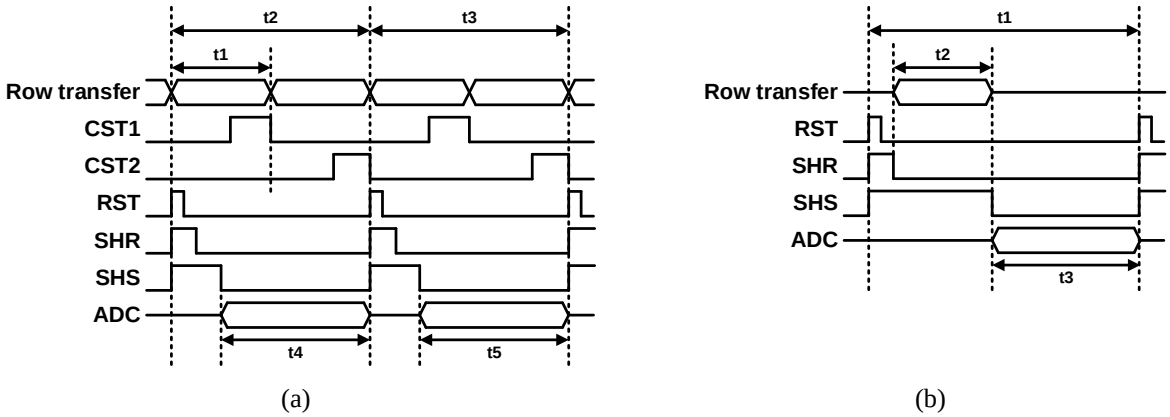
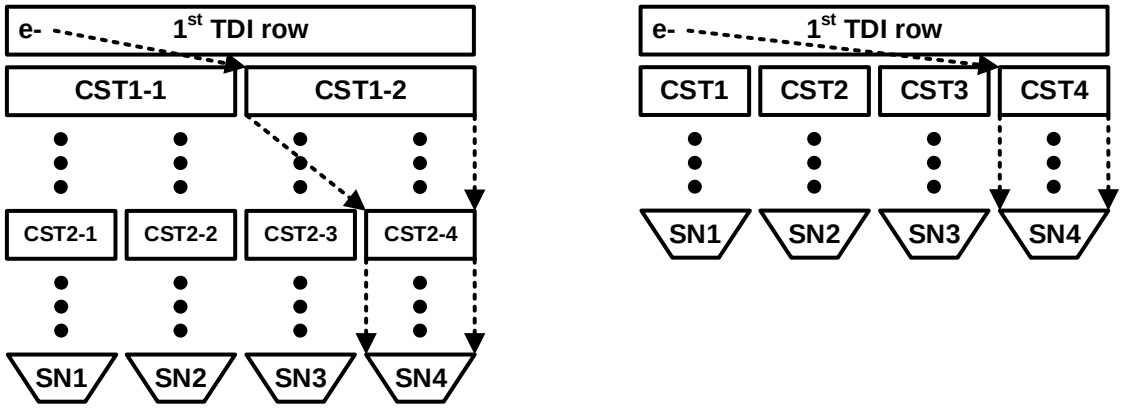


Figure 3. Operational timing diagram: (a) for the proposed parallel processing for 2 rows and (b) for the traditional sequential readout.

The charge demultiplexing operation can be extended to any higher number of rows to be processed in parallel. In real implementation, the 2-row steering can be cascaded repeatedly for better charge transfer. This is illustrated in Figure 6(a) for 4 (i.e., 2 × 2) rows as an example in comparison with direct charge steering without cascading in Figure 6(b). The signal charge (denoted as e-), for example, located at the rightmost corner of the first TDI row should traverse the entire row without cascading as shown in Figure 6(b), where fringing fields that aid charge transfer are essentially non-existent. However, it travels only half the distance in Figure 6(a).



(a) (b)

Figure 6. (a) Exemplary 2 × 2 cascaded charge steering operation and (b) steering without cascading.

The proposed charge demultiplexing increases the TDI scan rate greatly. The expected maximum line rate in 12 bit as a function of the number of parallel-processed TDI rows are calculated for two row transfer times, 200 ns and 400 ns, respectively in Figure 5. With 2-row (each row having a transfer time of 200 ns) parallel processing, a maximum TDI line rate is expected to be over 2 MHz. A line rate of 3 MHz was experimentally confirmed in 10 bits. The detailed test results are presented in the next section.

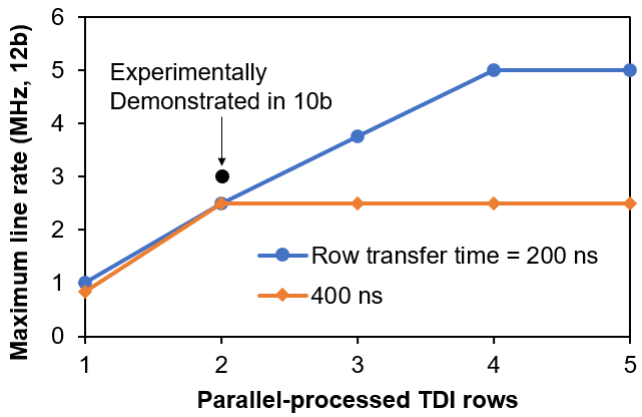


Figure 5. Expected maximum TDI scan rate as a function of the number of parallel-processed rows.

III. Test Results

A test pixel array including various charge demultiplexing structures for the 2-TDI row operation discussed earlier and CMOS peripheral circuits including high-speed pixel drivers and readout circuits were monolithically integrated in the test vehicle using the same 0.18 µm CMOS technology reported previously by our group [1]. Here, the 10-µm pitch active pixels were demultiplexed to two 5-µm pitch sub-columns. To assess the functionality of the proposed charge steering structure, charge transfer efficiency (CTE) was measured using the extended pixel edge response (EPER) method [6] at a transfer speed of 25 ns per transfer as shown in Figure 4, with the signal read out through the CST1 that is clocked high while the CST2 is clocked low. Here, the reduction in the signal of the first and last rows are not due to

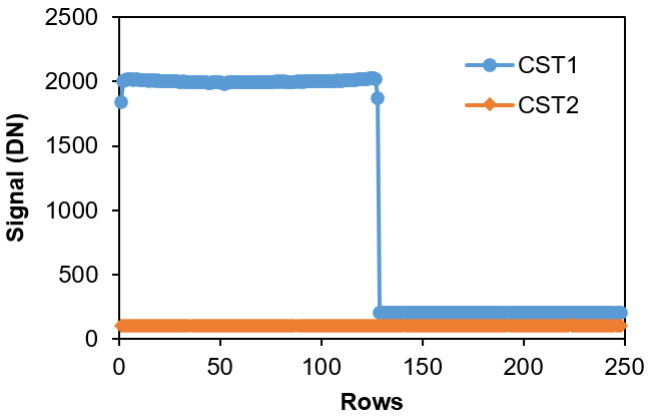


Figure 4. EPER for CTE measurement for the demonstration of charge demultiplexing.

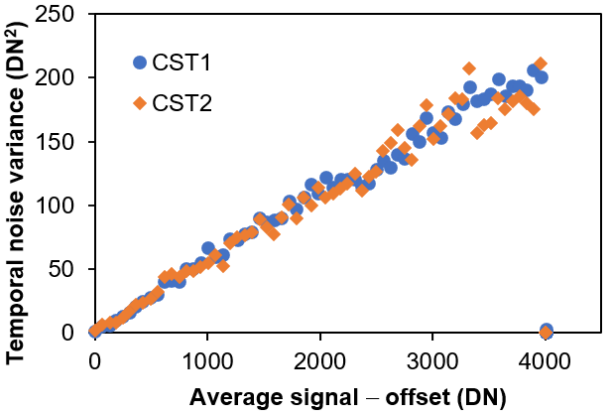


Figure 7. PTC.

incomplete charge transfer but due to the light-shield covering the first and last rows partly. The CTE over 0.99999 per transfer was measured through the CST1 while no charge leaked through the CST2 was detected. This demonstrates that the charge steering structure is capable of demultiplexing charge selectively to a wanted SN while blocking it to the other unwanted SN. The maximum TDI scan rate of 3 MHz was demonstrated experimentally in 10 bits with charge demultiplexing while the other imager performance parameters such as full well capacity, dark current, linearity and responsivity were not compromised. It is worth to note that the noise remains unchanged despite the higher line rate, since the speed improvement is achieved not by increasing the readout speed itself but by performing parallel processing at the same speed. The photon transfer curves (PTCs) for CST1 and 2 signals are presented in Figure 7. The test results are summarized in TABLE I.

TABLE I. Summary of the test results.

Parameters	Unit	Value
Pixel pitch	μm	10 (2 × 5-μm sub-columns)
Maximum TDI scan rate	MHz	3 (demonstrated in 10b)
CTE per transfer	Fraction of 1	> 0.99999
Conversion gain	μV/e-	13
Full well capacity	ke-	> 60
Dark current at 25°C	nA/cm^2	< 4
Non-linearity	%	< 2
Responsivity	DN/(nJ/cm^2)	4971
Noise floor	e-	~20

IV. Conclusion

We have developed charge demultiplexing for ultra-high-speed CMOS TDI imaging in charge domain. A test vehicle has successfully demonstrated a maximum TDI scan rate of 3 MHz without compromising the other imager performance. The ultra-high scan speed enabled by the proposed charge demultiplexing opens the door for highly demanding applications such as ultra-high-speed machine vision, semiconductor mask and wafer inspection, and flat panel display inspection. A charge demultiplexed CMOS TDI image sensor with high resolution is currently being developed, which will be reported in a future publication.

References

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