A Burst Mode 20 Mfps Low Noise CMOS Image Sensor

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Abstract

This paper presents an ultra-high-speed CMOS image sensor utilizing charge-sweep transfer gate technology. This technology eliminates the need for advanced process customization and enables total noise reduction by optimizing the pixel conversion gain.

We have implemented a test chip with a resolution of 64 (columns) by 64 (rows) in a standard 180 nm process and characterized part of its performance. Our testing results demonstrate agreement with theoretical analysis and simulation in areas such as charge transfer time, conversion gain, and readout noise.

Introduction

High-speed CMOS image sensors are widely used in various scientific, industrial, and medical applications. While the current state-of-the-art image sensors reported in literature achieve over 100 million frames per second (Mfps) through process customization [1,2,3,4], this approach can be prohibitively expensive for small-volume customers, and accessing fabrication process modifications can be challenging, especially during the COVID-19 pandemic. Moreover, high-speed CMOS image sensors are prone to higher noise due to the trade-off between the design requirement for fast readout speed, which favors smaller capacitance, and lower thermal noise, which necessitates larger capacitance. In [5], the lowest state-of-the-art input-referred noise was reported to be 8.4 *e-* rms.

This paper introduces a methodology for optimizing charge transfer time and the concept of charge-sweep transfer gates. We demonstrate that these techniques can be implemented using a standard 180 nm process and enable a CMOS image sensor to achieve over 20 Mfps frame rate. We also discuss optimizations for the floating diffusion, in-pixel correlated double sampling (CDS) circuitry, and memory array, which further reduced the input-referred noise without degrading the frame rate.

The structure of the paper is as follows: in the first section, we describe our approach to designing the photodiode and transfer gates. Then, we discuss the circuitry for in-pixel CDS and the memory array. Finally, we present the results of the characterization and analyze their limitations.

Photodiode Optimization

From the perspective of charge transportation, it is well-known that electrons can achieve a higher velocity in a strong electrical field. To leverage this, we propose creating a lateral electrical field along the charge transfer direction in the pixel. Equation 1 from [7,9] provides a simplified relationship between the maximum electrostatic potential (ψ) in a photodiode, the elementary charge (q), the doping concentration of the photodiode (N_D), the doping concentration of the substrate (N_A), and the photodiode half width (X_n). By adjusting X_n parabolically, a constant electrical field can be established [1,7] from the tip of the photodiode to the transfer gate, as described by Equation 2, where x and y stand for the coordinates of the photodiode finger. To achieve an optimal trade-off between pixel fill factor and charge transfer time, we implement and simulate several different photodiode designs in TCAD, as depicted in Figure 1 [8]. Our results, summarized in Table 1, show that the E800 (800 V/cm) design outperforms the others. Therefore, we select this design for the rest of the pixel finger design.

$$\psi_{max} \approx \frac{q \cdot N_D \cdot X_n^2}{2 \cdot \varepsilon_0 \cdot \varepsilon_r}\left(1 + \frac{N_D}{N_A}\right) \quad (1)$$

$$y = -\frac{q \cdot N_D \cdot x^2}{2 \cdot E \cdot \varepsilon_0 \cdot \varepsilon_r}\left(1 + \frac{N_D}{N_A}\right) + C_0 \quad (2)$$

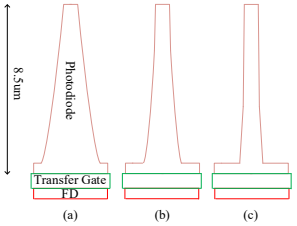

Figure 1*. Sample pixel layouts*

Charge Transfer Time of Different Photodiodes					
CTE	90%	99%	99.5%	99.9%	Unit
E400	10.2	41.2	51.3	75.2	ns
E500	0.67	17.4	25.8	47.0	ns
E600	0.67	5.01	11.0	28.3	ns
E700	0.74	1.51	5.16	19.3	ns
E800	0.82	1.18	3.78	15.5	ns

Table 1. *Charge transfer time of different photodiode designs*

Charge-sweep Transfer Gate

One may observe that the transfer gate in the sample pixels depicted in Figure 1 has a comparable width to the pixels. As a result, when dealing with large pixels, such as 20 µm * 20 µm, the transfer gate width is also around 20 µm. This will result in a considerable floating diffusion node area [8] and a reduction in pixel conversion gain. As shown in [6], the conversion gain is estimated to be less than 10 µV/*e-* for a 20 µm pixel. To address this issue, we propose utilizing charge-sweep transfer gates (TX3, TX2, and TX1), as depicted in Figure 2. Each gate features a smaller geometry size than the prior one, resulting in a smaller floating diffusion node, as highlighted in the red rectangle.

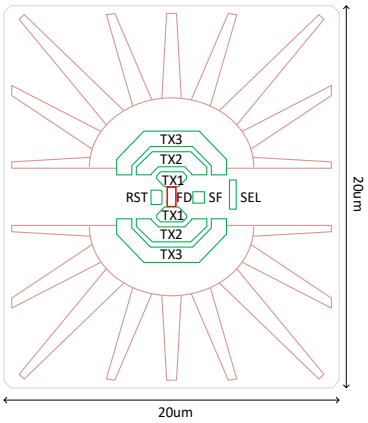

***Figure 2**. High-speed pixel layout based on charge-sweep transfer gate*

In a 180 nm process, the typical gap between two poly gates is 0.2 µm ~ 0.3 µm. We developed two timing sequences to achieve complete charge transfer from the photodiode to the floating diffusion node without using a double poly gates process or implementing special doping beneath the transfer gates. Figure 3 depicts the two timing sequences.

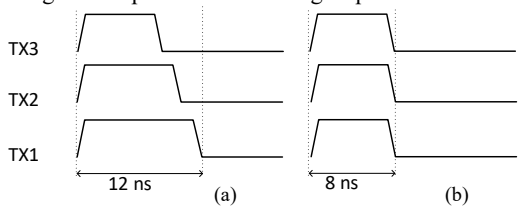

***Figure 3.** TX gates timing for charge-sweep transfer gates*

In timing sequence a), TX1's On voltage is slightly higher than that of TX2, and TX2's On voltage is slightly higher than that of TX3. At the start of the charge transfer, all three gates, TX1, TX2, and TX3, are turned on. As the charge transfer comes to an end, TX3 is the first to turn off, followed by TX2, and finally, TX1. Considering the rise and fall time of the TX pulses, the complete charge transfer sequence takes 12 ns in simulation.

In timing sequence b), the On voltage of TX1 is considerably higher than that of TX2, and the On voltage of TX2 is significantly higher than TX3. This removes the potential barrier between the adjacent gates while they are turned on. Initially, all three gates, TX1, TX2, and TX3, are switched on during charge transfer, and then all three gates are turned off simultaneously when charge transfer is complete. The complete charge transfer sequence is simulated to take only 8 ns.

Floating Diffusion Node Optimization

For a typical floating diffusion, self-alignment technology allows the N+ implant to fully cover the transfer gate and floating diffusion, leaving no gap in between, which facilitates charge transfer. However, for pixels with charge-sweep transfer gates, complete charge transfer can only be achieved after all gates have been fully turned off. Therefore, it is safe to move the floating diffusion away from the TX1 gate and create a gap in between [10,11], as depicted in Figure 4. This can effectively reduce the parasitic capacitance overlap between the floating diffusion node and TX gate and further improve the conversion gain.

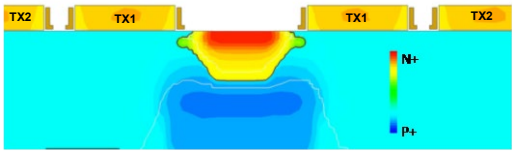

***Figure 4.** Cross-section of the doping profile of floating diffusion node*

Pixel Source Follower

The analysis of the capacitance distribution at the floating diffusion node was conducted, as depicted in Figure 5, which revealed that the gate-to-drain capacitance ($C_{fd\_sf\_gd}$) and gate-to-ground capacitance (C_{fd_gnd}) of the source follower dominated. To enhance the pixel conversion gain, the high-conversion-gain (HCG) variant removed the lightly-doped drain (LDD) on the drain side [12] and decreased the gate length from 0.6 µm to 0.3 µm, as shown in Figure 6. TCAD simulations demonstrate that the modification resulted in an increase in the pixel conversion gain from 138 µV/*e*- to 174 µV/*e*-.

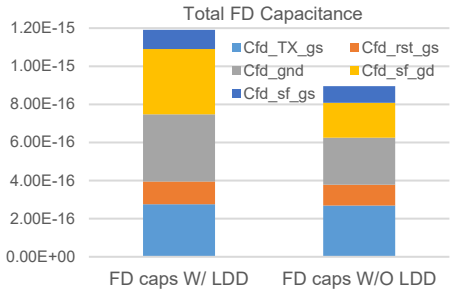

***Figure 5.** Capacitance distribution of baseline pixel (left) and HCG pixel (right)*

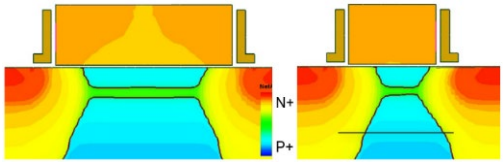

***Figure 6.** Cross-section of the doping profile of SF in baseline pixel (left) and HCG pixel (right)*

In-Pixel CDS Circuitry

Similar to many CMOS image sensors, the flicker and thermal noise of the pixel's first stage source follower (SF) typically dominate the input-referred noise. Without altering the standard fabrication process or incorporating advanced interface passivation, correlated double sampling (CDS) remains a useful method for decreasing low-frequency thermal noise and flicker noise.

To account for the voltage gain attenuation introduced by the CDS circuit, we are implementing the circuit shown in Figure 7 in this pixel [13]. Specifically, we are placing the C_{SH} at the output of the first-stage source-follower instead of the input of the second-stage source-follower, as described in [1,5]. This configuration allows us to reduce the voltage attenuation in the signal chain to $C_{CDS}/(C_{CDS}+C_P)$, where C_{CDS} stands for the AC CDS capacitor, and C_P is the parasitic capacitor.

The following section will provide details of the 1.8 V thin gate sample/hold capacitor bank. To protect the 1.8 V thin gate devices in a 3.3 V environment, the V_{RST} voltage is isolated from the V_{DDpix} and can be adjusted autonomously, with V_{RST}

usually set to 1.8+V_{GS_SF2}. This configuration guarantees that the SF2's maximum output voltage stays below 1.8 V.

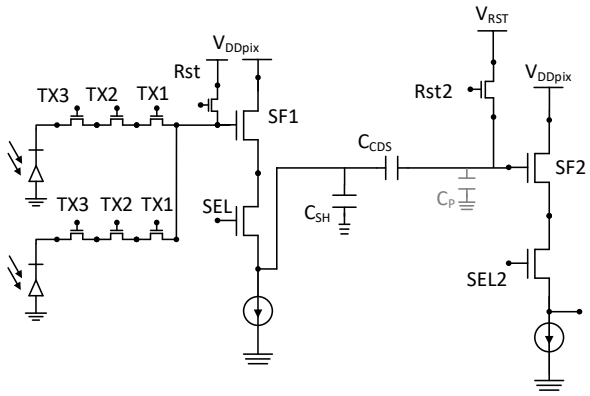

Figure 7. *In-pixel CDS circuit*

Sample/Hold Capacitor Unit

For design simplicity and durability in a 3.3 V operating environment, it is preferable to use thick gate 3.3 V devices. However, the difference in dielectric layer thickness leads to a lower capacitance density of 3.3V NMOS capacitors, which typically ranges from 0.25 to 0.5 of that of 1.8 V thin gate NMOS capacitors, and an increase in thermal noise. To overcome this challenge, this pixel utilizes 1.8 V NMOS capacitors in the sample and hold capacitor bank.

To achieve a higher capacitance density, a custom Metal-1 (M1) Metal-Oxide-Metal (MOM) capacitor is installed on top of the poly gate of the NMOS capacitor. Moreover, a Metal-2 (M2) layer acts as a shielding layer positioned above the M1 MOM capacitor, as depicted in Figure 8. By implementing this design, we were able to fit 108 units of sample and hold capacitors (each with a capacitance of 78 fF) into a 52 µm pixel in the final layout.

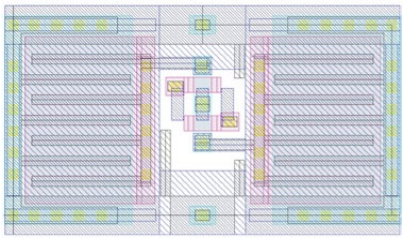

Figure 8. *The layout of in-pixel Sample/Hold unit*

Top Chip Power Distribution

One of the challenges involved in designing a burst mode CMOS image sensor pertains to the power distribution network. In particular, during the pixel resetting phase, a significant amount of instantaneous current is necessary to reset both the floating diffusion node and CDS capacitors. If the supply network has high resistance, temporary collapses on the supply rails may occur and take time to recover. To reduce routing resistance, the power and reference rails associated with pixels are placed on the top thick metal layer in the layout and are star-connected to all four sides of the pad ring. Figure 9 highlights these connections, which are enclosed by red boxes.

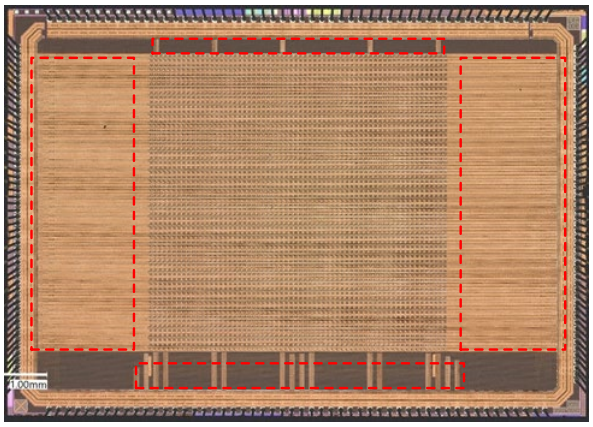

Figure 9. *Microscope Image of the sensor*

Test System and Measurement

Despite demonstrating in [6] through TCAD simulation that the sensor is capable of operating at 20 Mfps, the current prototype test system is constrained by the hardware capabilities of the FPGA, prototype PCB, and chip carrier, which restricts reliable operation to a maximum of 15.6 Mfps. The prototype system utilizing a CPGA-208 package and a zero-insertion-force (ZIF) socket introduces parasitic inductances that cause significant ringing on the power supply during pixel reset operations. This ringing can result in CDS errors and increase noise if the power supply and reference voltage have not fully settled before the end of CDS sampling. Increasing the CDS reset pulse (Rst2 in Figure 7) width can suppress this artifact, but it also reduces the frame rate of the sensor. Hence, to achieve optimal noise performance, we conducted the remaining measurements at a frame rate of 4 Mfps.

The total output noise was measured for both the baseline pixels and high-conversion-gain (HCG) pixels, as depicted in Figure 10. The baseline pixels exhibited a noise level of 10.9 DN at the sensor output, which is equivalent to 8.7 *e-* rms at the input. In contrast, the HCG pixels were expected to have higher flicker noise due to the smaller in-pixel source follower gate area. However, the short CDS period canceled out the majority of the noise, resulting in a total output noise of 12 DN, which is equivalent to 5.1 *e-* rms at the input, as shown by the silicon measurement.

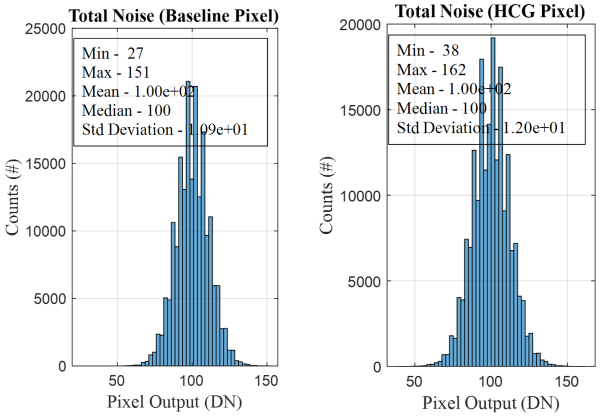

Figure 10. *Total noise measurement result for baseline pixel (left) and HCG pixel (right)*

In Figure 11, the Photon-Transfer-Curve (PTC) was measured for both pixel types. The measured data, adjusted by the voltage gain of 0.485 V/V across the entire signal chain and ADC LSB 38 µV/DN, indicates that the baseline pixel has a conversion gain of 98 µV/*e*-, whereas the HCG pixel has a conversion gain of 183 µV/*e*-.

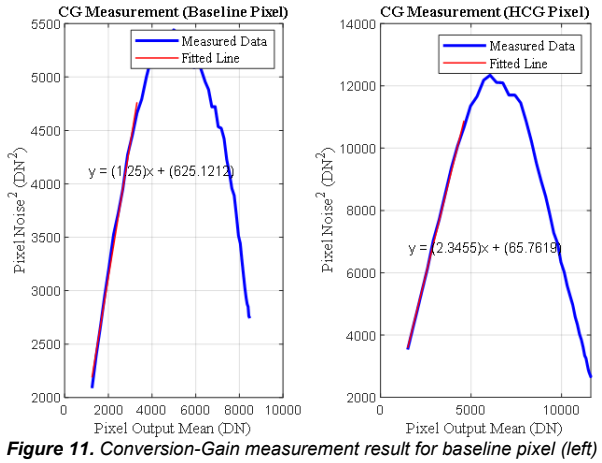

Figure 11. *Conversion-Gain measurement result for baseline pixel (left) and HCG pixel (right)*

The image lag test was conducted on both the baseline and HCG pixels, and Figure 12 shows the results. The measurements reveal that the baseline pixel has a negligible lag (<0.1%). On the other hand, the HCG pixel displays an approximately 3% lag, which is due to overflow at the floating diffusion node.

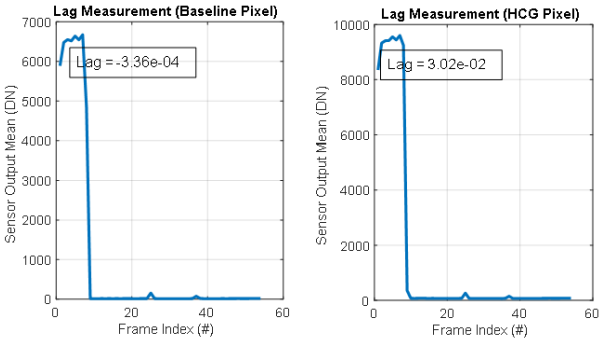

Figure 12. *Lag measurement result for baseline pixel (left) and HCG pixel (right)*

Conclusion

The initial characterization results indicate that the use of a charge-sweep transfer gate can enhance the pixel conversion gain and decrease the input-referred noise. Unfortunately, due to time constraints, certain measurements, such the quantum efficiency, were left incomplete before the paper submission deadline. Nonetheless, we aim to present supplementary test findings in future research.

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References

[1] Suzuki, M., Sugama, Y., Kuroda, R., & Sugawa, S. (2020). Over 100 million frames per second 368 frames global shutter burst CMOS image sensor with pixel-wise trench capacitor memory array. *Sensors*, *20*(4), 1086.

[2] Tochigi, Y., Hanzawa, K., Kato, Y., Kuroda, R., Mutoh, H., Hirose, R., Tominaga, H., Takubo, K., Kondo, Y., & Sugawa, S. (2013). A global-shutter CMOS image sensor with readout speed of 1-tpixel/s burst and 780-mpixel/s continuous. The IEEE Journal of Solid-State Circuits, 48(1), 329–338.

[3] Dao, V. T. S., Ngo, N., Nguyen, A. Q., Morimoto, K., Shimonomura, K., Goetschalckx, P., ... & Etoh, T. G. (2018). An image signal accumulation multi-collection-gate image sensor operating at 25 Mfps with 32× 32 pixels and 1220 in-pixel frame memory. Sensors, 18(9), 3112.

[4] Mochizuki, F., Kagawa, K., Okihara, S. I., Seo, M. W., Zhang, B., Takasawa, T., ... & Kawahito, S. (2016). Single-event transient imaging with an ultra-high-speed temporally compressive multi-aperture CMOS image sensor. Optics express, 24(4), 4155-4176.

[5] Wu, L., San Segundo Bello, D., Coppejans, P., Craninckx, J., Süss, A., Rosmeulen, M., Wambacq, P., & Borremans, J. (2018). Analysis and design of a CMOS ultra-high-speed burst mode imager with in-situ storage topology featuring in-pixel CDS amplification. *Sensors*, *18*(11), 3683.

[6] Yue, X., & Fossum, E. R. (2023). Simulation and design of a burst mode 20Mfps global shutter high conversion gain CMOS image sensor in a standard 180nm CMOS image sensor process using sequential transfer gates. Electronic Imaging, 35, 1-5.

[7] Takeshita, H., Sawada, T., Iida, T., Yasutomi, K., & Kawahito, S. (2010, January). High-speed charge transfer pinned-photodiode for a CMOS time-of-flight range image sensor. In Sensors, Cameras, and Systems for Industrial/Scientific Applications XI (Vol. 7536, pp. 235-243). SPIE.

[8] Cao, X., Gäbler, D., Lee, C., Ling, T. P., Jarau, D. A., Tien, D. K. C., ... & Bold, B. (2015). Design and optimisation of large 4T pixel. In Proc. Int. Image Sensor Workshop (IISW) (pp. 112-115).

[9] Park, S., & Uh, H. (2009). The effect of size on photodiode pinch-off voltage for small pixel CMOS image sensors. Microelectronics Journal, 40(1), 137-140.

[10] Chen, S., Ma, J., Hondongwa, D. B., & Fossum, E. R. (2017). High conversion-gain pinned-photodiode pump-gate pixels in 180-nm CMOS process. IEEE Journal of the Electron Devices Society, 5(6), 509-517.

[11] Ma, J., & Fossum, E. R. (2015). A pump-gate jot device with high conversion gain for a quanta image sensor. IEEE Journal of the Electron Devices Society, 3(2), 73-77.

[12] Kusuhara, F., Wakashima, S., Nasuno, S., Kuroda, R., & Sugawa, S. (2016). Analysis and reduction technologies of floating diffusion capacitance in CMOS image sensor for photon-countable sensitivity. ITE Transactions on Media Technology and Applications, 4(2), 91-98.

[13] De Wit, Y., Walschap, T., & Cremers, B. (2010). U.S. Patent Application No. 12/766,798.