

Chip-level Performance Analysis using Test Element Group Devices for indirect Time-of-Flight CMOS Image Sensor

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We developed Test Element Group (TEG) module to analyze image characteristics of Indirect Time-of-Flight (iToF) pixel. It is difficult to figure out the cause of image degradation, since iToF pixel has more complicated structure compared to conventional 4T CIS pixel. Therefore, it is needed to analyze iToF sensor not only with the chip-level image, but also with single pixel device. In this paper, we developed TEG device, which consists of electric potential curve, C-V curve, and charge pumping method. In addition, we also showed correlations between TEG and chip-level image results.

Indirect Time-of-Flight (iToF) uses 4-sampling method with Global Shutter (GS) operation to calculate depth information of an image. For this operation, multiple devices including MOSCAP storage are connected in a chain structure. Due to the complex structure, it is difficult to define the cause of image degradation, so device-level analysis is needed. In addition, since both operation and structure of iToF are different from 4T CIS, the approach using conventional TEG cannot be used in our sensor. In this work, we designed TEG devices to figure out image characteristics suitable for iToF sensor.

We propose new TEG device designed for iToF pixel structure and operation. Figure 1 shows unit pixel schematics and timing diagram of iToF. First, turn on the Overflow Gate (OG) during the global reset operation time to empty the photodiode (PD). Then, during the integration time, the photogate (PG) is toggled for modulation, and the photoelectron is transferred by Transfer Gate (TGA), and stored under the Storage Gate (SG). After that, read out the floating diffusion (FD) signal by turning SG OFF and TG1 ON [1].

Figure 2 (a) shows the potential of each device during modulation. Shut-off (S/O) and maximum voltage (Vmax) under each device determines the performance of iToF pixel, for example, the Full Well Capacity (FWC). To obtain these electrical potentials, we applied current bias to the source node, and observed change of the source voltage by increasing TGA or TG1's voltage [2-3], an example is shown in figure 2 (b). The measured S/O voltage and Vmax with different SG voltage is shown in figure 3. We also compared the chip-level FWC result and TEG potential measurement. Both measured chip-level FWC and calculated TEG FWC are increased as SG voltage increases. This states that we can predict FWC with TEG measurement.

Figure 4 shows the capacitance of MOSCAP obtained with conventional C-V curve measurement. The operating frequency of PG is 100 MHz, and SG is held at high voltage to store photoelectron during integration time until readout operation. Therefore, we categorized the source of dark current into PG and SG components. At low frequencies and low voltage, the capacitance decreases with increasing temperature. This indicates that the charge at the interface traps becomes more likely to de-trap with increasing temperature. On the other hand, at high frequencies and high negative voltage, the capacitance increases as the temperature increases because the probability of charge tunneling into the border trap inside the oxide increases. In this way, we separated the trap component of each device. Also, we calculated the total trap density using the conventional charge pump measurement method. [4-5]

In addition, TEG can be used to predict global reset operation. As illustrated in figure 5, 3 chip-level data with different process condition shows different amount of overflowing charges from PD to SG. It is confirmed that the S/O voltage of OG is lowered in the TEG data under the process condition where the amount of overflow charge increased. This shows that the TEG and the chip-level results are correlated.

We correlated the chip-level dark current and TEG result. First we designed devices with different SG sizes, and compared the number of traps calculated from TEG charge pump measurement and chip-level dark current. Figure 6 (a) illustrates the correlation between chip-level dark current and the number of traps calculated from

TEG. Next, maximum capacitance (C_{max}) measured from TEG also be correlated with dark current in chip-level in different process condition. As shown in figure 6 (b), we confirmed that the number of border traps is increased through TEG C-V measurement, and is related to the increase of chip-level dark current.

References

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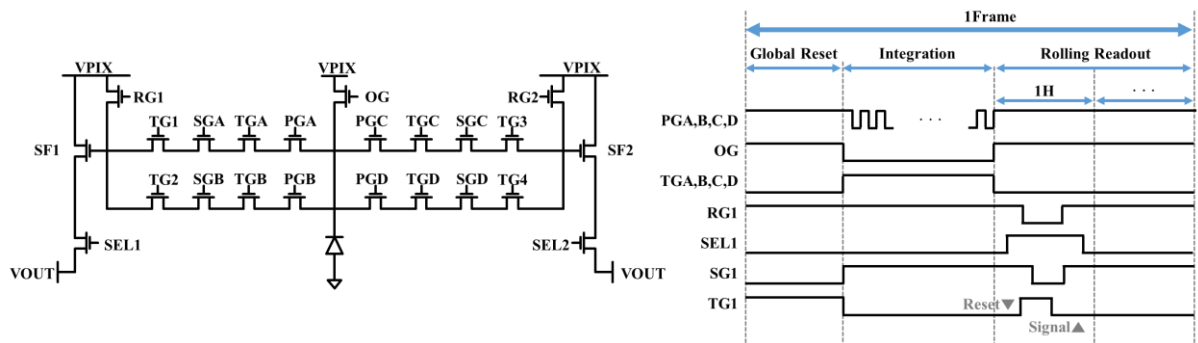


Figure 1. Schematics and timing diagram of 4-tap iToF unit pixel

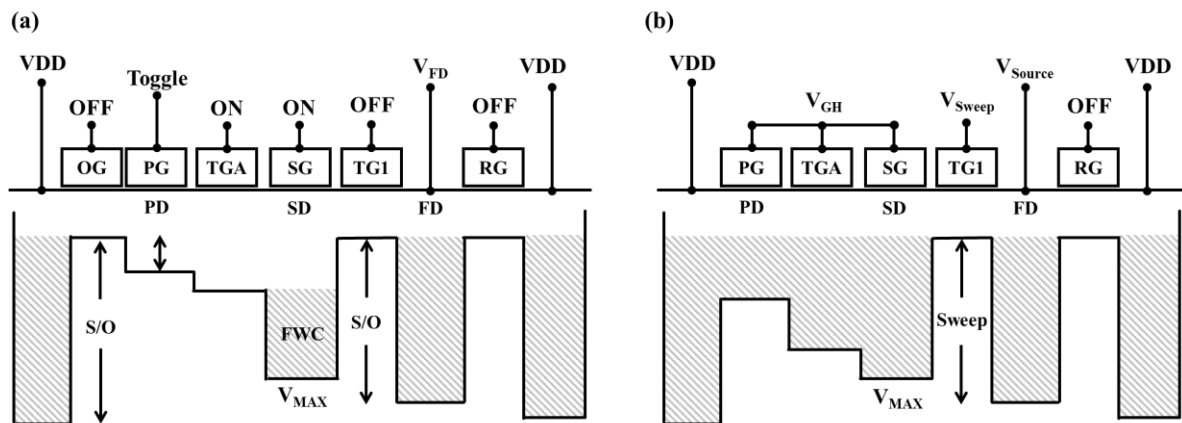


Figure 2. (a) Potential diagram of iToF in modulation (1 of 4 taps is shown)
 (b) Measurement setup for TG S/O voltage in TEG device

