Near Infrared Quantum Efficiency Simulations for CMOS Image Sensors

Andrew Perkins
Intelligent Sensing Group
onsemi
Nampa, ID USA
andrew.perkins@onsemi.com

Swarnal Borthakur
Intelligent Sensing Group
onsemi
Nampa, ID USA
swarnal.borthakur@onsemi.com

***Abstract*— This paper presents results of 3D finite-difference-time-domain (FDTD) simulations for predicting Near Infrared (NIR) Quantum Efficiency (QE) of complementary metal oxide semiconductor (CMOS) image sensors. JMP statistics software [1] and Lumerical FDTD [2] simulation software were used to setup and analyse a Central Composite Design (CCD) design of experiment (DOE) with factors of pixel pitch varying from 1.5um to 3.5um, epitaxial silicon substrate thickness varying from 3um to 8um, and number of inverted pyramids per pixel varying from 1 to 36. NIR QE at wavelengths of 850nm and 940nm is predicted and compared to products on the market. Factors to further increase NIR QE are also discussed.**

Keywords—near infrared, quantum efficiency, inverted pyramids, CMOS image sensor

I. Introduction

Near Infrared (NIR) quantum efficiency (QE), specifically at wavelengths of 850nm and 940nm, is becoming increasingly important in CMOS Image Sensors (CIS). The need for enhanced NIR QE is driven by multiple markets: the security market wants to reduce the power consumption of active light emitting diodes (LED) illuminants; the automotive market wishes to employ NIR in-cabin monitoring for driver awareness, and aid in advanced driver assistance systems (ADAS) detection of objects at night; the industrial market wants NIR for automated inspection with enhanced contrast under low-light conditions and improved spectral information; and the consumer markets need NIR for facial recognition, depth detection, and internet of things (IoT). The current NIR QE of standard CMOS image sensors (~3um epitaxial silicon thickness) without any NIR enhancement structures is 18%/9% at 850/940nm respectively, but NIR QE of up to 60%/40% at 850/940nm is now needed to stay competitive, with QE of 70%/50% at 850/940nm desirable.

To keep manufacturing costs low, silicon remains the substrate of choice, compared to Germanium or III-V substrates. Silicon substrate enables the use of existing CMOS manufacturing techniques. However, silicon is an indirect bandgap semiconductor and has a weak absorption coefficient of <0.1 um^{-1} in wavelengths >800nm. This means the Si thickness needs to be at least 23um thick to achieve 70% QE at 850nm wavelength, and 38um thick to achieve 50% QE at 940nm wavelength as shown in Fig.1. Current costs and manufacturing make such a thickness impractical, especially for backside illumination (BSI) image sensors. This means a solution beyond simply increasing the silicon substrate thickness must be utilized. NIR light scattering structures are a way to effectively increase the absorption path length.

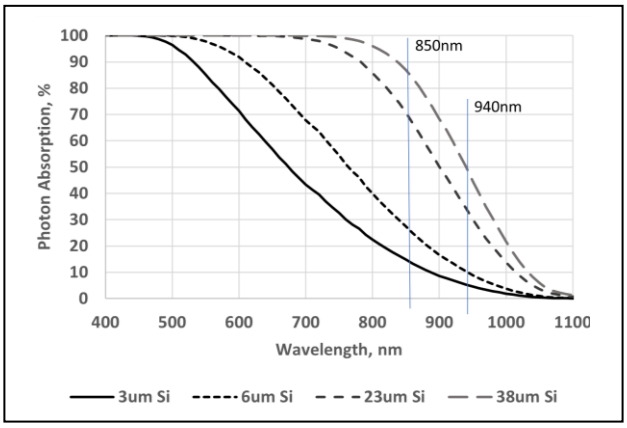


Fig. 1. Photon Absorption at silicon thicknesses of 3um, 6um, 23um, and 38um (based on absorption coefficient data [3])

II. CMOS Image Sensor with NIR Light Scattering Structures

BSI has enabled integration of light scattering surfaces directly on the silicon surface where light enters the pixel. CIS manufacturers have increased NIR QE by incorporating light scattering structures like refractive inverted pyramids (IVP) or diffractive trenches on the silicon surface.

A. Inverted Pyramids (IVPs)

IVPs are formed using a wet etch process that follows the (111) crystalline plane of silicon. This results in fixed relationship of pyramid width and height, and an etch angle of ~54.7° when etched in a (100) silicon surface. Because the wet etch slows on the (111) silicon crystal plane, the orientation of the wafer notch relative to the crystal orientation is important to consider. Depending upon the wafer notch orientation relative to crystal orientation, an IVP will etch with walls parallel to the pixel (square) if the notch is at <110> direction, or with pyramid walls at an angle to the pixel (diagonal) if the notch is at <100> direction. This can impact the pyramids layout and scattering effectiveness.

B. Diffractive Trenches

Diffractive trenches are formed with a dry etch process during backside processing and are typically ~100-200nm wide with a depth of 400-1000nm. A dry etch requires an annealing to reduce the damage to silicon surface during the dry etch. The geometry is largely guided by subwavelength

diffractive physics. The geometry and layout of trenches are not limited by the crystal orientation like IVPs.

C. *Other relevant structures*

Other structures such as microlens, color filter array (CFA), anti-reflective coating (ARC) films, backside or frontside trench isolation (BDTI/FDTI), and metal structures and circuitry can impact NIR QE as shown in Fig. 2. These other structures can lead to further optimization of NIR QE.

Table 1 shows a sample of NIR enhanced CIS with a variety of pixel pitches, silicon thicknesses, and NIR scattering structures. When considering the design of an image sensor, it would be helpful to be able to estimate what NIR QE to expect. Comprehensive three-dimensional Finite-Difference-Time-Domain (FDTD) simulations along with design are used to model NIR QE response as a function of pixel pitch, silicon thickness, and IVP layout.

III. Simulations

3D Finite-Difference-Time-Domain (FDTD) optical simulations using Lumerical [2] software with relevant geometry and material properties is used to simulate NIR QE.

The importance of how NIR scattering structures play a role in NIR QE can be seen in Fig. 3 which shows the QE results of a 3D FDTD simulations for an image sensor with 2um pixel pitch, 6um silicon thickness, and 4um backside deep trench isolation (BDTI). The simulations include results for no NIR scattering structures, IVP in a diamond configuration, IVP in a square configuration, and trenches in a 'star' configuration.

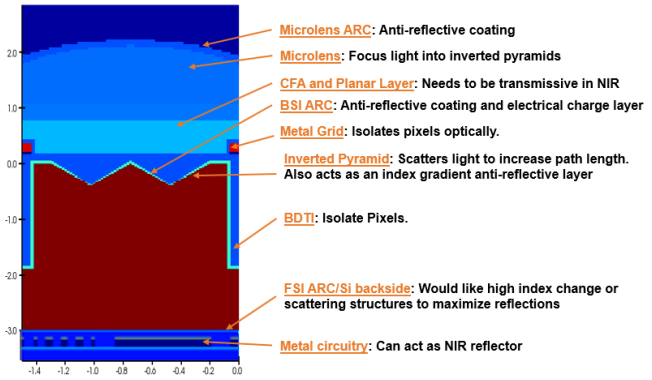
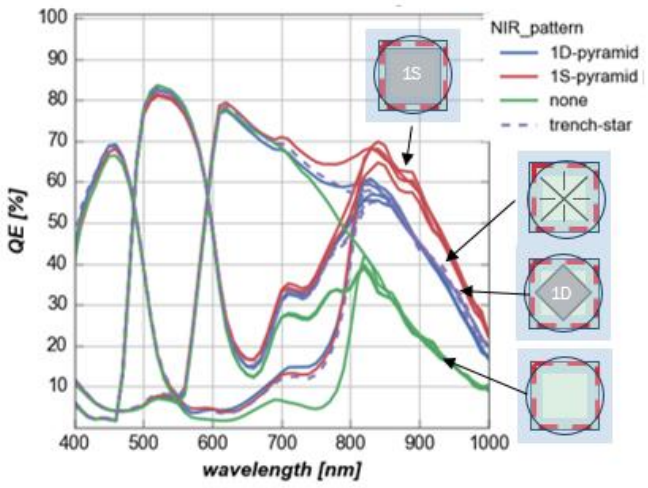


Fig. 2. 3D FDTD simulation cross-section with important structures for NIR QE



		QE%				
NIR type	NIR width [nm]	850nm	940nm	Blue	Green	Red
1S: Square IVP	1414	66	44	68	82	79
1D: Diagonal IVP	910	56	35	69	82	77
trench-star	120	57	37	69	83	78
None	0	33	16	66	84	78

Fig. 3. Simulated QE for 2um pixel pitch, 6um Si thickness, 4um BDTI depth with various light scattering structures

IVPs and trenches can have similar NIR QE performance. It can be seen from Fig.3 that an IVP oriented in a diamond configuration (1D), and trenches in a star pattern have similar NIR QE. However, if the pyramid is etched in a square configuration (1S) then NIR QE increases due to more light entering the pyramid and being scattered more effectively. This study will focus on IVPs in a square orientation.

IV. DOE and Results

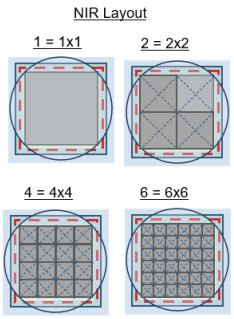
JMP software is used to develop a modified Central Composite Design (CCD) design of experiment (DOE) with factors of pixel pitch (1.5um to 3.5um), NIR layout (1 to 6 IVPs per pixel side), and silicon thickness (3 to 8um). Fig. 4 shows the DOE values with the simulated NIR QE results, and illustrations of how IVPs are laid out.

TABLE I. Sample of Image Sensors with NIR Surface Scattering Structures

	Sony IMX332[4]	**SmartSens SC5035 [4]**	**OmniVision 0S05A20 [5]**	**OmniVision OS02C10 [4]**	**Samsung (Conference) [6]**	**Sony IMX462 [4]**	**onsemi AR0830 [7]**
Date Announced/Published	2017	2017	2018	2020	2020	2021	2022
Pixel Pitch (um)	1.12	2.0	2.0	2.9	2.3	2.9	1.4
Si Thickness (um)	3.5	2.4	3.6	6	8	6	6
BDTI depth (um)	2 (backside)	1.6 (backside)	2.1 (backside)	4 (backside)	8 (frontside)	2 (backside)	4 (backside)
NIR type	IVP	IVP	Trenches	IVP	Trench-Star	IVP	IVP
NIR Width (nm)	400	770	160	580	170	400	900
NIR Depth (nm)	236	545	410	360	1000	236	636
# NIR Structures per pixel	4	4	9	16	1	36	1

Pixel_Pitch (um)	NIR_Layout	Si thk (um)	850nm QE%	940nm QE%
1.5	1	3.0	48.3	30.9
		5.5	60.9	35.0
		8.0	64.5	44.1
	2	3.0	43.2	25.7
		8.0	63.2	37.7
	4	5.5	33.2	16.6
	6	3.0	18.2	9.6
		8.0	33.7	18.0
2.5	2	8.0	60.8	40.8
	4	3.0	48.0	26.4
		8.0	60.7	39.5
	6	5.5	43.3	23.4
3.5	2	3.0	60.4	35.5
		8.0	66.8	46.7
	4	5.5	58.4	41.0
	6	3.0	53.2	26.3
		8.0	65.9	40.8

a)



b)

Fig. 4. a) Modified Central Composite Design of Experiment with results of NIR QE. b) NIR pyramid layout

A least squares fit analysis was run in JMP to determine the important factors. Fig. 5a shows the important factors (p-value <0.05) are pixel pitch, silicon thickness, NIR_layout, and the interaction term of pixel pitch and NIR_layout. The prediction profiler and interaction profiles as shown in Fig. 5b,c can be used to estimate NIR QE with pixel pitch, number of NIR pyramids, and silicon thickness as inputs.

In general, the following observations can be made:

1) NIR QE increases linearly with pixel pitch. This is to be expected as absorption path increases due to lateral scattering of light.
2) Single large pyramids are preferred over a greater number of smaller pyramids. As the width of pyramid increases it becomes easier to focus into the pyramid and more light is effectively scattered. Pixel pitch plays a role in the practical size and layout of IVPs.
3) As expected, NIR QE increases with silicon thickness. For example, given a 2um pixel pitch and four IVPs, the expected QE@940nm for 3um Si thickness would be 29%, and for 6um Si thickness QE@940nm would be 36%. For a target of 40% QE@940nm then 7.4um of Si thickness would be needed.

In this study the microlens size and shape was a fixed function of pixel pitch. Further NIR QE improvement is possible by optimizing the microlens for each specific pixel pitch and NIR layout.

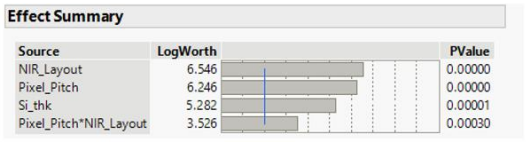
V. Conclusions

3D FDTD simulations and DOE can provide guidance and insight when estimating NIR QE for an image sensor for a given pixel pitch, NIR layout, and silicon thickness.

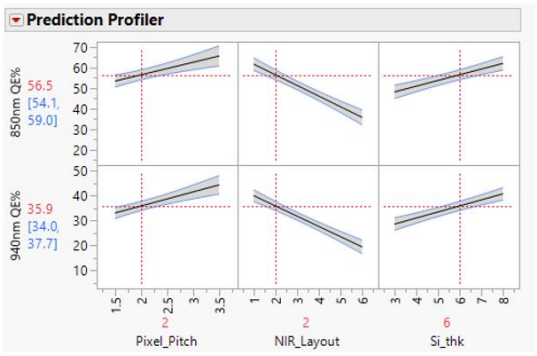
Acknowledgment

The help of Marc Sulfridge and Byounghee Lee is greatly appreciated.

a)



b)



c)

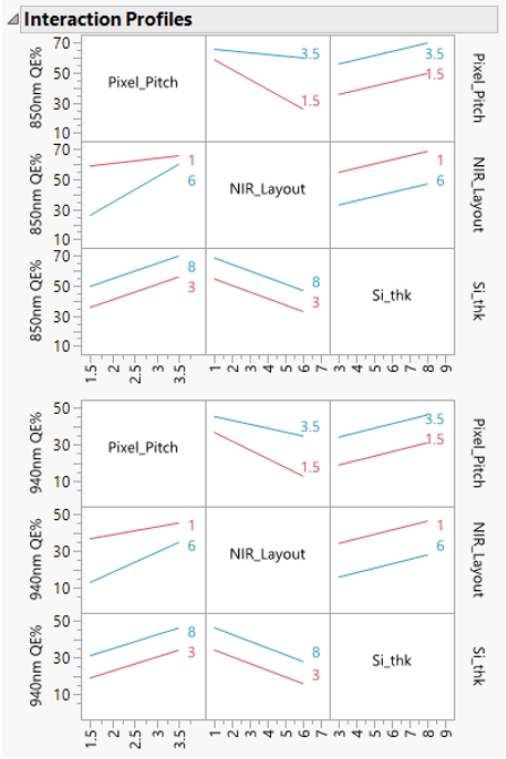


Fig. 5. A) Least squares fit. b) prediction profiler c) interaction profiles for NIR QE based on pixel pitch, NIR layout, and silicon thickness

References

[1] JMP 14.3. SAS Institute Inc., Cary, NC, 1989-2021.

[2] ANSYS Lumerical FDTD, Release 2022R1.4

[3] Martin A. Green, 'Self-consistent optical parameters of intrinsic silicon at 300 K including temperature coefficients', *Solar Energy Materials and Solar Cells* **92** (11), pp.1305-1310, (2008)

[4] Tech Insights, 2021 Image Sensor Device Essentials (DEF) Annual Seminar. 2021.(BRF-2201-808)

[5] TechInsights, OmniVision OS05A20 Device Essentials Plus Summary. DEP-1810-801. 2018.

[6] J. -K. Lee *et al.*, "5.5 A 2.1e⁻ Temporal Noise and −105dB Parasitic Light Sensitivity Backside-Illuminated 2.3µm-Pixel Voltage-Domain Global Shutter CMOS Image Sensor Using High-Capacity DRAM Capacitor Technology," *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 102-104, doi: 10.1109/ISSCC19947.2020.9063092.

[7] O. Skorka, S. Micinski, A. Perkins, B. Gravelle, X. Li, R. Ispasoiu, "1.4um pixel, 8MPixel, thick epi image sensor for RGB-IR imaging," 2021 International Image Sensor Workshop, 2021, R32.