A hybrid, back-illuminated image sensor for high QE visible and infrared detection

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Abstract — For future space science and earth observation missions, the need for an image sensor with a high quantum efficiency over a wide band was identified. Having separate substrate for the detecting layer and the readout circuit allows for better optimization of the property of the substrate. The solution presented here is to have a thicker, back-side illuminated silicon die for the detector layer so that high QE can be achieved in a wide band, extending from visible to the near infrared.

In this paper we present the design of a 1Megapixel, BSI hybrid image sensor, which comprises of a detector and a CMOS readout integrated circuit (ROIC) layers. The detector was also manufactured in a modified CMOS image sensor technology. Test results of the detector and initial test of the ROIC will be presented.

I. Introduction

Most CMOS image sensors are fabricated on wafers with a thin epitaxial layer (~a few µm), which provides the sensing substrate. This selection matches well the requirements of vision applications, but it limits the quantum efficiency, especially for longer wavelengths. For space and earth observation applications, the specifications are driven by the need for high-efficiency over a wide band. This means it is possible to use a single sensor for many applications, thus limiting weight, power consumption and complexity, which are at premium in embarked instruments.

A hybrid detector (Figure 1) allow to separately optimise the sensing and the readout layers. For the former, the silicon photodetector array (SiPDA), we selected a 100 µm thick silicon substrate, while for the latter a CMOS readout integrated circuit (ROIC) was developed. The two are connected together by bump bonding and can then be mounted in a standard package.

The format of the hybrid array is 1040x1040 or 1 megapixel, with a pitch of 20 µm.

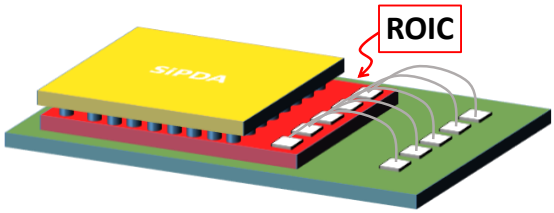

Figure 1. Artistic view of the hybrid sensor

II. The Silicon Photodiode Array

The target process for the SiPDA is a modified 110nm CMOS (LF11IS) process [1]. As a substrate we used a low dark current, high resistivity (>2kOhm cm), float zone, 100 µm thick substrate with a backside p+ implantation and Anti-Reflective Coating. The mask set for the SiPDA is limited to only a few layers, which are going to define the implants for the pixel, together with contacts and one metal layer for the connections (Figure 3). Around the pixel array, guard rings are integrated and the outermost ring is used to bias the substrate: the bias voltage is transferred to the backside p+ layer through the non-depleted peripheral volume of the sensor chip. In this way, no back contact is needed. As shown in Figure 1, the SiPDA is slightly smaller than the ROIC, so all biases are provided through dedicated pads on the ROIC and routed to corresponding pads for bump bonding to the SiPDA. The guard-ring and the substrate contact geometry were defined by TCAD simulation to make smooth transition of the silicon

[1] L. Pancheri et al., A 110nm CMOS process with fully depleted high resistivity substrate for NIR, X-ray and charged particle imaging, Proceedings of the 2019 International mage Sensor Workshop, Snowbird Resort, USA, June 24-27, 2019

electric field from the pixels to the substrate contact. For the pixels, we consider different options for the N+ implants and the P+ isolations, as well as different geometries. In the simulation, we considered the parameters listed in Table 1. A simulation of the expected transmission and quantum efficiency for the sensor with the selected ARC and 100µm thickness is shown in Figure 4.

The megapixel array was divided in twelve subarrays, each with a variant of the design. In order to avoid breakdown of one structure to disrupt the correct functioning of their neighbours, guard-rings were inserted in between the subarrays. Stand-alone test structures were also designed to allow early characterisation of the pixel parameters. The manufactured wafer, together with a zoom to the reticle (Figure 5) and to the test structures (Figure 6) is shown in the referenced figures.

III. The Readout Integrated Circuit (ROIC)

A 150nm CMOS standard process (LF15A) was selected for the ROIC. The ROIC was partitioned in: an analogue ROIC (A-ROIC), comprising the pixel array with its row control as well as the programmable gain amplifiers (PGA) and a temperature sensor: a digital ROIC (D-ROIC) which includes the multi-column ADCs, followed by a piece-wise linearity correction block, the sequencer and a serial-to-parallel interface (SPI).

In the A-ROIC, the pixel analogue front-end (AFE) has to match 1-to-1 the pixel array in the SiPDA. The AFE has to be able to work in global shutter as well as provide dual gain, with the gain being selectable on a row-by-row basis.

The schematic of the pixel is shown in Figure 7. The diode is in the SiPDA and the line to the input of the source follower MSF corresponds to the hybridising bump. The capacitance C0 is used to adjust the gain of the pixel: when SWG is high, it is connected in parallel to the diode and the pixel works in low gain LG mode; while when SWG is pulled low, C0 is disconnected and the diode works in high gain HG mode. The gain of the pixels can be selected in a row-by-row and frame-by-frame basis. An in-pixel bias transistor MB is provided to help with the global shutter operation. The command lines GR and GS control the shutter transistors MGR and MGS. When activated together with the bias VBIAS, the voltage at the output of the source follower is copied in the in-pixel sampling capacitance. The two samples for the signal and the reset are read in parallel on a dual analogue bus.

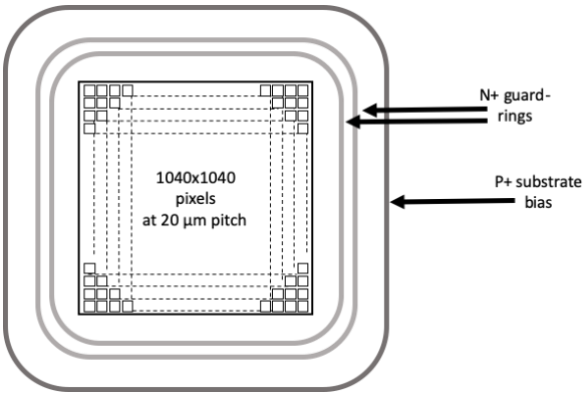

Figure 2. Layout of the SiPDA

Parameter	Optimisation goal
Capacitance	Minimise
Surface leakage current	Minimise
Breakdown voltage	Need to be higher (in absolute value) than the depletion voltage
Pwell isolation bias voltage	Need to be lower (in absolute value) than the breakdown voltage
Full depletion voltage	Minimise

Table 1 Pixel figures of merit and criteria.

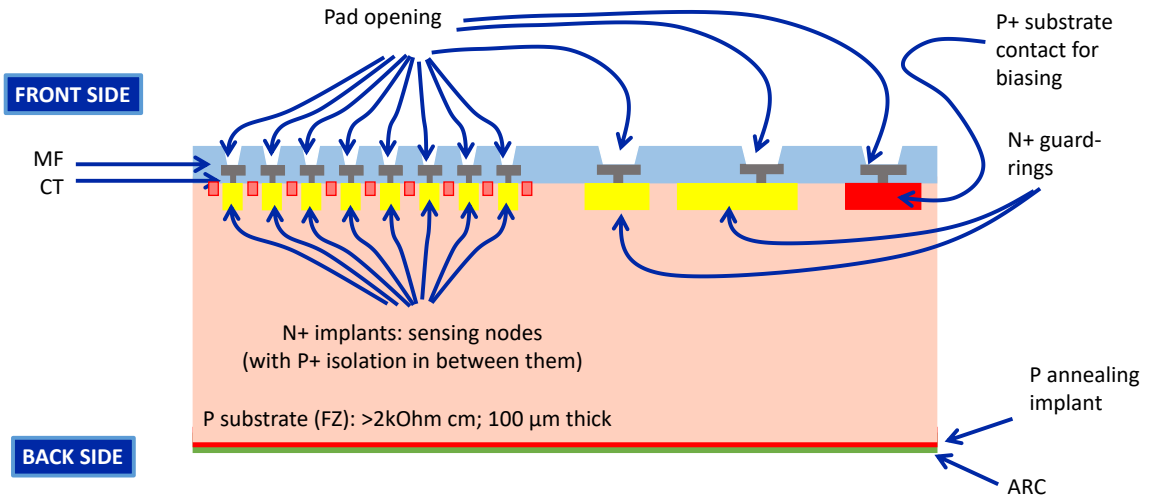

Figure 3. Cross-section of the SiPDA wafer. Drawing not in scale.

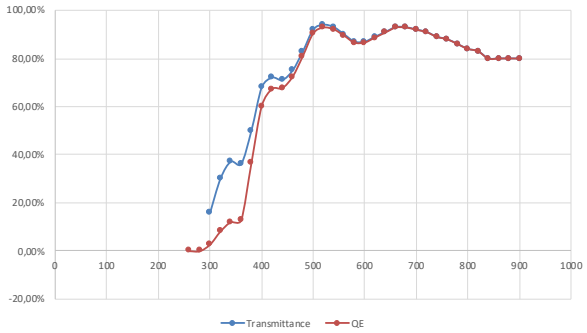

Figure 4. Simulated QE, showing the sensor achieves QE>75% over the 450 to 900 nm band.

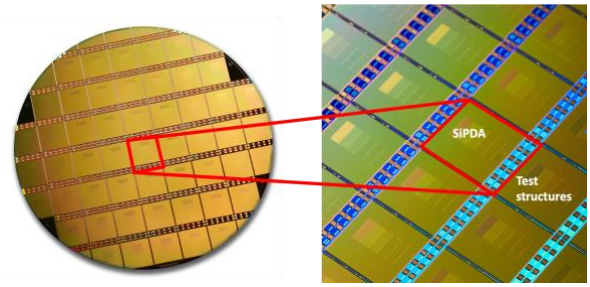

Figure 5. Photo of the SiPDA wafer with a zoom to the reticle

Figure 6. Photo of the test structures on the SiPDA wafer.

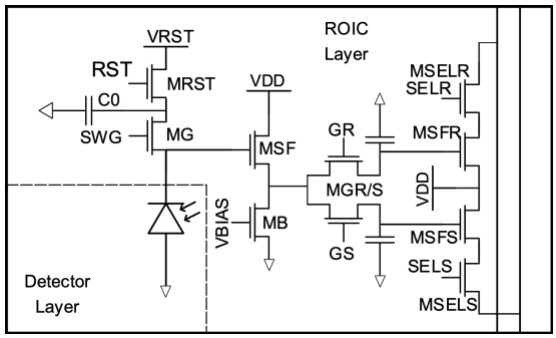

Figure 7. Schematic of the GS pixel, with CDS. The gain is set on a row-by-row basis.

A few variants of the pixel were designed and integrated in the ROIC. The variants have slightly different analogue performance. The targeted operating temperature is 240K. At this temperature, the simulated noise is 12.1/102 e- rms in HG/LG with a corresponding full well of 102/1,110 ke-. At higher temperature of 293K, the noise increases slightly to 12.8/108 e rms and the full well does not change.

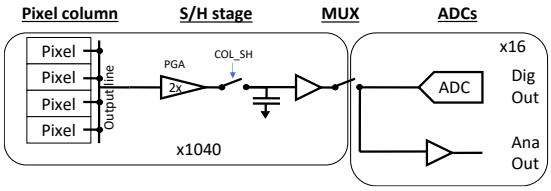

Figure 8. Schematic of the column analogue readout, including the ADC.

The pixel voltage is read through column-parallel programmable gain amplifier (PGA). Their gain can be set to x1, x2 or x4. In order to match the layout of the ADCs, after the sample-and-hold stage there is a 65:1 analogue multiplexer (Figure 9).

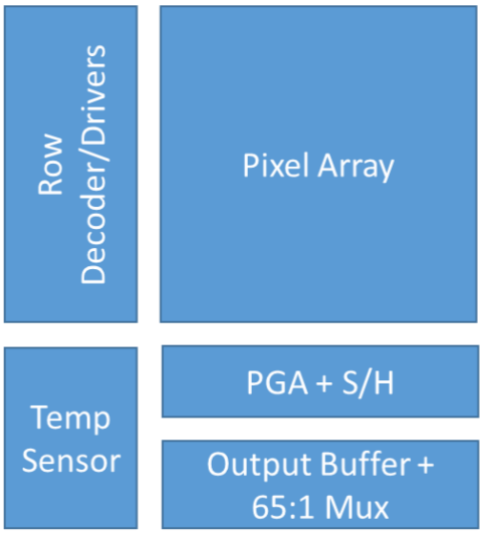

Figure 9. Floorplan of the A-ROIC.

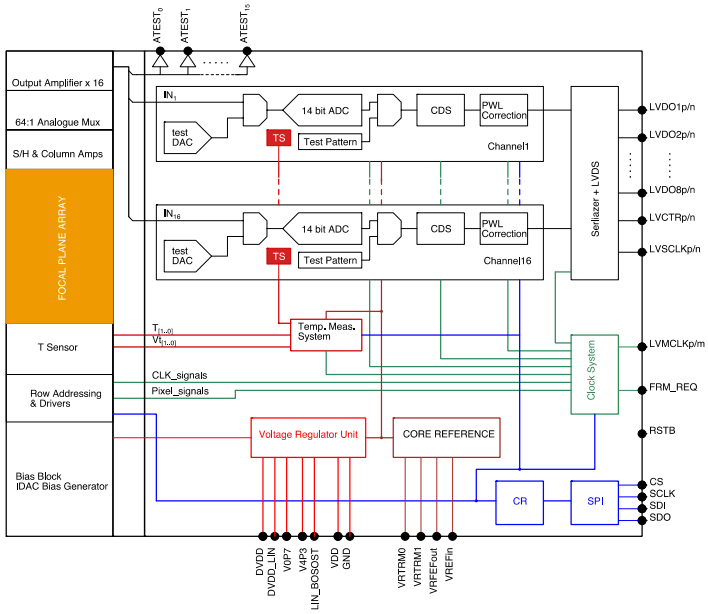

Figure 10. Floorplan of the D-ROIC

The ADC architecture is based on the hybrid successive approximation topology, with a 14-bit resolution. The conversion requires 10 clock cycles and with a clock of 100 MHz the conversion time is

100 nsec.

As a backup solution, an analogue output is also provided. The digitalisation occurs then off-chip. A photo of the packaged ROIC is shown in Figure 11.

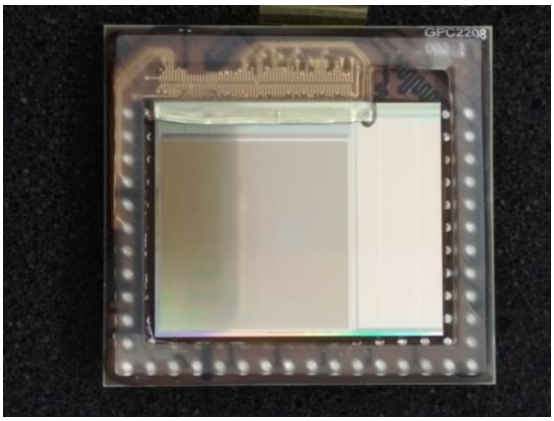

Figure 11. Photo of the packaged ROIC.

IV. Experimental results

The test structures on the SiPDA provided early insight on the behaviour of the sensor before hybridisation. With respect to the parameters listed in Table 1, all but the inter-pixel isolation can be measured on the test structure. Each array in the test structure includes 60x60 pixels, all connected together. In Figure 12, the capacitance is measured for different test arrays as a function of the voltage. The line corresponding to the theoretical minimum capacitance corresponding to the full depletion of the 100 µm thick substrate is also shown. The curve indicates that full depletion is achieved in all test structures for a low bias voltage of around 25-30V.

Figure 13 shows the measured dark current as a function of the applied back-bias for the different test structures. A back-bias as high as 200V was applied, well above the full depletion voltage, and no breakdown was detected, showing that all pixel variants are safe to operate in full depletion.

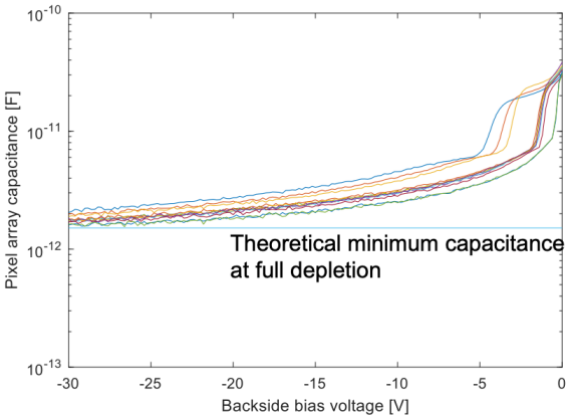

Figure 12. Measured capacitance from different types of pixels on the SiPDA test structure. It shows full depletion is achieved from around 20 V bias.

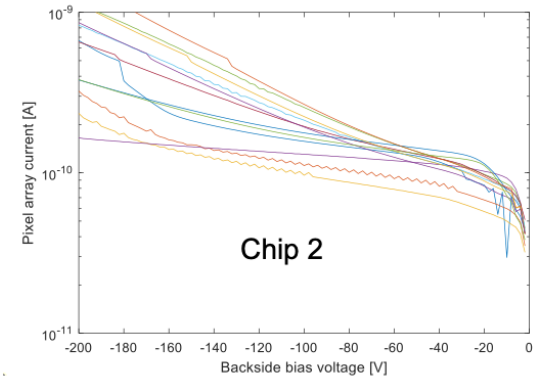

Figure 13. Measured dark current from different types of pixels on the SiPDA test structure.

Figure 14 summarises the dark current measurement for all 12 pixel variants and for 3 different chips. The pixel types can be ordered by implants (three groups: B00 to 03; B04 to 07; B08 to 11) and within each groups similar layouts are used. The measurements show some trends, with the first group (B00 to 03) and the third layout (B02, B06 and B10) having lower leakage. These results can be used for future optimisation of the SiPDA.

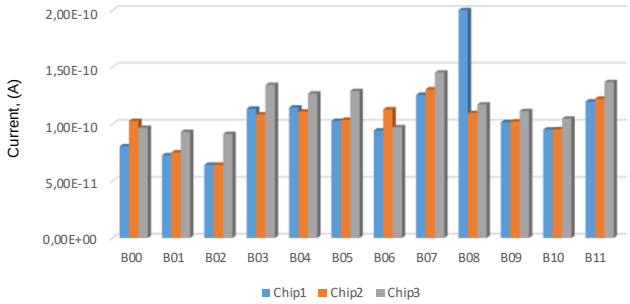

Figure 14. Measured dark current as a function of the design number B00 to B11. The colours refer to data measured on different chips. The dark current seems to be dominated by surface current generation. A new design with improved results is in preparation.

The ROIC is being currently tested before hybridisation. Most functionalities have already been proven. We expect the hybridisation to start soon and being under way by the time of the conference.

V. Conclusions

A megapixel, global shutter, high QE over a wide band hybrid image sensor was designed and manufactured. Initial results of the two layers, the SiPDA and the ROIC, taken individually show their good performance. The two layers should soon be sent for hybridisation with bump-bonding.

VI. Acknowledgement

This work was done under the European Space Agency (ESA) contract number AO/1-9801/19/NL/AR.