Correlations between DCR and PDP of SPAD integrated in a 28 nm FD-SOI CMOS Technology

S. Gao [1], D. Issartel [1,3], M. Dolatpoor Lakeh [2], F. Mandorlo [1], R. Orobtchouk [1], J.-B. Kammerer [2], A. Cathelin [3], D. Golanski [3], W. Uhring [2], F. Calmon [1*]

[1] Univ Lyon, INSA Lyon, CNRS, Ecole Centrale de Lyon, Université Claude Bernard Lyon 1, CPE Lyon, INL, UMR5270, 69621 Villeurbanne, France
[2] ICube, University of Strasbourg, UMR CNRS 7357, Strasbourg, France
[3] STMicroelectronics, Crolles, France

** Contact author: Francis Calmon, francis.calmon@insa-lyon.fr*

Abstract — **This article presents an experimental study of the Dark Count Rate (DCR) and the Photon Detection Probability (PDP) of Single-Photon Avalanche Diodes (SPAD) implemented in 28nm Fully Depleted Silicon-On-Insulator (FD-SOI) CMOS technology and proposes a TCAD simulation study correlating the experimental DCR et PDP results. The measurements and the TCAD simulations show a dependence of DCR and PDP with the amount of the Shallow Trench Isolation (STI) oxide in the active zone and the alignment of the peripheral STI with the SPAD junction. SPADs featuring more STI oxide in the active zone (including the peripheral STI) tend to present higher DCR and PDP. The TCAD simulations show higher values of Avalanche Triggering Probability (ATP) explaining higher PDP obtained with SPAD featuring more STI oxide in the active zone. The defects located at the interface of P-Well / STI and related to the doping steps are potentially the one of the main sources of the higher DCR of the aforementioned SPAD.**

Key words — SPAD; 28nm FD-SOI CMOS; Dark Count Rate DCR; Photon Detection Probability PDP; Shallow Trench Isolation STI; TCAD Simulation; Avalanche Triggering Probability ATP

I. INTRODUCTION

Thanks to their high luminous sensitivity and sub-nanosecond response time, Single-Photon Avalanche Diodes (SPADs) are considered as one of the most suitable candidates in the field of photon counting [1], light detection and ranging (LIDAR) [2], and all applications requiring high sensitivity and fast response time. Also known as Geiger-mode Avalanche Diodes, SPADs have been intensively investigated both in academic research and industry. The Si-based SPADs have been already widely used for visible and near-infrared light due to their compatibility with the CMOS technologies [3][4], with remarkable performances for small SPAD pitches and/or large matrices [5][6][7]. As an alternative architecture, SPAD devices have been successfully implemented in Ultra-Thin Body and BOX (UTBB) 28nm Fully Depleted Silicon-On-Insulator (FD-SOI) CMOS technology [8], in which the SPAD devices are integrated below the buried oxide layer (BOX) and the associated electronics is implemented in the ultra-thin silicon layer above the BOX layer. This integration allows intrinsic 3D stack at die level and therefore a greater fill-factor.

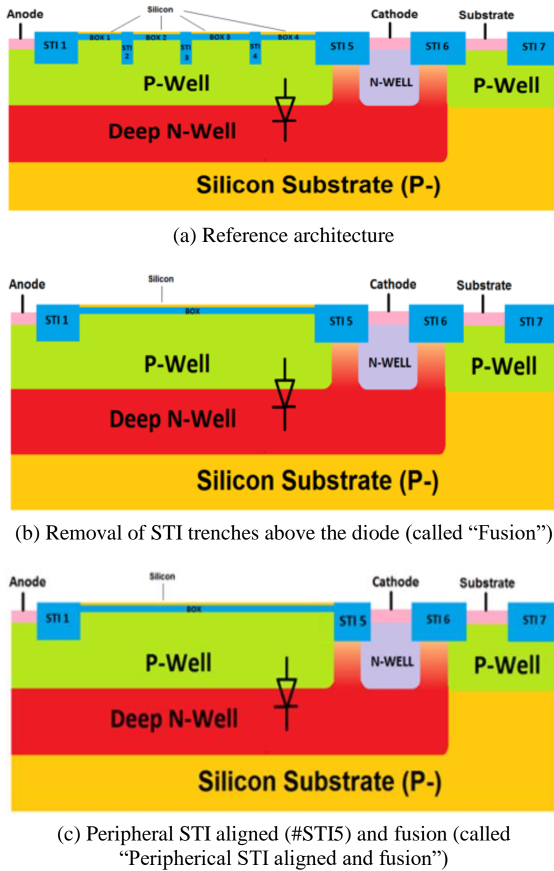
The performances of SPADs can be estimated by several criteria. Two of the most crucial ones are the Dark Count Rate (DCR) and the Photon Detection Probability (PDP). The former is defined as the number of undesired avalanche events per second and characterises the intrinsic noise of the SPAD device. The latter is used to evaluate the optical efficiency of the SPAD device and is defined as the probability of a received incident photon to generate an avalanche event.

In previous work, optimized architectures have been proposed to reduce DCR level of SPAD implemented in FD-SOI technology [9]. In this work, the proposed SPAD devices are characterised both in DCR and PDP. TCAD simulations are performed in order to correlate the experimental results of DCR and PDP measurements. The following sections are organised as follow: Section II introduces the proposed SPAD implemented in 28nm FD-SOI CMOS technology; Section III and IV respectively present the DCR and PDP measurements; Section V proposes an analyse of TCAD simulations allowing cross correlations between DCR and PDP; Section VI concludes the manuscript and gives some perspectives.

II. SPAD INTEGRATED IN CMOS FD-SOI TECHNOLOGY

The SPAD FD-SOI reference architecture is presented in Figure 1-a, the diode is made of a P-well / deep N-well (DNW) junction below the BOX layer

and the thin silicon layer (UTBB FD-SOI technology). The main advantage of this approach is to natively obtain a 3D SPAD pixel at die level considering back side illumination after die thinning, and associated electronics on top of the diode. Thanks to a Multi Project Wafer (MPW) run with standard CMOS FD-SOI 28nm standard process (except DNW implant), SPADs (25µm diameter, pseudo-circular shape) have been processed and characterized with 200kΩ integrated resistance as passive quenching and external readout [8][9]. Figure 1-b and 1-c represent two alternatives of SPAD FD-SOI architectures.



(a) Reference architecture

(b) Removal of STI trenches above the diode (called “Fusion”)

(c) Peripheral STI aligned (#STI5) and fusion (called “Peripherical STI aligned and fusion”)

Figure 1: SPAD FDSOI schematic drawing of the three main studied structures with different positions of the STI regards to junction between P-Well and Deep N-Well.

In the reference architecture, design rules impose the presence of the Shallow Trench Isolation (STI) oxide in the active zone (represented by “STI 2”, “STI 3” and “STI 4”). The defects located at the interfaces STI / P-Well are considered as the one of the main sources of DCR. The architecture called “Fusion” (Figure 1-b) has been proposed by removing (minimizing) these STI. Beyond the “Fusion” architecture, the peripheral STI (“STI 5”) in the reference architecture is also considered as one major contribution to the DCR. The alignment of “STI 5” with peripheral junction (called “Peripheral STI aligned”) alongside with the “Fusion” architecture has been proposed to further reduce the DCR level (called “Peripheral STI aligned and fusion”, Figure 1-c).

III. DCR STUDY

DCR has been intensively studied for specific architectures as depicted in Figure 1 (different STI locations) leading to different V_{ex} operating ranges above breakdown voltage around 15.8V at room temperature [9]. The STI locations in the active zone and at the periphery of the diode impact significantly the DCR performances (Figure 2). The “Fusion” architecture presents similar DCR level compared to reference architecture for V_{ex} below 7% V_{BD}. The alignment of peripheral STI allows to reach higher values of V_{ex}. A maximum excess voltage range of 20% can be reached for the architecture shown in Figure 1-c when removing the STI in the active zone and aligning the peripheral STI with the junction (i.e. structure called “Peripheral STI aligned and fusion”). This same architecture also presents the lowest DCR among the three aforementioned architectures for the same V_{ex}. Extracted activation energy, less than half the band gap of Si (between 0.2-0.3eV), indicates that the origin of the DCR can be a combination of band to band tunnelling and trap assisted or field enhanced generation recombination mechanisms.

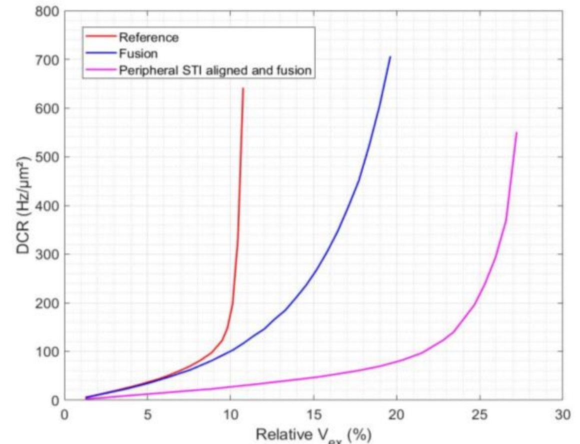


Figure 2: DCR versus relative excess voltage for the different architectures presented in Figure 1 (20°C)

IV. PDP STUDY

Measured PDP (front side illumination) for the different architectures are represented in Figure 3 (V_{ex} = 0.8V i.e. ~5%V_{BD}). The standard process is used (except DNW implant) including all back end of line layers (BEOL) without antireflective coating (ARC), micro-lens. The reference architecture presents the highest PDP, but the lowest performances in terms of DCR as maximum V_{ex} is around 10% (Figure 2). On the other hand, the “Peripheral STI aligned and fusion” architecture

presents the lowest values of PDP (PDP_{max} is around 4.2% for V_{ex} = 0.8V at 620 nm of wavelength) while presenting the best DCR performances, since it can reach 20% higher values of V_{ex} and the reference architecture exhibits 2 to 4 times higher values of DCR. The performance of the “Fusion” architecture stands in between of the other two architectures, with PDP_{max} being around 5% for V_{ex} = 0.8V at 620 nm of wavelength.

Then, we characterized the optimized architecture for DCR (“Peripheral STI aligned and fusion” Figure 1-c) varying V_{ex} up to 20% in Figure 4 with a maximum measured PDP around 12% at 620 nm of wavelength. This time, although the reference architecture exhibits higher PDP for the same V_{ex}, the “Peripheral STI aligned and fusion” architecture is more realistically advantageous due to the higher applicable V_{ex}. The PDP_{max} around 12% is comparable to some studies in the literature [10][11][12].

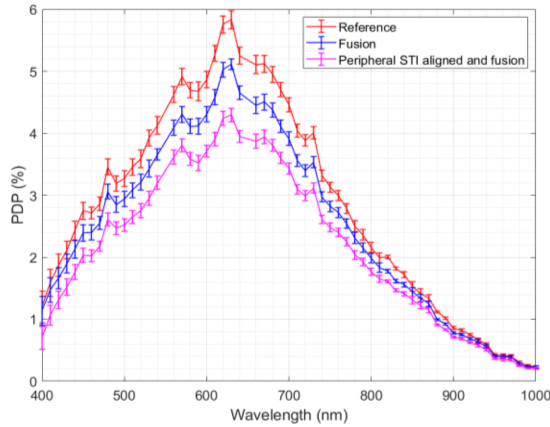


Figure 3: PDP for the different architectures presented in Figure 1 (Vex = 0.8V, 20°C)

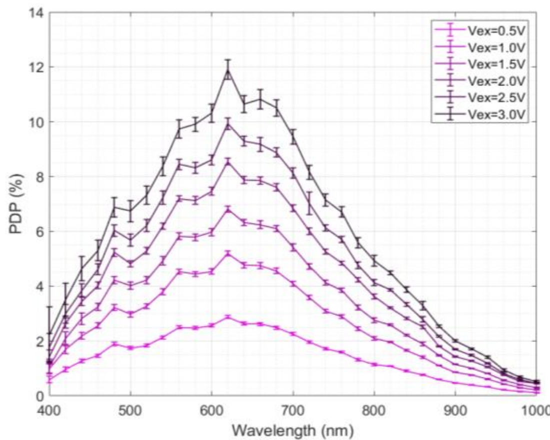


Figure 4: PDP for different V_{ex} (architecture: Peripheral STI aligned and fusion), 20°C

V. Analysis and complementary TCAD simulations

To further correlate the PDP and DCR measurements, the PDP_{max} results have been plotted as a function of the DCR measurements in Figure 5. The points {PDP_{max}-DCR} of the three architectures at same V_{ex} = 0.8V are highlighted in the triangle. The reference architecture, with the most amount of STI trenches (in the zone active and at the periphery) presents both higher DCR and PDP results, while the opposite case applies to the “Peripheral STI aligned and fusion” architecture. Now considering the points PDP_{max} versus DCR with different V_{ex} for the “Peripheral STI aligned and fusion” architecture (green symbols), we observe a quasi-linear behaviour.

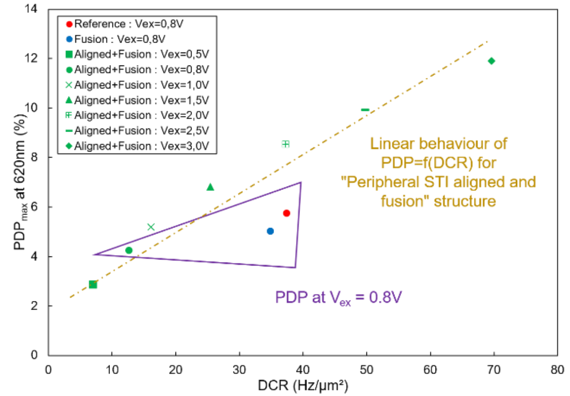


Figure 5: Maximum PDP at 620 nm of wavelength versus DCR for different structures and biasing voltages (20°C)

TCAD simulations indicate that the electric field is maximum at the diode periphery whatever the architecture. Moreover, for a given bias voltage, the reference architecture (Figure 1-a) exhibits the highest electric field and consequently the highest Avalanche Triggering Probability (ATP) compared to other architectures (observed in Figure 6). This remark explains the higher PDP observed for the “reference” structure compared to the “Peripheral STI aligned and fusion” one for the same excess voltage V_{ex}.

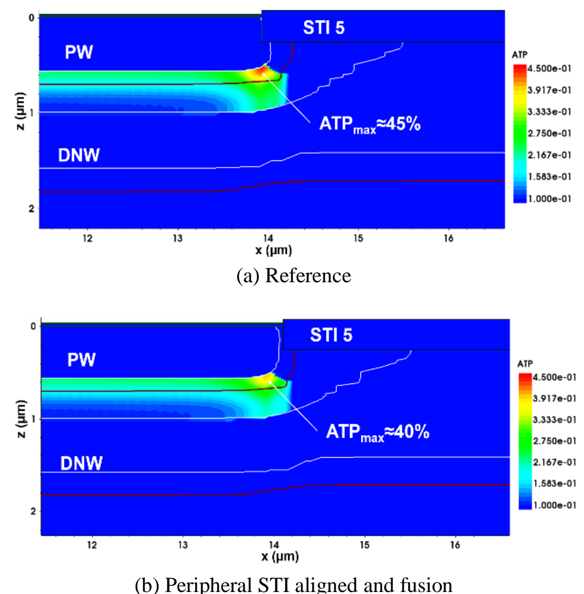


Figure 6: Simulated Avalanche Triggering Probability (ATP) maps at the diode periphery

When including the defects located at the STI interfaces (that contribute to DCR), simulated dark current level decreases when the peripheral STI is shifted at the edge of the junction (architecture called "Peripheral STI aligned", Figure 7). Then we conclude that the "reference" structure presents the higher PDP due to higher electric field and ATP at the diode periphery, and the higher DCR due to STI defects.

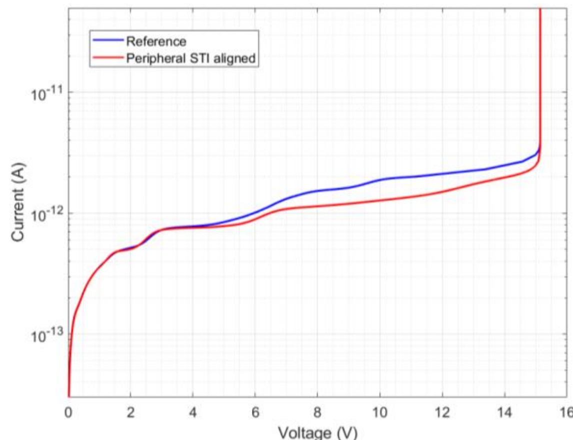


Figure 7: Simulated $I(V)$ curves with defects located at STI interfaces for the "reference" and the "Peripheral STI aligned" structures

VI. Conclusion and Perspectives

Experimental DCR and PDP results obtained with passive quenching and external readout for SPAD integrated on CMOS FD-SOI technology are presented. The impact of STI locations (in the active zone and at the periphery) is analysed and TCAD simulations allows to understand the different experimental performances. Minimizing the amount of shallow trench isolation above the active region of the SPAD allows reducing the Dark Count Rate while extending the excess voltage range. Promising results have been obtained with a maximum PDP around 12% (at a wavelength of 620 nm) associated with a DCR less than 70 Hz/µm² (room temperature) at 20% excess bias voltage. Recently active quenching has been introduced and significant after-pulsing reduction has been demonstrated [13]. Ongoing work concerns PDP measurement for different STI patterning using approach introduced in [14].

Acknowledgment

The authors would like to thank the Nano2022 research program, the French national research agency ANR (ANR-18-CE24-0010) and CMP (Grenoble) for IC prototyping services.

References

[1] M. Perenzoni et al. "A 160×120 Pixel Analog-Counting Singe-Photon Imager With Time-Gated and Self-Referenced Column-Parallel A/D Conversion for Fluorescence Lifetime Imaging," IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 155-167, 2015 (https:// 10.1109/JSSC.2015.2482497)

[2] I. Takai et al. "Single-Photon Avalanche Diode with Enhanced NIR-Sensitivity for Automotive LIDAR Systems," Sensors, vol. 16 no. 4, p. 459, 2016 (https://doi.org/10.3390/s16040459)

[3] W. Jiang et al. "Time-Gated and Multi-Junction SPADs in Standard 65nm CMOS Technology," IEEE Sensors Journal, t. 21, no. 10, p. 12092-12103, 2021 (https://doi.org/10.1109/JSEN.2021.3063319)

[4] S. Pellegrini et al. "Industrialised SPAD in 40nm technology," IEEE International Electron Devices Meeting (IEDM) 2017 (https://doi.org/10.1109/IEDM.2017.8268404)

[5] K. Morimoto et al. "3.2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing," IEEE International Electron Devices Meeting (IEDM) 2021 (https://10.1109/IEDM19574.2021.9720605)

[6] S. Shimada et al. "A Back Illuminated 6µm SPAD Pixel Array with High PDE and Time Jitter Performance," IEEE International Electron Devices Meeting (IEDM) 2021 (https://10.1109/IEDM19574.2021.9720639)

[7] S. Shimada et al. "A SPAD Depth Sensor Robust Against Ambient Light: The Importance of Pixel Scaling and Demonstration of a 2.5µm Pixel with 21.8% PDE at 940nm, IEEE International Electron Devices Meeting (IEDM) 2022 (https:// 10.1109/IEDM45625.2022.10019414)

[8] T. Chaves de Albuquerque et al. "Integration of SPAD in 28nm FDSOI CMOS technology," ESSDERC 2018 (http://dx.doi.org/10.1109/ESSDERC.2018.8486852)

[9] D. Issartel et al. "Architecture optimization of SPAD integrated in 28 nm FD-SOI CMOS technology to reduce the DCR," Solid-State Electronics, Elsevier, Volume 191, April 2022, p. 108297 (https://doi.org/10.1016/j.sse.2022.108297)

[10] Z. You et al. "3µm Pitch, 1µm Active Diameter SPAD Arrays in 130nm CMOS Imaging Technology," IISW 2017, (Available: http://www.imagesensors.org /Past%20Workshops/2017%20Workshop/2017%20Papers/R21.pdf)

[11] A. Karz et al. "CMOS Single-Photon Avalanche Diode Pixel Design for a Gun Muzzle Flash Detection Camera," IEEE Transactions on Electron Devices, t. 65, no. 2, p. 547-554, 2018, (https://doi.org /10.1109/TED.2017.2779790)

[12] H. Ouh et al. "Combined In-Pixel Linear and Single-Photon Avalanche Diode Operation With Integrated Biasing for Wide-Dynamic-Range Optical Sensing," IEEE Journal of Solid-State Circuits, t. 55, no. 2, p. 392-403, 2020 (https://doi.org/10.1109/JSSC.2019.2944856)

[13] M. Dolatpoor Lakeh et al. "An Ultrafast Active Quenching Active Reset Circuit with 50 % SPAD Afterpulsing Reduction in a 28 nm FD-SOI CMOS Technology Using Body Biasing Technique" MDPI Sensors, 21(12), 4014, 2021 (https://doi.org/10.3390/s21124014)

[14] S. Gao et al. "3D Electro-optical Simulations for Improving the Photon Detection Probability of SPAD Implemented in FD-SOI CMOS Technology" SISPAD conference, 27-29 Sept. 2021 (https://doi.org/10.1109/SISPAD54002.2021.9592555)