

A Charge pump based TDI accumulator for CMOS Image Sensors

Rahul Kumar Singh^{1,2,3}, Siddhant Jain², Aakash Vishwakarma², and Mukul Sarkar^{1,2}

¹Indian Institute of Technology, Delhi

²3rdiTech (DV2JS Innovation LLP), Delhi

³Email: rahul@3rditech.in, Tel: +91-1126591072

Abstract—Time delay integration (TDI) imaging sensors are used in remote push-broom sensing systems to improve the image quality in low light or when the relative speed of the scene and the detector is large. As the light from the scene accumulates in succession on each row, an accumulator adds the signals. The accumulator limits the signal-to-noise ratio of the TDI imaging systems. This paper presents an 8-stage, charge pump-based TDI accumulator addressing the saturation problem of integration-based accumulators. A prototype microchip of 128 x 8 TDI stage has been designed and fabricated in AMS 350 nm 1P4M OPTO process. The supply voltage used is 3.3 V with a pixel pitch of 10 μm . The measured SNR improvement for the 8-stages is 10.6 dB.

Keywords— Time Delay Integration(TDI), CMOS Image Sensors(CIS), Analog accumulators

I. INTRODUCTION

Time delay integration (TDI) imaging sensors are used in remote push-broom sensing systems. It is used to improve the image quality in low light or when the relative speed of the scene and the detector is large. A large relative motion between the scene and the detector results in blurred images. In TDI, the pixels in the along-track direction capture the same target multiple times, therefore extending its equivalent integration time [1-2].

A typical 4-stage TDI operation has been demonstrated in figure 1. An object O1 is captured by pixels P1-P4 at time intervals $t_0 - t_3$. As the light from the scene is accumulated in succession on each row, an accumulator is used to add the signals. The extended integration time or accumulation of the same signal significantly improves the Signal-to-Noise (SNR) ratio of the captured image [3-4]. In the analog-domain accumulation, the output of the pixels are accumulated by an analog accumulator and then quantized by column ADC. The preferred choice of accumulator in the analog domain is switched capacitor-based integrator [2,3,5]. The maximum accumulated voltage for switched capacitor integrator-based accumulator depends on the supply voltage and thus has a limited accumulation and dynamic range.

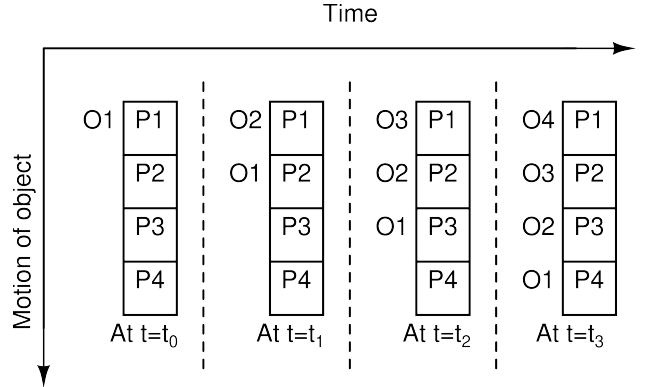


Figure 1: TDI operation

The multiple captures of the same scene work well in low-light environments or with a lesser number of TDI stages. In the presence of moderate or high light or as the number of TDI stages increases, the output of the accumulator saturates [2,5]. High precision and high linearity accumulation in low light have always been a problem with TDI [6]. Conventional integrator based accumulators have limited voltage swing and thus it becomes problematic in case of higher number of TDI stages or in case of over exposure of signals.

In this paper, a charge pump based hybrid TDI accumulator is presented. Charge pump based accumulator helps in utilising a hybrid mode of accumulation where analog as well as digital summation can happen. The hybrid algorithm also solves the accumulator saturation problem often seen with switched capacitor-based integrator. The hybrid mode extends the cumulative range of the TDI accumulator improving the SNR. A prototype chip has been designed and characterized in AMS 350 nm 1P4M OPTO process. The SNR boost obtained using charge pump-based accumulator is 10.6 dB for an 8-stage TDI.

The rest of the paper is organized as follows: section II describes the imager architecture, section III describes the measurement results and conclusions are presented in section IV.

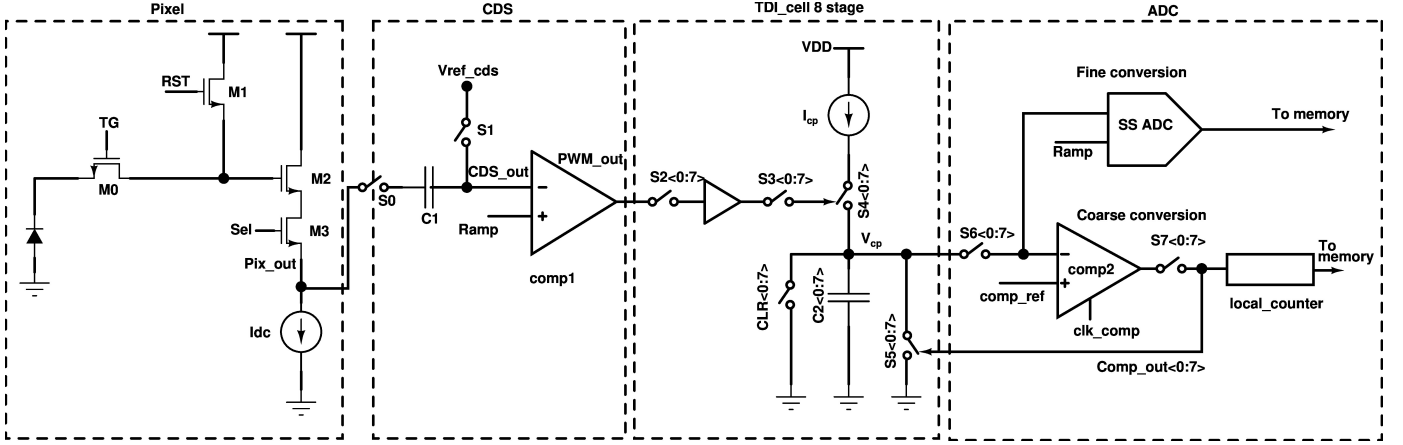


Figure 2: Proposed TDI architecture

II. SYSTEM ARCHITECTURE AND CIRCUIT

The proposed system architecture for the linear TDI sensor is shown in figure 2. The TDI sensor consists of four components (a) 3T-APS (active pixel sensor) (b) correlated double sampling (CDS) with pulse width modulator (PWM) in column (c) charge pump-based integrator and (d) slope-based ADC for digital conversion. A 3T pixel with an extra switch between the photodiode and the source follower is used to decouple the sensing and storage nodes. The operational timing diagram for the sensor is shown in figure 3.

The integrated output of the pixel is transferred to column using in-pixel source follower. The output of the column is sampled on the CDS capacitor (C_1). The sampled output is compared with a ramp in comparator (comp1) to get a PWM signal. The width of the PWM signal represents the incident light intensity on the photodiode. The resultant PWM_out signal controls the charge pump. This charge pump functions as a TDI accumulator or TDI cell. When PWM_out signal is high, capacitor bank C_2 is charged with a DC current source I_{cp} . The accumulated output of the charge pump (V_{cp}) is compared with a fixed reference comp_ref in a clocked comparator (comp2).

A feedback circuitry using comparator comp2 is used to monitor the output of the charge pump (V_{cp}). It resets C_2 through switch S_5 , when V_{cp} exceeds comp_ref value. The output of comp2 is stored in a 6 bit counter which tracks the total number of comparator triggering. The counter output is stored in a memory and provides the 6 MSB bits coarse conversion of the ADC. For PWM_out signal being active, the charge pump accumulates. When PWM_out is inactive, the charge pump holds its output V_{cp} . The stored V_{cp} , is quantized for fine conversion using a single slope 8-bit ADC. The resultant digitized signal is the combination of the 6-bit coarse and 8-bit fine conversion. The effective ADC resolution is 14 bits.

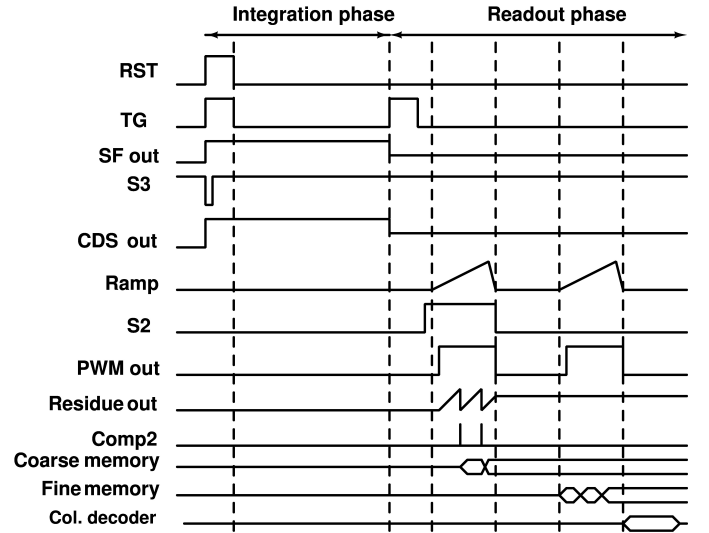


Figure 3: TDI operation

A. Charge pump accumulator theory

For high light, comp2 can trigger multiple times. It results in multiple integration cycles for C_2 . Thus total pulse width of PWM signal is given as

$$T_{PWM} = nT_{ch} + T_{res} \quad (1)$$

where n is the number of times capacitor C_2 is reset, T_{ch} is the charging time till V_{cp} reaches comp_ref value and T_{res} is the time left in PWM pulse after multiple reset signals.

Since the charge pump feeds the input to both analog and digital mode of accumulator conversion, the total digitized output is the sum of both analog as well as digital outputs. Thus digitized output is given as

$$(Vout)_{eq} = (Vout)_{ana} + (Vout)_{dig} \quad (2)$$

where, $Vout_{ana}$ is the analog output which is the residue voltage stored on C_2 . $Vout_{dig}$ is the voltage

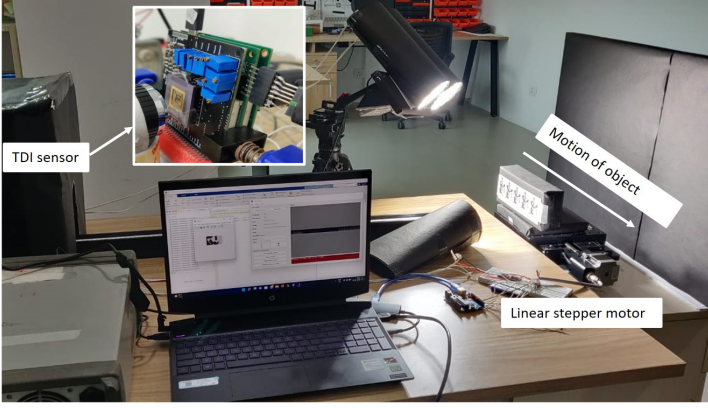


Figure 4: Measurement setup

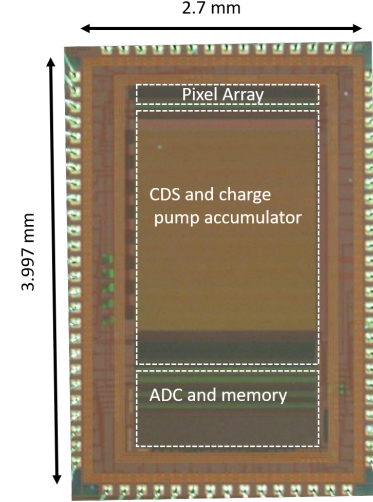


Figure 5: Microchip photograph of the sensor

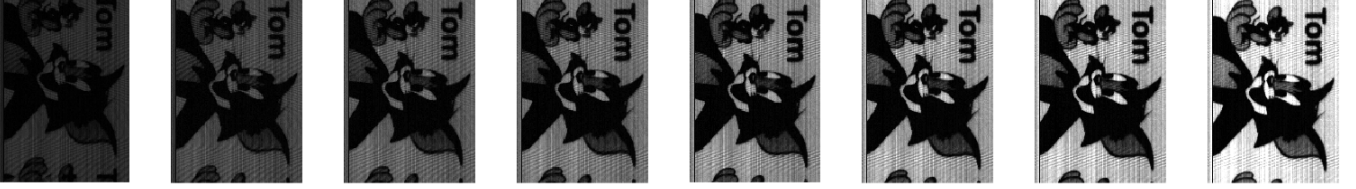


Figure 6: Captured images using prototype sensor (TDI 1 to 8 stage)

output equivalent to the number of times the charge pump is reset. The analog output can be written as

$$(V_{out})_{ana} = \int_0^{T_{res}} \frac{I_{cp}}{C_2} dt = \frac{I_{cp}T_{res}}{C_2} \quad (3)$$

In case of coarse conversion digital equivalent voltage $V_{out,d1}$ can be given as

$$V_{d1} = \int_0^{T_{ch}} \frac{I_{cp}}{C_2} dt + \int_0^{T_{del}} \frac{I_{cp}}{C_2} dt \quad (4)$$

where T_{ch} is the charging time till V_{ch} reaches $comp_ref$ value, T_{del} is the excess delay time because of comparator delay. Excess delay term will come into picture only when residue voltage exceeds $comp_ref$ and comparator gets triggered.

Thus digital equivalent of voltage that can be stored on C_2 when comparator triggers is

$$V_{d1} = \frac{I_{cp}(T_{ch} + T_{del})}{C_2} \quad (5)$$

I_{cp} keeps on charging V_{cp} even when $comp2$ is high and V_{cp} is grounded. This results in a loss of charges which should have been part of the accumulation. Thus for multiple integration cycles, the equivalent digital output is given as

$$(V_{out})_{dig} = n(V_{d1}) - \frac{(n-1)I_{cp}T_{clk}}{C_2} \quad (6)$$

where T_{clk} is the comparator clock time when capacitor C_2 is forced to reset value while being charged

by the current source. The $n-1$ term in equation (6) denotes the loss of charges in accumulation.

$$(V_{out})_{dig} = \frac{nI_{cp}(T_{ch} + T_{del})}{C_2} - \frac{(n-1)I_{cp}T_{clk}}{C_2} \quad (7)$$

Thus the total digitized output can be written as

$$(V_{out})_{eq} = \frac{I_{cp}T_{res}}{C_2} + \frac{nI_{cp}(T_{ch} + T_{del})}{C_2} - \frac{(n-1)I_{cp}T_{clk}}{C_2} \quad (8)$$

Rearranging equation (8),

$$(V_{out})_{eq} = \frac{I_{cp}}{C_2} (T_{res} + n(T_{ch} + T_{del}) - (n-1)T_{clk}) \quad (9)$$

The comparator clock is chosen to be at a relatively higher frequency compared to the PWM. Thus $T_{clk} \ll T_{PWM}$. So equation (9) can be simplified as

$$(V_{out})_{eq} = \frac{I_{cp}}{C_2} (T_{res} + n(T_{PWM} + T_{del})) \quad (10)$$

The maximum output voltage, $(V_{out})_{eq}$ is limited by a maximum swing in the analog domain but its digital equivalent is limited by the maximum count n that the counter can support. Thus total accumulation range can be enhanced n times by combining the coarse and fine conversion.

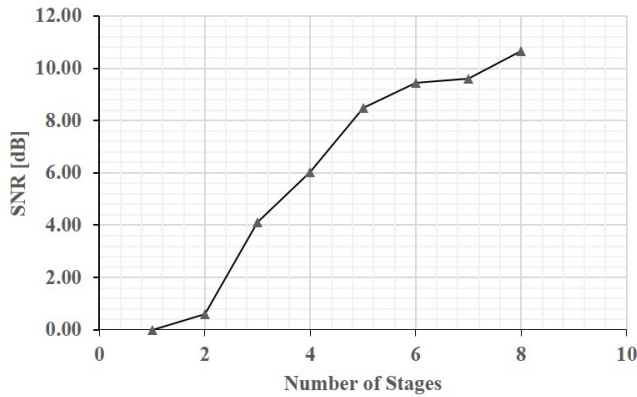


Figure 7: SNR boost plot

III. MEASUREMENTS RESULTS

Figure 4 shows the microchip photograph of the proposed TDI sensor. The TDI sensor is fabricated in AMS 350 nm OPTO process. It works on 3.3 V power supply. The pixel pitch is $10 \mu\text{m} \times 10 \mu\text{m}$. Figure 5 demonstrates the measurement setup. A linear actuator-based stepper motor has been used to provide orthogonal movement of the object with respect to the sensor. Corresponding images have been captured using Pleora iPORT CL-U3 frame grabber.

Figure 6 shows the images captured using the prototype sensor. These images are unprocessed images. As the TDI stage increases, the captured images have an improved SNR as expected. The accumulator suffers from non-idealities of the charge pump and hybrid ADC architecture. Therefore, the effective ADC resolution measured is 12-bit. The measured performance of the prototype sensor is summarized in Table. I. Figure 7 shows the measured SNR boost plot. The measured SNR with 8-stage TDI demonstrates an SNR improvement of 10.6 dB. The SNR boost obtained in [6] is 9.2 db for 8-stage TDI. Power dissipation per column is $16.5 \mu\text{W}$ at a line rate of 620 Hz.

Table I: Sensor characteristics

Technology (nm)	350
Pixel type (μm)	3T APS with extra switch
Array size	128×8
Pixel pitch (μm)	10
Supply voltage (V)	3.3
Max Line rate	1.07 kHz
Power consumption	$16.5 \mu\text{W}$ per column @ line rate of 620 Hz
SNR boost	10.6 dB

IV. CONCLUSION

A prototype of 128×8 TDI sensor has been designed and fabricated in AMS 350 nm 1P4M OPTO

process. The TDI imager uses charge pump based accumulator. The accumulator is reset based on the PWM signal generated proportional to the incident light intensity. The combination of the number of times the charge pump is reset and the residue voltage left on the charge pump gives a 12-bit resolution. The limitation in the resolution is due to the noise of the comparator. The proposed imager overcomes the swing limitation of conventional integrator based imagers by utilising hybrid mode of accumulation and provides a 10.6 dB SNR boost.

REFERENCES

- [1] M. G. Farrier and R. H. Dyck, "A Large Area TDI Image Sensor for Low Light Level Imaging," in *IEEE Journal of Solid-State Circuits*, vol. 15, no. 4, pp. 753-758, Aug. 1980, doi: 10.1109/JSSC.1980.1051465.
- [2] G. Lepage, J. Bogaerts and G. Meynants, "Time-Delay-Integration Architectures in CMOS Image Sensors," in *IEEE Transactions on Electron Devices*, vol. 56, no. 11, pp. 2524-2533, Nov. 2009, doi: 10.1109/TED.2009.2030648.
- [3] H. Yu, X. Qian, M. Guo, S. Chen and K. S. Low, "A time delay integration CMOS image sensor with online deblurring algorithm," *VLSI Design, Automation and Test(VLSI-DAT)*, 2015, pp. 1-4, doi: 10.1109/VLSI-DAT.2015.7114510.
- [4] K. -L. Liu, C. -C. Hsieh, S. -Y. Lai and C. -F. Chiu, "A time delay multiple integration linear CMOS image sensor for multispectral satellite telemetry," *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2016, pp. 37-40, doi: 10.1109/ASSCC.2016.7844129.
- [5] H. Yu, X. Qian, S. Chen and K. S. Low, "A Time-Delay-Integration CMOS image sensor with pipelined charge transfer architecture," *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, Korea (South), 2012, pp. 1624-1627, doi: 10.1109/ISCAS.2012.6271566.
- [6] K. Nie, S. Yao, J. Xu, J. Gao and Y. Xia, "A 128-Stage Analog Accumulator for CMOS TDI Image Sensor," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 7, pp. 1952-1961, July 2014, doi: 10.1109/TCSI.2014.2304663.