A SPAD based Multi-Mode Compressive LiDAR Pixel for Depth Ranging by Direct ToF Measurement

Sohail Faizan, Kapil Jainwal - *Member IEEE*, Minal Bisen, and Nitin Khanna

***Abstract*—This work proposes a novel compressive Light Detection and Ranging (LiDAR) pixel. The pixel operates by the direct Time-of-Flight (dToF) method and utilizes a Single Photon Avalanche Diode (SPAD) for photon detection. It implements a current-starved circuit for an initial logarithmic response, resulting in a higher resolution at short ranges. The pixel subsequently switches to a linear circuit, providing a large full-scale range. The multi-mode implementation provides high accuracy and a long full-scale range (FSR), while avoiding a high data rate all in a compact pixel design. The proposed pixel is realized in standard 65nm TSMC process. It has a minimum detection distance of 16 mm (106.65 ps), a logarithmic depth resolution of 16mm - 0.17 m and a linear depth resolution 0.59 m (3.9 ns). The dynamic range of the pixel is 500 m. The maximum voltage error of the logarithmic part is 2.5% to -0.5%. The logarithmic pixel has a pitch of 8 μm×6 μm**

I. Introduction

Depth measurement is a crucial mode of sensing, the need for which is rapidly growing with the ongoing automation revolution. The Time-of-Flight (ToF) method uses the time taken by LASER pulses reflected from a surface to calculate the distance. Indirect ToF (iToF) uses the phase difference between the transmitted and the received pulse to calculate the distance, while direct ToF (dToF) measures the total time taken by the light pulse from the transmission to detection [1]- [3]. iToF based pixels provide a higher resolution but are confined to small ranges, while dToF provides a lower resolution but can be designed for much larger ranges. The dToF ranging is realised using time-to-amplitude converters (TAC) or time-to-digital converters [4]- [15]. TACs integrate the time to a voltage, while TDCs use counters to measure the time [11]- [12]. The former are more compact but offer lower depth resolution, while the latter are larger (due to large in-pixel elements such as counters) but provide a high degree of depth accuracy [4]- [15].

Compressive pixels are used to achieve higher sensitivities at desired ranges [4]. An implementation of the same is logarithmic pixels (Fig. 1(a)), which provide high sensitivity at lower ranges. Standard logarithmic pixels are built by a current-starved design [4], where the gate of a transistor is connected to a full switch on voltage, but the transistor is kept in the sub-threshold region by limiting the current flowing through it. The sub-threshold operation gives a logarithmic voltage relation dependent on the current flowing through the circuit as follows:

$$V_{out} = V_{dd} - \alpha V_T \ln\left(\frac{L}{W} \cdot \frac{I_{ds}}{I_{d0}}\right), \quad (1)$$

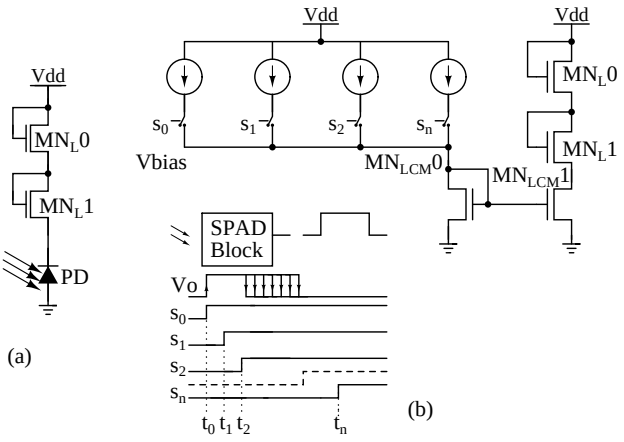

Fig. 1: (a) Conventional log pixel (b) Step logarithmic generation theorisation

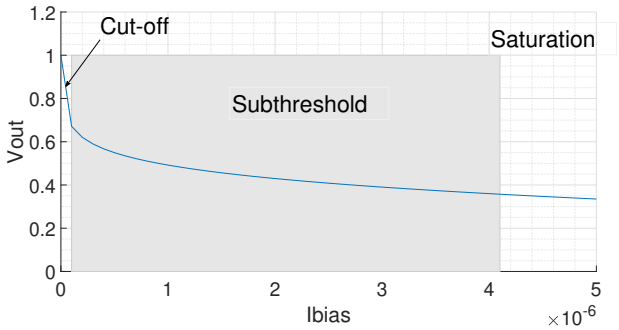

Fig. 2: Operational range of log design

where V_{dd} is the supply voltage, V_T is the thermal voltage, L (length) and W (width) stand for the general representations of the dimensions of the transistor MN_L0, 'α' refers to the sub-threshold swing coefficient, and I_{d0} is the reverse saturation current. In conventional intensity-based imagers, the sub-threshold current is drawn by a photodiode, which has a linear current output in relation to incident light intensity [4]. A cascode transistor is implemented to increase the impedance, increasing the output voltage swing. This paper builds on the same concept to measure the time-of-flight in a compressive manner, porting the design from the intensity domain to the time domain to achieve a high degree of accuracy. The logarithmic voltage is generated by creating a stepped ramp current mirror (vis-a-vis Fig. 1(b)). From eq. 1, it can be concluded that such a current will provide a logarithmic output (as is reflected in Fig.2).

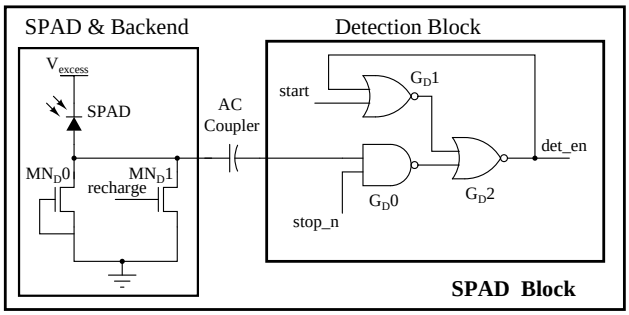

Fig. 3: SPAD block with Enable Generation [15]

II. Compressive Pixel Design

A. SPAD Back-end and Detection Block

This pixel utilises a single photon avalanche diode (SPAD) for the detection of photons. A SPAD on the incidence of a single photon goes into the breakdown region, thus providing a large current [16]- [17]. As shown in Fig.3, a passive quench circuit is implemented with MN_D0, providing a large resistance. An active recharge circuit is created by MN_D1. A similar but modified enable generation logic, presented in [15], is implemented. The circuit generates an active-high enable 'det_en', which starts from the signal 'start'. 'det_en' goes back to low again at either the 'stop' signal or when a photon is detected, whichever event occurs first. Thus, the gap between the start and stop signals is the full-scale range of the system, and the ' det_en' signal's pulse width gives us the total ToF.

B. Time Dependent Ramp Current Mirror

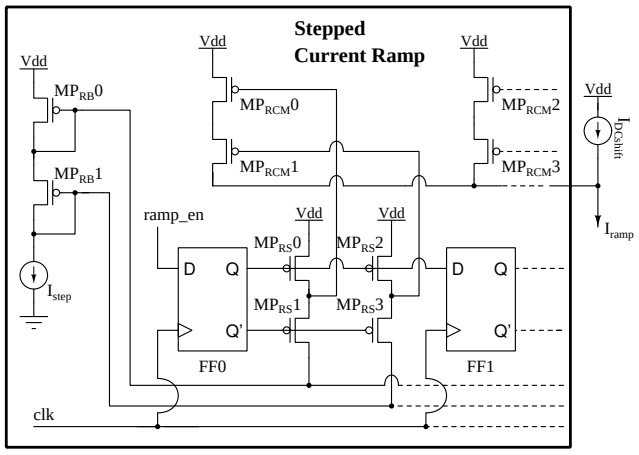

Fig. 4: Stepped Ramp Current Source

A linearly time-dependent current is generated by a series of (cascode) current mirrors, which are biased sequentially using flip-flops (Fig. 4). This biased flip-flop structure creates a stepped current ramp. The biasing current used is the current increment of each step of the current ramp. $MP_{RB}0$ and $MP_{RB}1$ provide the bias voltage as cascoded current sources. Each of the flip-flops of the shift register bias their corresponding current mirroring transistors ($MP_{RCM}0$ and $MP_{RCM}1$ for FF0, $MP_{RCM}2$ and $MP_{RCM}3$ for FF1 and so on) so that they are

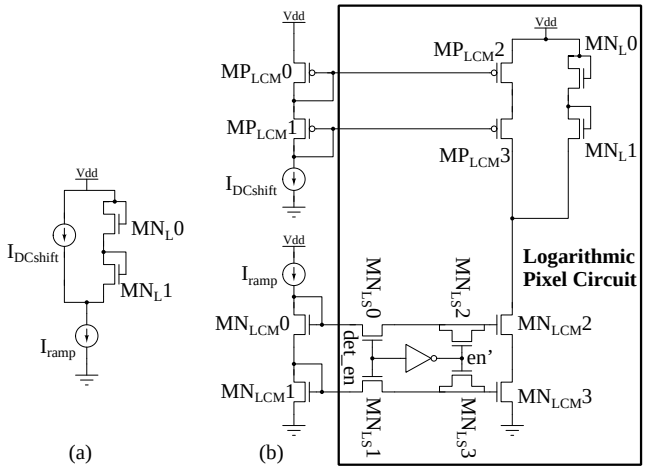

Fig. 5: (a) Model of Logarithmic Pixel (b) Log Pixel Implementation

off when the flip-flop is low and are biased when the flip-flop is active. This results in a sequentially increasing number of mirroring transistors being biased as the shift register operates, creating a stepped current ramp. A larger number of biasing flip flops can be used to get a smooth ramp, reducing the significance of the stepping. As this circuit is present at either the chip level or the column level, it can be made large for better performance without any impact on the pixel-pitch (and thus the fill-factor). An always-on current of $300nA$ is added to keep the subsequent circuit in saturation. This creates a shifted current ramp that varies linearly from $300nA$ to $4\mu A$. The last flip-flop turning on also signifies the end of the logarithmic range. Thus the output signal 'log_end' of the last flip-flop (FF_n) is taken as a start signal for the subsequent linear block.

C. Logarithmic Circuit

The logarithmic voltage is a function of the current through MN_L0. It remains in the subthreshold region for currents up to 4 μA, providing an output swing of $310mV$ (Fig. 2). As the initial current has a very large output swing, it is essential to utilise this range. This becomes a problem as current mirrors can't be in saturation for near-zero current values. Thus a differential approach is considered. A small constant current '$I_{DCshift}$' is supplied to the pixel, which the shifted ramp current dissipates (Fig. 5(a)). The excess current provided (by PMOS current mirror) is made to match the minimum of the current ramp mirror as closely as possible.

The differential design is implemented using cascode current mirrors (Fig. 5(b)). $MP_{LCM}0$ and $MP_{LCM}1$ constitute a cascode current mirror for providing the '$I_{DCshift}$' mirrored in each pixel (by $MP_{LCM}2$ and $MP_{LCM}3$). A switched cascode current mirror mirrors the ramp current (mirrored by $MN_{LCM}0$, $MN_{LCM}1$ at $MN_{LCM}2$, $MN_{LCM}3$). The switches $MN_{LS}0$ and $MN_{LS}1$ are low leakage (high V_T) NMOS switches. When the enable is high, the ramp current is mirrored; thus, the voltage generated changes logarithmically. As soon as the enable goes low, the switches turn off, disabling any change to the gate

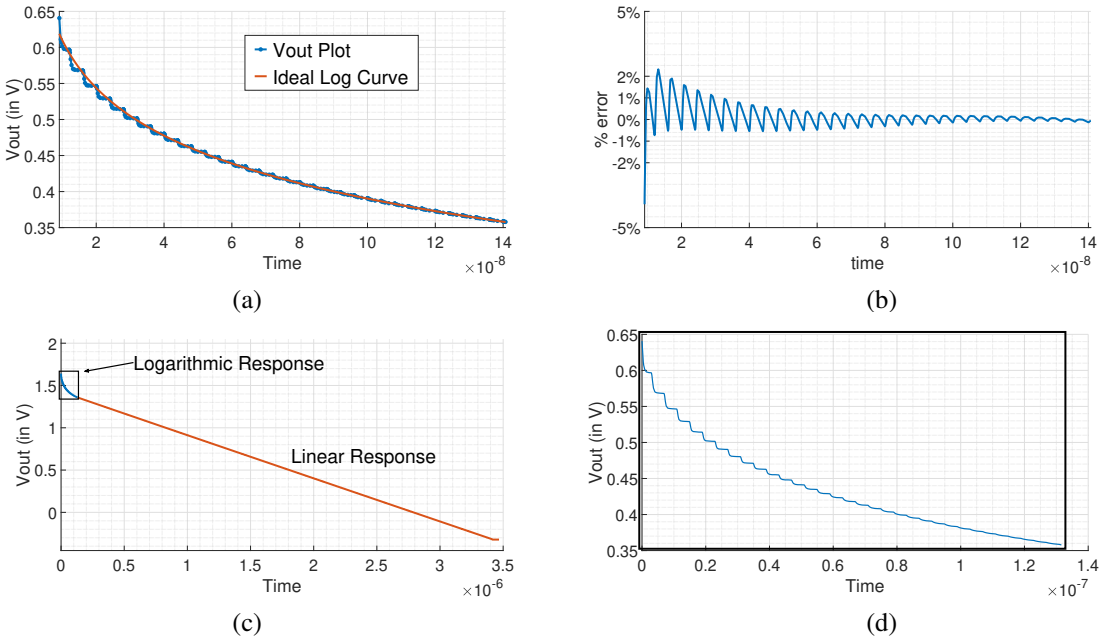

Fig. 6: (a) Achieved log response and ideal log curve (b) Percent error from ideal (c) Full-scale voltage response of pixel (d) Expanded view of logarithmic response

voltages of $MN_{LCM}2$ and $MN_{LCM}3$. The gate capacitance thus stores the bias voltage of the moment when the enable goes low. Thus the mirrored current (and consequently the logarithmic voltage) holds its value as it was at the instant of the 'det_en' signal going low. Dummy transistors $MN_{LS}2$ and $MN_{LS}3$ are implemented to mitigate the issue of the bias changing due to clock feed-through.

III. Pixel Operation and Results

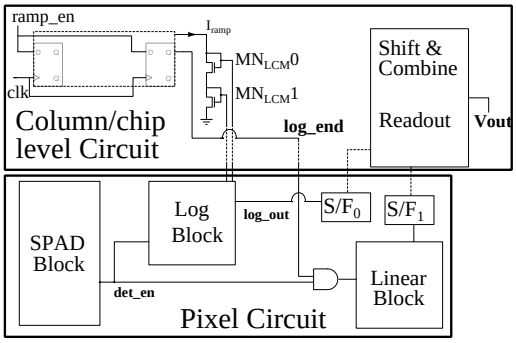

Fig. 7: System Level Design of Pixel

The system-level block diagram for the proposed pixel is shown in Fig. 7. A linear TAC circuit is implemented (as the linear block) from [15] to achieve a linear response after the logarithmic response. This circuit is configured with a low current to provide a long-range (at a low resolution). This circuit is activated after the logarithmic circuit reaches its FSR. This signal 'log_end' is received when the stepped current ramp circuit's shift register overflows. The AND of 'log_end' and 'det_en' is the enable signal for the linear circuit, thus giving us a logarithmic response initially and then switching

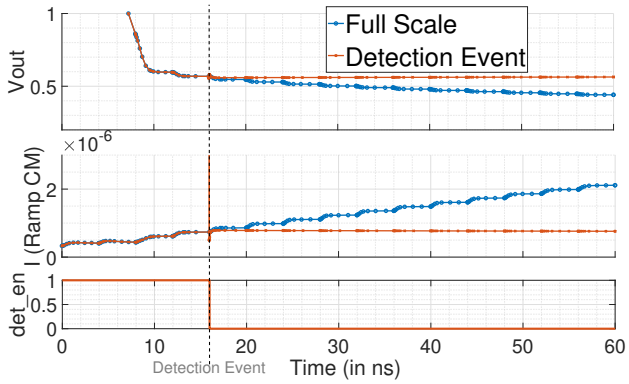

Fig. 8: Pixel response to photon incidence during logarithmic operation

to a linear response (as seen in Fig. 6(c) and Fig. 6(d)) Thus the linear circuit operates only after the FSR of the logarithmic circuit and stops when a photon is detected, or the FSR of the entire pixel is achieved, whichever occurs first. 'ramp_en' is an active high enable signal for the entire circuit, input at the shift register. Its pulse width is chosen such that the output of the shift register ('log_end') goes low after the FSR of the whole pixel. If a photon is incident when the circuit is operating in the logarithmic region, the logarithmic circuit holds the current ramp value (and consequently the voltage) at the instant of detection. The linear circuit is not activated as 'det_en' will be low hereafter (till the next 'start' signal to the SPAD block). The pixel's response to a detection event is shown in Fig. 8.

Assuming that an 8-bit ADC is implemented with the least count of 7.7 mV, the operational performance of the pixel is estimated. This pixel achieves a maximum resolution of 16

Parameter	This Work	2014 [13]	2021 [15]	2019 [7]	2011 [12]
Technique	TAC	TAC	TAC	TDC	TDC
CMOS Technology (nm)	65	130	180	180	350
Dynamic Range (FSR)	3.33 μ s	80 ns	20 ns	330 ns	160 ns
Dynamic Range (Distance)	500 m	12 m	3 m	50 m	24 m
ToF Resolution (Log/Linear)	106.6 ps-1.51/15.1 ns	NA / 93 ps	NA / 29 ps	NA / 48.8 ps	NA / 10 ps
Depth Resolution (Log/Linear)	16mm-172/226 cm	NA / 13.95 mm	NA / 11.76 mm	NA / 7.32 mm	NA / 1.5 mm
Min.Depth	16 mm	13.95 mm	11.76 mm	7.32 mm	1.5 mm

TABLE I: Comparisons with other state-of-the-art Pixels

mm (106.6 ps) in logarithmic operation, with the resolution relaxing to 172 cm (11.5 ns). The linear circuit is configured so that the pixel achieves an FSR of 500 m. The linear resolution thus achieved is 226 cm. The minimum measurable range by the pixel is 16 mm. The R^2 achieved by the logarithmic design when compared to an ideal logarithmic curve (Fig. 6(a)) is 0.9989 indicating that the achieved curve follows the ideal very closely. The maximum deviation of the logarithmic voltage from an ideal logarithmic curve is 2.5% to -0.5% as seen in Fig. 6(b).

IV. Conclusion

This work presents a compact compressive LiDAR pixel with multi-mode operation, which utilises a logarithmic design approach to achieve a high resolution (16 mm reducing to 172 cm) at lower ranges (upto 19.5 m) and switches to a linear circuit with a relaxed resolution (226 cm) for long-range measurement (upto 500 m).

Fig. 9: Layout of logarithmic circuit. Dimensions:8 μm×6 μm

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