A back-illuminated full-frame low-noise HDR 8µm, 12Mpixel, 34fps image sensor for industrial, medical and scientific applications

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***Abstract* —** The need for a low-noise, high-dynamic range (HDR), high-resolution, back-side illuminated (BSI) sensor with a frame rate level that allows video applications for next-generation X-ray medical, scientific, and industrial equipment has been identified. Such a sensor will allow reductions in the radiation dose received by patients in medical applications and use of the sensor in low-light conditions while increasing the image resolution. It will make possible fluoroscopy and X-ray video in some healthcare and industrial applications where it is not used presently. To this end, a BSI stitched sensor with HDR, 8µm, CDS-capable pixels has been designed. The sensor has 12M pixels and can be readout at a frame rate of 34fps. The sensor is amenable to many other industrial and scientific applications that can benefit from its 1.5 e- (rms) noise level.

I. INTRODUCTION

2D and 3D radiographs are an indispensable diagnostic tool in healthcare. Consequently, annual per-capita effective doses from radiologic and nuclear medicine procedures have increased about 2,467% between 1980 and 2017. Absorbed doses from medical and dental radiography have declined by more than 60% in recent years because of reductions in x-ray kilovoltage peaks (kVp) and the introduction of front-side-illuminated CMOS digital sensor technology, among other developments. However, effective radiation doses of cumulative medical and dental imaging examinations of patients are still too high. In addition, image resolution of the available technology is not high enough to provide the level of confidence required to avoid a significant quantity of diagnostic errors.

The range of x-ray tube currents has not been taken into consideration as a way of reducing radiation dose so far. The major challenge of decreasing current level in X-ray imaging systems is the quantum noise phenomena. However, previous studies show a significant improvement in medical image quality compared to existing equipment by using BSI sensors, pixel sizes in the range of 6µm-11µm and microlenses [1][2].

This paper presents a low-noise, high-resolution, high pixel count, BSI sensor with microlenses that will allow moving medical and dental diagnostic beyond the state-of-the art. The sensor features will also enable its use in scientific and industrial applications that require similar characteristics. For X-ray applications the sensor will be coupled to a scintillator.

Making sensors able to provide higher quality image with lower radiation levels also opens the door to the use of X-ray video (fluoroscopy) in new medical and dental procedures. Similarly, the sensor presented can be used in industrial and scientific applications that require high quality video at low light levels.

II. SENSOR OVERVIEW

The sensor presented has been manufactured with Tower Semiconductor 180nm CIS process. The top-level block diagram is shown in Figure 1. The sensor features 3000 columns x 3864 rows of pixels with a pitch of 8µm. The pixel is based on a 6T pixel architecture that allows HDR operation with Correlated Double Sampling (CDS). The pixel is described in section III. The size of the focal plane array is 24.0mm x 30.9mm, whereas the die size is 25.5mm x 37.1mm. The row-drivers are implemented with a compact design and layout to reduce the die area, as required in some medical applications.

The sensor has one pixel output line per pixel column routed towards the south-side of the sensor periphery. The pixel output lines are funnelled in the periphery through an array of Programmable Gain Amplifiers (PGA), Sample and Hold stages (SH), and column-parallel ADCs. Then, the digital data is shifted into a buffer, serialized, combined with clock alignment and

data alignment patterns and, finally, fed to the sub-LVDS output data transmitters. There are 5 sub-LVDS output data channels that can operate at a maximum speed of 1.2Gbps and 1 clock output, for systems that required a clock-synchronous interface. Power and I/O pads are located only on the south-side of the die. This allows having the perimeter of the packaged sensor to be very close to the edge of the focal plane on 3 sides of the sensor.

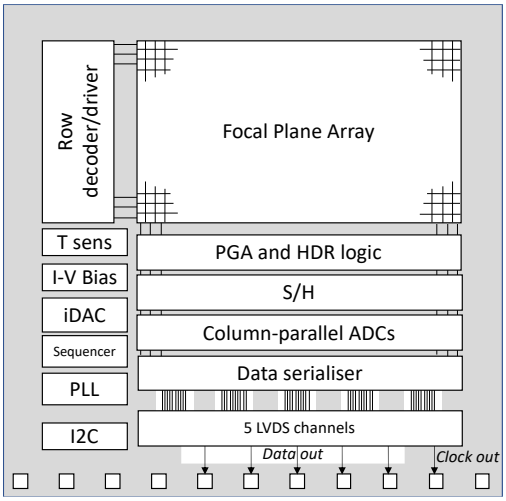

Figure 1. Sensor top-level block diagram.

The sensor includes all the internal logic to control its operation with a digital sequencer. The operation is highly configurable through an I^2C serial interface. In addition to the 2-wire serial bus, only power and ground lines and a low-speed (default: 25MHz) reference clock are needed from the system. The high-speed clock for the 1.2Gbps LVDS output data channels is generated on-chip with a ring-oscillator-based PLL. The output of the same clock generator goes through a clock divider block to generate the sequencer and ADC clocks. All ancillary blocks such as the programmable current biasing network with current and voltage references and current DACs and a temperature sensor are also included on-chip.

The 12M pixel sensor achieves a frame rate of 34fps in HDR mode and 40fps in dual-gain (DG) mode. These numbers are limited by the position of the IO pads (only on the south-side of the sensor) and the form factor with 30% more rows than columns. These characteristics are required by some of the target applications of the sensor. Using the same circuit blocks but with a different focal plane form factor and having pads in more than 1 side of the sensor would allow significantly higher frame rates.

The specifications are summarized in Table 1. At the time of writing, the sensor is still in manufacturing, thus the specifications given are based on design parameters and simulation results.

Table 1. Sensor specifications

Technology	180nm CIS
Number of pixels	3000 x 3864
Effective focal plan size	24.0mm x 30.9mm
Die size	25.5mm x 37.1mm
Pixel pitch	8µm
HDR	Yes
Noise [e-rms]	1.5 e-rms
FW	≥ 65 ke-
Dynamic Range	92.7 dB
ADC on chip	12 bit
Data output interface	5 LVDS @ 1.2Gbps
Frame rate	34 fps @ full frame (HDR) 40 fps @ full frame (DG)
Stitching	Yes

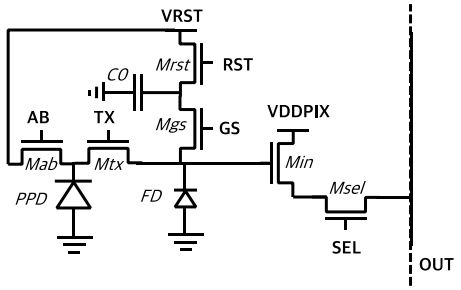

Figure 2. 6T pixel schematic

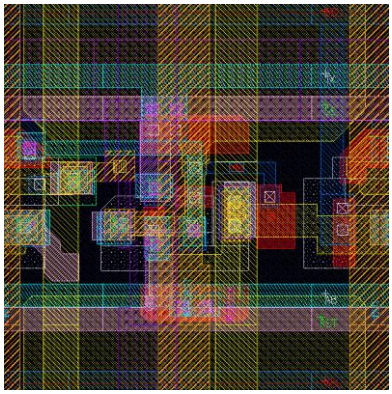

Figure 3. Pixel layout.

III. PIXEL

The schematic and layout of the pixel are shown in Figure 2 and Figure 3, respectively. The pixel size is 8µm x 8µm. The pixel uses a 6T pixel architecture with lateral overflow capacitors. This enables HDR operation of the pixel. The pixel has two possible gain levels. The Mgs transistor is driven always at a low voltage level during signal integration or pixel reset reading for CDS. After the TX pulse, the signal is first read with the pixel in High Gain (HG). For this, transistor Mgs is driven with a low gate voltage. In this configuration, when the PGA further down the readout chain in the periphery is set to its maximum gain of 8

(linear), the total readout noise is 1.5e-rms. In HDR mode, after the HG reading the gate of transistor Mgs is driven to a high-voltage and the pixel is read in low gain (LG). In this configuration, the pixel has higher noise and a higher full-well (65ke).

The sensor can be configured to work in HDR mode or in dual-gain mode. In this second mode of operation the pixels are read with a fixed gain setting, either LG or HG. In this mode higher frame rate can be achieved if the pixel timings are modified such that only LG or HG reading is done after reset reading for CDS.

IV. READOUT ARCHITECTURE

The signal readout architecture in the south side of the sensor periphery is shown in Figure 4. The first stage in the readout chain following the pixel matrix is an 8-level programmable gain amplifier (PGA). In HDR mode the gain of the amplifier is adjusted automatically depending on the pixel signal strength between two pre-selected gain settings. For LG the default PGA gain is 1, whereas for HG the default gain is 8. These defaults can be modified by the sensor application through the I^2C interface.

The HDR-logic circuit will set the gain bit (GBIT) signal HIGH if the output of the PGA is saturated when reading the pixel in HG. The HDR logic output is controlled by the sensor timing sequencer in dual-gain mode.

In order to achieve higher data rate, the Sample & Hold (SH) stage has two storing capacitors operated in ping-pong (SH1 and SH2). The ADC conversion of one row signal (N) is pipelined with the signal analog settling from the next row (N+1).

In HDR mode, for each row, one of the SH capacitors first samples the HG gain reading of the pixel at the PGA output. If the output of the PGA is higher than a programmable VREF_GBIT saturation limit, then, when reading the pixel in LG, the same SH capacitor will sample the LG reading (the HG sample will be lost). If the PGA is not saturated during HG read, then the LG sample is not stored in any SH capacitor and this is the reading which is ignored. The ADC only does one conversion per pixel. When the pixel reading in HG is above the saturation limit the ADC will convert the LG pixel signal. Otherwise, it will convert the HG signal. An example of this sequence is show in Figure 5. It also shows the SH stage ping-pong operation. In this example, the pixels in row N for a given column receive a strong signal that requires LG, whereas pixels in row N+1 receive a weaker signal that requires HG.

The dual-gain mode operation is shown in Figure 6. In this case, the readout chain in the periphery only receives the LG or the HG reading of the pixel as configured through the serial interface of the sensor.

The last stage in the readout chain in Figure 4 is a 12-bit incremental sigma-delta ADC. The GBIT is added to the ADC output code for each conversion to indicate the pixel and PGA gain used for this reading. The final 13bit code will be used by the system host for HDR pixel value reconstruction. The design of the ADC is similar to the one presented in [3].

V. DATA SERIALIZATON AND STREAM-OUT

The 5 readout channels in the sensor are each assigned to 600 ADCs and composed of a 600:16 multiplexer, a 16 words' buffer, a serializer and a sub-LVDS output, as shown in Figure 7.

After the ADCs have completed the conversion, the 12-bit result is stored in buffers internal to each ADC. In HDR mode, the GBIT is also sampled into the buffer. This sampling allows the pipelining of the ADC conversion with the data stream-out, as shown in Figure 5 and 6. The ADCs are subsequently accessed in groups of 16 at a time via a 600:16 multiplexer (since 600 is not a multiple of 16, the last selection includes 8 ADCs instead of 16), and their data is shifted out and stored in a 16 words' buffer. The total size of the buffer is configurable 12x16 or 13x16 depending on whether the selected mode is dual-gain or HDR, respectively. After storing the data into the buffer, it is shifted out to the serializer and ultimately streamed out by the sub-LVDS driver at 1.2 Gbps at double-data rate. The storage of data from the $N+1^{th}$ group of ADCs and the stream-out of the data from the N^{th} group are pipelined, allowing a seamless data stream, as shown in Figure 8.

VI. CONCLUSION

The use of smaller pixel sizes than is common in medical and dental sensors, a low-noise HDR pixel, high-data rate throughput, BSI technology and microlenses in the sensor presented will increase patient safety by reducing overexposure to radiation while increasing diagnostic confidence. The sensor does not only target the medical and dental markets but it can also be used in industrial and scientific applications that need low-noise and high-dynamic range operation. The sensor is stitched so other sensor sizes can be manufactured with the same mask set.

VII. REFERENCES

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[3] M. Sannino, A. Bofill-Petit, G. Pinaroli and R. Turchetta, *A high dynamic range, 1.9 Mpixel CMOS image sensor for X-ray imaging with in-pixel charge binning and column parallel ADC*, IISW 2019.

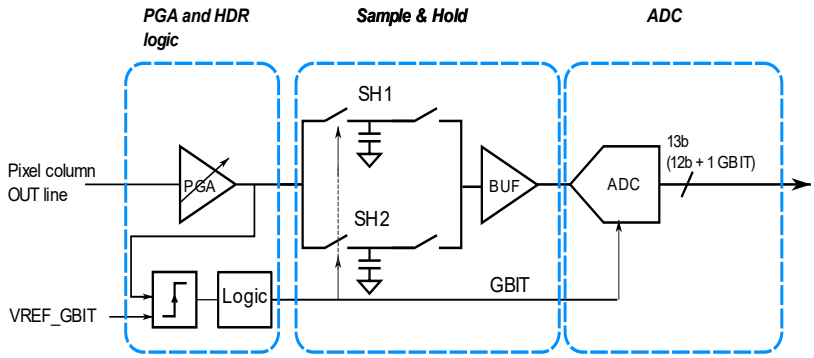

Figure 4. Readout architecture

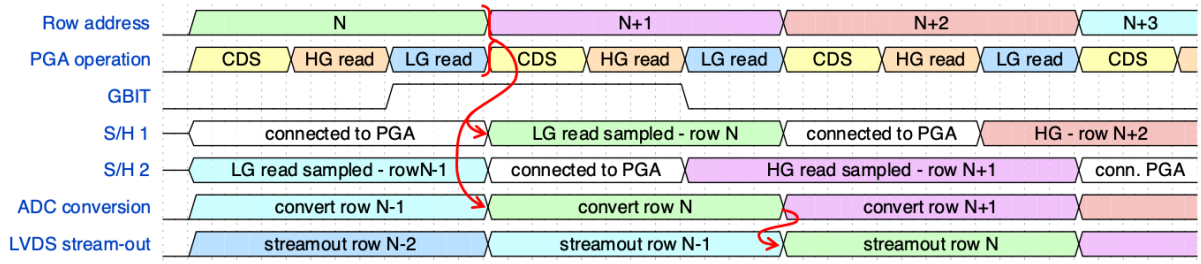

Figure 5. HDR readout operation.

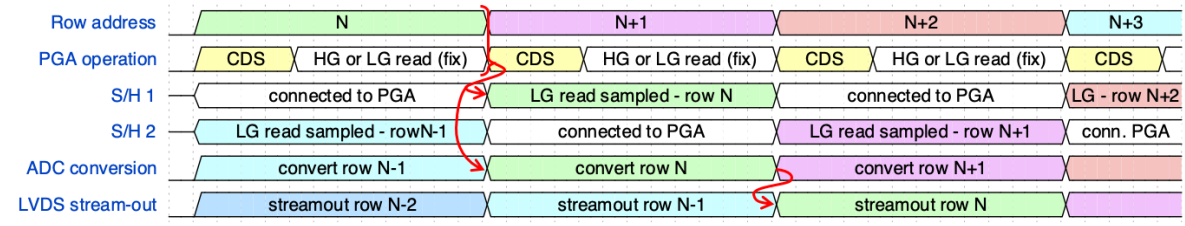

Figure 6. Dual-gain readout operation.

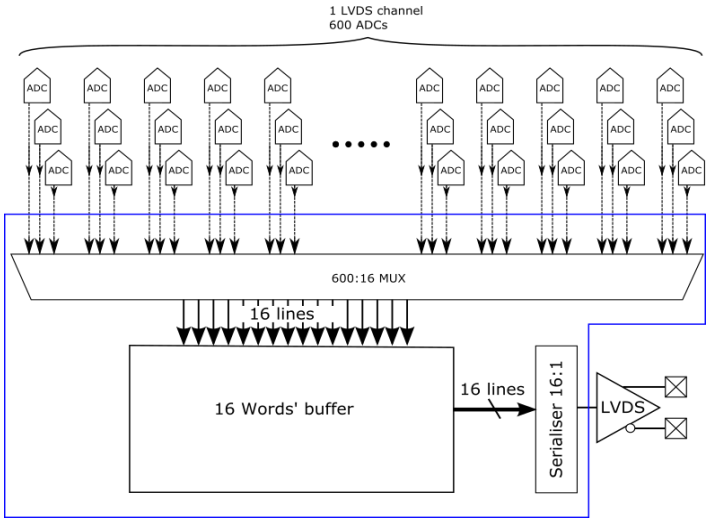

Figure 7. Data serialization and streamout architecture

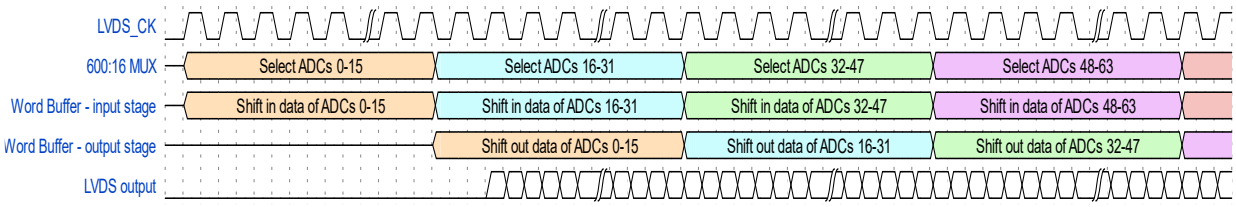

Figure 8. Data serialization operation