Front- / Backside Illuminated Low Noise Embedded CCD image sensor with Multi Level Anti Blooming functionality

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***Abstract*— This paper presents a 320 columns x 128 lines Time Delay and Integration (TDI) image sensor with an embedded charge-coupled device (eCCD) structure fabricated in a 0.35 µm high voltage CMOS process. The paper focuses on the noise characteristics of the sensor analog readout chain and presents an analytical model for effective noise reduction down to an equivalent input noise (ENC) of 20 e^-. The TDI sensor utilizes bidirectional charge shifting and additional excess charge draining by the pixel reset transistor. These techniques provide an effective anti blooming capability, which together with the optimized noise characteristics offers a dynamic range of 13 bit.**

Keywords—noise; conversion gain; correlated double sampling; time-delayed integration; charge-coupled device; responsivity; photon transfer curve; signal-to-noise ratio; blooming; backside illumination; frontside illumination;

I. Introduction

Commencing with a brief illustration of the target application specification, the paper introduces the eCCD cell and the analog readout path constituting the key building blocks of the TDI sensor. The subsequent sections address the bidirectional charge shift implementation followed by a noise model of the full analog signal path emphasizing the effectiveness of correlated double sampling (CDS). The paper concludes with a presentation of measurement results covering a Photon Transfer Curve (PTC) method based noise characterization and the bidirectional charge shift functionality showing its impact on TDI-linearity.

II. Earth Observation Boundary Conditions

Satellite-based earth observation systems are required to detect and distinguish low reflectivity objects under high background irradiance conditions (typically sunlight). Imaging systems utilizing CCDs thus have to offer high intrascene dynamic range (DR), high signal to noise ratio (SNR) and optimum scene contrast resolution capability [1]. High DR is given by maximizing the full well capacity (FWC) of the CCD cell. High SNR is provided by operating the CCD sensor in time-delay integration (TDI) mode. Sensor contrast resolution is directly related to its full well capacity (FWC) and disturbing charge (dark current, blooming charge). In order to cover a large viewing area, earth observation satellites are operating in the exosphere, at orbital altitudes of approximately 600 km. Resolving ground objects of less than a buildings size requires a ground speed distance (GSD) of less than 1 m. Assuming a focal length of 8 m, a pixel pitch of 7 µm would result (Fig. 1). Gravitational and centripetal force equilibrium requires a satellite ground speed (GS) of 7.1 km/s. For the TDI sensor to be in synchronization with its ground speed, the TDI line frequency f_{line} calculates according to (1).

$$f_{line} = \frac{GS}{GSD} = \frac{7{,}100\ ^m/_s}{0.5\ m} = 14.1\ kHz \qquad (1)$$

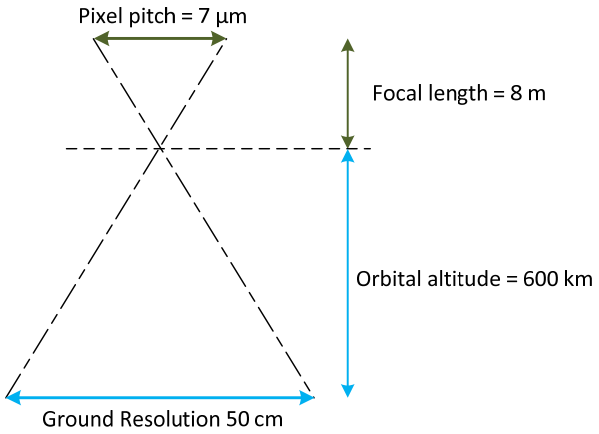

Fig. 1. Ground resolution (600 km orbit)

The targeted TDI sensor performance parameters are summarized in TABLE I. and further discussed in the following sections.

TABLE I. TDI sensor key performance parameters

Parameter	*Variable*	*Value*	*Unit*
Dynamic Range	DR	13	bit
Pixel Pitch	p	7	µm
Line rate	f_{line}	14.1	kHz

III. TDI SENSOR BUILDINGN BLOCKS

The pixel geometry is given by the input requirements GSD and orbital altitude. Starting with the eCCD cell design, the following subsections introduce the circuit solution concepts.

A. CCD cell design

The high voltage regime of our 0.35 µm eCCD process allows a maximum potential difference of 16 V. For a square 7 µm x 7 µm pixel, a reduced eCCD column is numerically modeled using Synopys TCAD™. Fig. 2 depicts the potential profile when the pixel carries a full well capacity (FWC) of 168 ke⁻, ensuring that the photocharge does not get into contact with the surface.

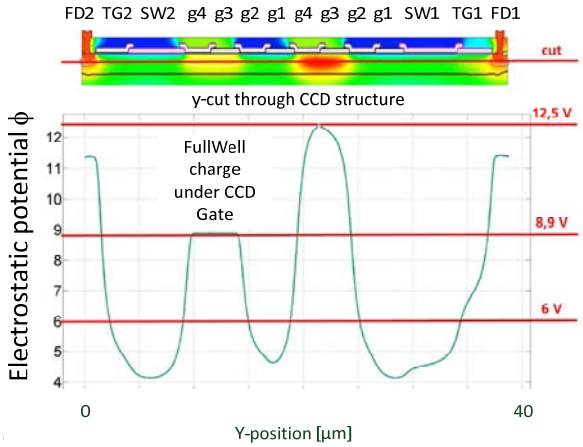

Fig. 2. CCD column potential profile at FWC. g1-4 denotes the individual 4-phase gates within a single pixel. TG1/2, SW1/2, FD1/2 denote the transfer gates, summing wells and floating diffusions adressable for bidirectional charge shift, respectively

Utilizing a 4-phase trapezoidal shaped TDI charge shift clock, the charge distributes under 2 gates at any time within a line cycle (Fig. 3).

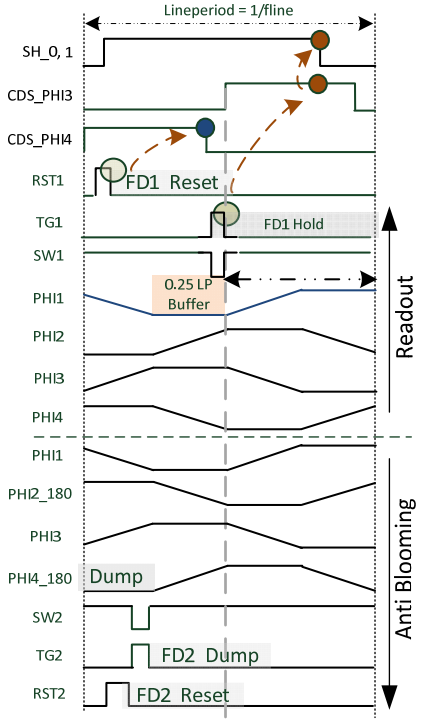

Fig. 3. Bidirectional charge shift in conjunction with CDS

CCD gates g1…g4 are fed with shift sequence PHI1 … PHI4. Excess charge (i. e. not belonging to the programmed TDI depth) is drained to the opposite side (either FD1, or FD2) by applying g2, g4 with the respective inverted signal PHI1-180, PHI4-180. Bidirectional TDI shift is employed by swapping readout / dump side through selection of summing wells (SW1/2), transfer gates (TG1/2) and floating diffusions (FD1/2). The voltage levels are set according to TABLE II.

TABLE II. ECCD GATE OPERATING LEVELS

Node / Gate	*Vmin [V]*	*Vmax [V]*	*Remark*
Floating Diffusion (FD1, FD2)	0 … 8	12	Reset voltage, Fill & Spill
TDI Gate (g1 … g4)	-3.5	+6.5	Charge shift
Summing Well (SW1, SW2)	-3.5	+6.5	Charge collect and buffer
Transfer Gate (TG1, TG2)	-4.5	-3.5	Charge transfer to FD

Fig. 4 depicts the column readout circuit of the eCCD element. Our eCCD process offers full CMOS integration together with the 16 V high voltage domain of the CCD structure.

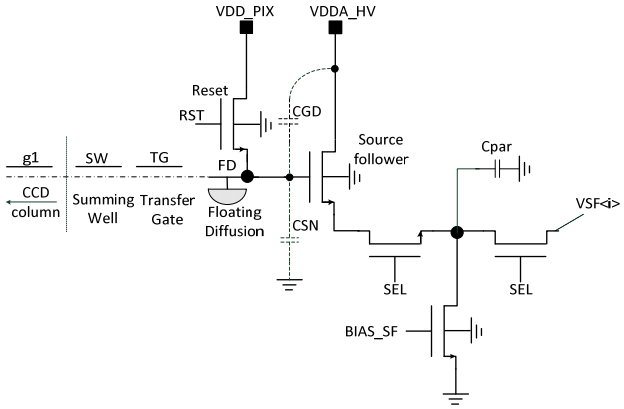

Fig. 4. eCCD column readout circuit (at top and bottom of each column)

Upon transfer from SW to FD via TG, the accumulated photocharge discharges the previously reset FD sense node capacitance (CSN). The resulting voltage (V_FD) is buffered by a high voltage source follower and fed to a correlated double sampling readout stage (CDS, discussed in the next section).

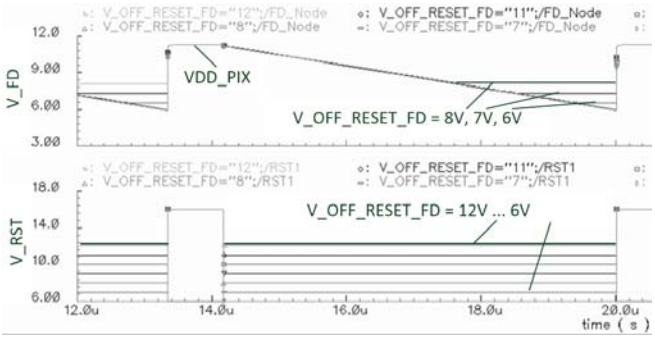

Fig. 5. Anti blooming function of pixel reset transistor. Top figure shows FD node potential, Bottom figure shows reset transistor gate voltage

Depending on the applied “V_OFF_RESET_FD”-Level, the reset transistor acts as an anti blooming gate, whenever the

FD potential becomes less than V_OFF_RESET_FD minus the reset threshold voltage. Fig. 5 shows a parametric simulation with the FD node (top waveform) being "pinned" depending on the OFF-Level of the reset transistor.

B. CDS Readout design

CDS operation is given by sampling a "reset" value onto a sampling capacitance (CS), followed by a "signal" value with the differential charge finally being transferred onto a feedback capacitance (CF) according to (2).

$$VCDS = \frac{C_S}{C_F} \cdot \left(VSF_{reset} - VSF_{signal}\right) + Vrefcds \qquad (2)$$

In the context of the eCCD, CDS is employed by resetting FD1 (RST1 being "HIGH" & CDS_PHI4 active) prior to charge transfer (TG1 being "HIGH" & CDS_PHI3 active, Fig. 3, Fig. 6).

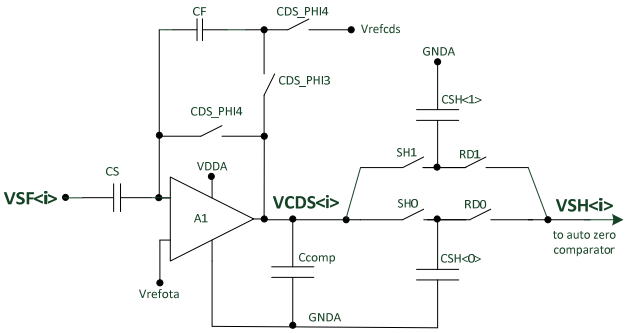

Fig. 6. Correlated double sampling (CDS) stage with Sample & Hold

CDS effectively cancels out the thermal noise of the pixel reset transistor, which is dominant for a carefully designed analog readout path [2]. According to TABLE I. , the intrascene DR is given by the ratio of FWC and equivalent noise charge (ENC) at the input node (CSN). The ENC is gained by referring the total noise voltage $V_{n,out,tot}$ at the imaging system´s output (which can be measured by PTC method [3]) to the total gain of the analog readout path, according to (3).

$$ENC = \frac{V_{n,out,tot}}{{}^{CS}/_{CF} \cdot ASF \cdot CG} \qquad (3)$$

Conversion gain ($CG = \frac{{}^{q_e}/_{e^-}}{CSN}$) and source follower attenuation (ASF) are constrained by FD layout, parasitic wiring and source follower gate area. The sense node capacitance constitutes of about 1/3 FD well capacitance, 1/3 parasitic wiring and 1/3 SF gate area, leading to a total value of 20 fF, i.e. a conversion gain (CG) of 8 $\frac{\mu V}{e^-}$.

$$V_{n,dark} = \sqrt{\frac{TDI \cdot t_{int} \cdot q_{e^-} \cdot I_{dark} \cdot ASF^2 \cdot \left({}^{C_S}/_{C_F}\right)^2}{CSN^2}} \qquad (4)$$

Given a FWC of 168 ke$^-$ and a DR of 13 bits or 8192 gray value steps, the input referred noise has to be less than 21 e$^-$, hence CDS DC-Gain CS/CF has to be derived properly. We chose to employ an analytical noise model, giving the opportunity to evaluate the readout path´s noise contributors individually. Starting with the CCD detecting element, the dark current shot noise is modeled according to (4). High TDI depth´s and slow line rates ("TDI", "t_{int}" in (4)) are driving the dark noise as does the temperature dependent dark current I_{dark}. Dark current characteristic is a matter of careful process definition and control. The temporal noise of the reset transistor is corrected by CDS and given by (5).

$$V_{n,\frac{kt}{C},reset} = \sqrt{\frac{KT \cdot ASF^2 \cdot \left({}^{C_S}/_{C_F}\right)^2}{CSN + \frac{2}{3} \cdot CGD}} \qquad (5)$$

Besides from the sense node capacitance CSN itself, the gate drain capacitance CGD of the source follower is band limiting in favor of kT/C noise reduction (cf. Fig. 4), which also holds for the reset transistor´s partition noise (6).

$$V_{n,part,reset} = \sqrt{\frac{6 \cdot KT \cdot CRES \cdot ASF^2 \cdot \left({}^{C_S}/_{C_F}\right)^2}{\pi^2 \cdot \left(CSN + \frac{2}{3} \cdot CGD\right)^2}} \qquad (6)$$

Partitioning noise scales with the reset gate area (CRES), while also being cancelled by CDS. The active readout chain elements - source follower (7) and CDS stage (8) - impact the thermal noise with their bias settings ratio $\frac{g_{m,Bias}}{g_{m,SF}}$, excess noise factor g and parasitic column capacitance C_{par}.

$$V_{n,therm,SF} = \sqrt{\left(1 + \frac{7}{6} \cdot \frac{g_{m,Bias}}{g_{m,SF}}\right) \cdot \frac{g \cdot KT \cdot ASF^2 \cdot \left({}^{C_S}/_{C_F}\right)^2}{CL}} \qquad (7)$$

Totaling the thermal and kT/C noise of the CDS amplifier and the readout capacitances yields (8).

$$V_{n,CDS} = \sqrt{\frac{2 \cdot g \cdot KT \cdot \left(1 + \frac{C_S + C_{par}}{C_F}\right)^2}{C_S + C_{par} + CH \cdot \left(1 + \frac{C_S + C_{par}}{C_F}\right)} + \frac{KT \cdot (C_S + C_F)}{C_F^2}} \qquad (8)$$

The total rms noise voltage $V_{n,out,tot}$ is dominated by $V_{n,therm,SF}$ and $V_{n,CDS}$ with $V_{n,dark}$ gaining relevance for long exposure times. According to (3), the input referred noise scales with the CDS gain ratio CS/CF, with the CDS compensation capacitance $CH = C_{comp} + CSH$ (cf. Fig. 6).

TABLE III. DESIGN PARAMETERS FOR NOISE ANALYSIS

Parameter (Condition)	*Variable*	*Value*	*Unit*
Dark current	I_{dark}	2	fA
Sense node capacitance	CSN	20	fF
SF attenuation	ASF	0.68	
SF gate drain capacitance	CGD	25	fF
Reset gate capacitance	CRES	6.6	fF
Bias / SF ratio	$\frac{g_{m,Bias}}{g_{m,SF}}$	0.56	
Excess noise factor	g	5/3	
Parasitic column capacitance	C_{par}	2.14	pF
TDI stages	TDI	1, 32, 64, 128	

TABLE III summarizes the associated values. For a set CDS feedback capacitance of CF = 1pF, the input sampling capacitance CS is varied by +/- 10 % from its nominal value (700 fF). The influence on the ENC is shown in Fig. 7.

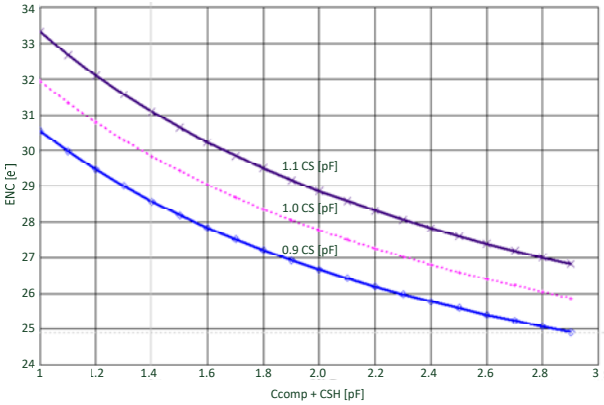

Fig. 7. Input noise vs. total CDS compensation capacitance CH

Above 3pF the ENC is effectively reduced to less than 20 e^-.

IV. 320 x 128 TDI ECCD SENSOR

The realized eCCD image sensor is depicted in Fig. 8.

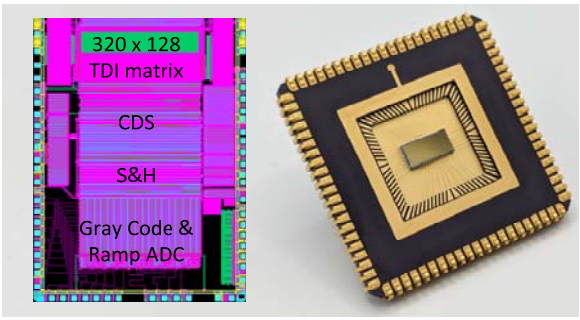

Fig. 8. 320 x 128 TDI eCCD sensor (left: layout, right: chip photo)

A. PTC characterization

The PTC characterization yields a mean camera gain of $K = 6.5 \cdot 10^{-3} \frac{DN}{e^-}$, as shown in Fig. 9.

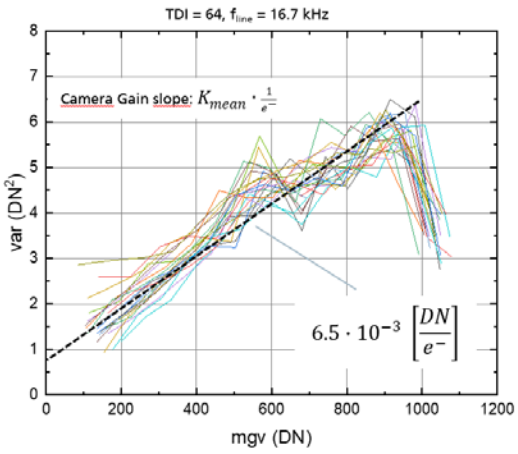

Fig. 9. PTC characterization

The analog readout chain camera gain K is represented by (9).

$$K[\frac{DN}{e^-}] = q_{ADC}[\frac{DN}{V}] \cdot \frac{C_S}{C_F} \cdot ASF \cdot CG[\frac{V}{e^-}] \qquad (9)$$

Rearranging and substituting CG for CSN (3) yields (10).

$$C_{SN}[\frac{As}{V}] = q_{ADC}[\frac{DN}{V}] \cdot \frac{C_S}{C_F} \cdot ASF \cdot \frac{q_{e^-}}{K[\frac{DN}{e^-}]} \qquad (10)$$

Ramp ADC conversion gain is set to $q_{ADC} = 1695 \frac{DN}{V}$. Together with the design parameters in TABLE III. , this confirms the targeted sense node capacitance of 20 fF. The dark noise is less than 1 DN, confirming the noise model.

B. Anti Blooming

Anti blooming measures (AB) incorporate AB functionality of the pixel reset in conjunction with bidirectional charge shift. Sole PTC measurement is insufficient here, since it does not distinguish between blooming and object charges. Only the determination of pixel-to-pixel modulation reveals the evidence of image quality degradation if no anti blooming measures are taken [4]. The PTC measurement characteristics depicted in Fig. 10 prove the correct AB functionality, since the TDI-depth normalized curves yield an equal slope, i.e. a – by definition - TDI-independent responsivity of $R = 3.68 \cdot 10^{-3} \frac{DN}{photon}$.

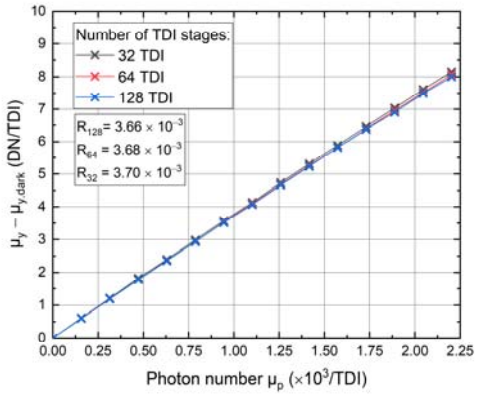

Fig. 10. TDI-depth normalized responsivity

CONCLUSION

An embedded CCD image sensor with high dynamic range, low noise and enhanced anti blooming functionality has been presented. Current development projects are based on the scalability of the low noise analog readout column element for large eCCD detectors (cf. Fig. 8). Bidirectional anti blooming clocking enables backside illuminated imaging in multi spectral earth observation applications, due to its high immunity against disturbing photocharges generated by high background irradiance.

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