High Dynamic Range Pinned Photodiode Pixel with Floating Gate Readout and Dual Gain

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***Abstract*—This paper presents a pixel based on the pinned photodiode (PPD) with high dynamic range achieved via in-pixel dual conversion gain. The pixel operates with a single exposure and a single charge transfer out of the PPD. The signal charge is first converted to voltage non-destructively with low gain using capacitive coupling to a floating gate. A second conversion with high gain follows at a *pn* junction-based sense node after another charge transfer. An increased dynamic range is achieved due to the sensing of the same charge with two different conversion gains. The results from a prototype 10 µm pitch pixel, manufactured in a 180 nm CMOS image sensor process, demonstrate conversion gain ratio of 3:1, dynamic range of 93.5 dB, 2.4 e^- RMS readout noise, and negligible image lag. The pixel can operate in global shutter mode with the same low noise as in rolling shutter due to the intermediate signal storage under the floating gate.**

Keywords—CMOS image sensor, pinned photodiode, high dynamic range, dual conversion gain

I. Introduction

CMOS image sensors with high dynamic range (HDR) are finding use in many applications, such as automotive, surveillance, industrial, and scientific. Among the huge variety of existing HDR methods, those using a single exposure are preferred when motion artifacts must be minimized, for example in automotive imaging [1].

One of the most widely used methods to boost the dynamic range (DR) is to use column-level amplifiers with dual gain [2]. Other types of single exposure HDR imagers implement multiple signal readout paths within the pixel, such as dual photodiodes [3] or multiple conversion gains [4][5]. In-pixel signal storage with lateral overflow integration capacitor (LOFIC) [6][7] offers some of the highest DR because the maximum signal is not limited by the capacity of the photodiode.

Virtually all HDR CMOS image sensors use the pinned photodiode (PPD) as the photosensitive element due to its low dark current and readout noise. The maximum output signal, commonly known as the full well capacity (FWC), is often not limited by the charge capacity of the PPD, but by the available voltage span at the sense node. This is particularly true for larger pixels above approximately 5 µm pitch. For a typical area charge capacity of 4 $ke^-/\mu m^2$, a PPD on 5 µm pitch and 60% fill factor can hold up to 60 ke^-. On the other hand, the voltage span at the sense node cannot be much larger than 1.5 V, which for a modest conversion gain (charge to voltage factor, CVF) of 50 $\mu V/e^-$ corresponds to 30 ke^-. Increasing the CVF further limits the amount of charge that can be converted, and although the DR may be improved due to the lower readout noise, a DR significantly higher than 80 dB is difficult to achieve in this way.

The presented development aims to keep the readout noise low while allowing a much larger part of the charge stored in the PPD to be converted to voltage before signal saturation is reached, thus increasing the dynamic range.

II. Principles of Operation

In the proposed pixel the signal charge is converted to voltage twice following a single exposure and a single transfer out of the PPD: first on a floating gate with low CVF (low gain), and then a second time on a sense node with high CVF (high gain). The two voltage output signals are read out consecutively.

Figure 1 shows a simplified schematic diagram of the pixel [8]. A normal PPD is used as the photosensitive element. Following the transfer gate (TG), the charge passes under a floating sense gate (SG) and an output gate (OG) before reaching the sense node (SN). The MOSFET M1 is used to reset SG to the reference voltage VREF. M2 connects SN to SG so that both can be reset to VREF, and also to allow readout using only one source follower, the M3. M4 is the row select switch. Global reset functionality is provided via the GRST gate, enabling the pixel to operate in global shutter (GS) mode.

An optional *n*-type implant is included under the gates SG and OG with the purpose to move the potential peak away from the $Si\text{-}SiO_2$ interface like in buried channel charge coupled devices (CCD). This is intended to reduce the interaction of the charge with the interface states and to improve the image lag.

The diagram in Fig. 2(a) depicts the potentials in the pixel at the end of the signal integration period, and after both the SG and the SN have been reset to VREF by turning M1 and M2 on. With M1 turned off and M2 kept on, the charge is transferred out of the PPD with the help of a voltage pulse applied to the transfer gate (Fig. 2(b)). The charge is stored under the sense gate while the OG is biased at 0 V to create a potential barrier to the sense node. The signal-induced voltage step on SG is read out via M2, M3 and M4 in Fig. 2(c). This readout path has low CVF due to the large area of the SG and its high capacitance to substrate, and also due to the junction capacitances of M1, M2 and the SN which are all connected in parallel with the SG.

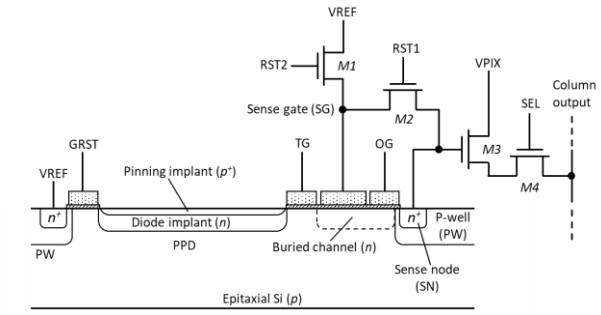

Fig. 1. Schematic diagram of the dual gain pixel.

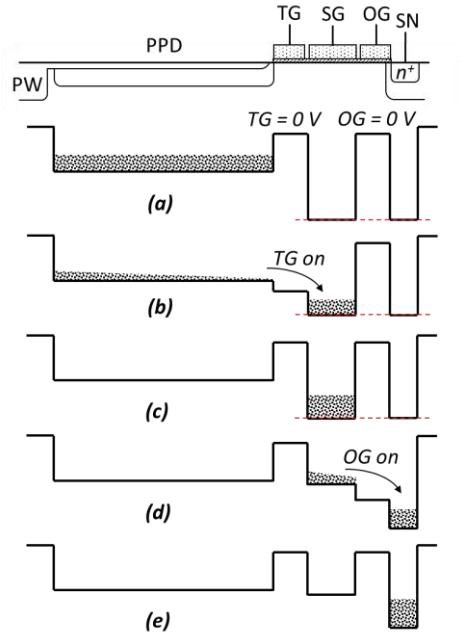

Fig. 2. Potential diagrams in: (a) signal integration with SN and SG under reset; (b) charge transfer from the PPD; (c) non-destructive signal readout at the SG; (d) charge transfer to the SN; (e) signal readout at the SN.

The first readout is non-destructive because the photogenerated signal is kept as a charge packet and is not affected by the process. Following that, the charge is transferred to the sense node for the normal charge-to-voltage conversion on a *pn* junction. First, the SN is reset to the voltage VREF by simultaneously turning on M1 an M2, while the charge is kept under SG. Following that, the voltage VREF is lowered while M1 is on, M2 is off, and OG is biased in a way to create a potential gradient towards the SN, as shown in Fig. 2(d). The charge reaches the SN and the signal is read out in Fig. 2(e). This second readout path has high conversion gain because the capacitance of the sense node is small and M2 is turned off.

III. Design

A prototype pixel with the layout shown in Fig. 3 was included in a test chip together with normal PPD (4T) reference pixels. All were laid on a 10 µm pitch, with each type occupying a 128×512-pixel sub-array.

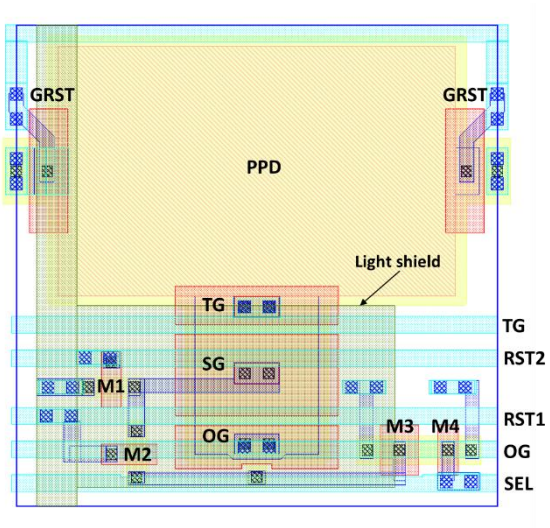

Fig. 3. Layout of the dual gain pixel.

The device was manufactured in a 180 nm CMOS image sensor process using 5 µm thick, *p*-type epitaxial wafers with resistivity of 8 Ω.cmThe estimated charge storage capacity of the PPD is 170 ke⁻. From TCAD simulations of the charge coupling to the SG, and after including all the capacitances from the layout, the expected CVF for the low and high gain paths was calculated as 13.7 µV/e⁻ and 54.2 µV/e⁻, respectively.

The metal track providing the source follower supply VPIX has been enlarged to form a light shield over the SG and the OG.

A distinct advantage of the proposed pixel design is that no changes to the manufacturing process are required if the additional buried channel under SG and OG is not implemented.

IV. Characterisation

The performance of the pixel was characterized in rolling shutter mode readout using the control signals shown in Fig. 4. In addition to the signals required to achieve the operation described in Section II, an optional charge clear was added before the PPD charge transfer. This is used to remove the charge collected under the SG during integration and is identical to the transfer SG-OG-SN shown in Fig. 2(c)-(e).

The sample & hold reset (SHR) is used to store the reset samples in the column circuitry, and SHS does this for the signal samples. Correlated double sampling (CDS) is implemented by storing the output signal voltages in capacitor pairs before and after the corresponding charge transfer, thus eliminating the reset noise for both conversion gains.

Figure 5 shows the photoresponse under visible illumination for the following operating conditions: VREF1 = 2.9 V, VREF2 = 1.0 V, VOG = 1.5 V, VRST = 3.6 V and VPIX = 3.3 V. The conversion gains were determined from the mean-variance photon transfer curve and the external electronic gain at 15.5 µV/e⁻ and 46.8 µV/e⁻ for the low and high gain readout paths, respectively.

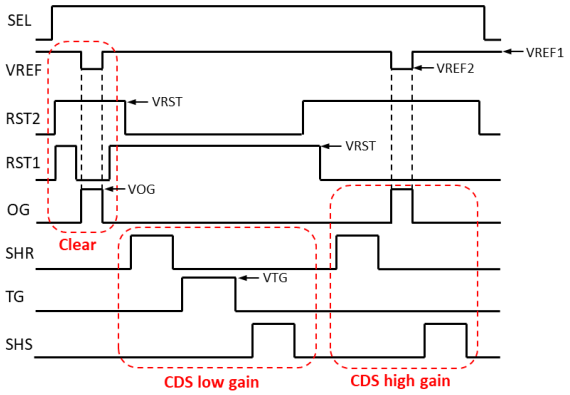

Fig. 4. Timing diagram used for pixel characterization showing the amplitudes of the control signals. The high levels of the signals not indicated are 3.3 V. All low levels are 0 V.

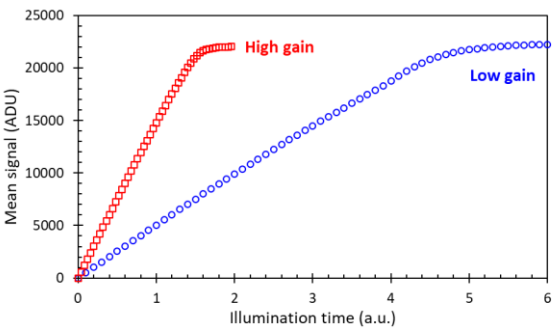

Fig. 5. Photoresponse at both gains. One ADU is 80.1 μV.

The two test images in Fig. 6 were taken under identical illumination and integration times. While the image at high gain in Fig. 6(a) is saturated, the image in Fig. 6(b), taken at low gain, has maximum signal of about a third of the FWC. The pixels having the buried channel implant had very similar characteristics, as can be seen in the right-hand side in Fig. 6.

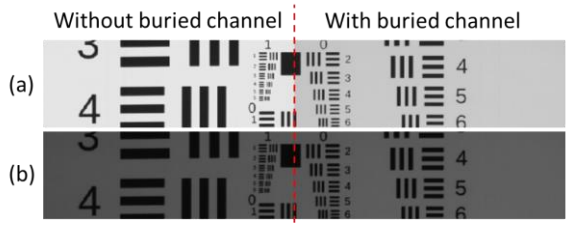

Fig. 6. Test pattern image at high gain (a) and at low gain (b) under the same illumination and readout conditions. The pixels in the left half of the image use surface channel transfer between the PPD and the sense node. The pixels in the right half have a buried channel as in Fig. 1.

The FWC and the readout noise for the low and high gain paths were measured to be 114 ke⁻ and 6.6 e⁻ RMS, and 38 ke⁻ and 2.4 e⁻ RMS, respectively. The gain ratio is very close to 3, and the dynamic range is 47500 (93.5 dB). The readout noise was measured without the shot noise from the dark current. This was accomplished by not pulsing the transfer gate and the OG in Fig. 4. With the dark current included, the noise at high gain rises to 3.6 e⁻ RMS, measured at 20 fps readout rate and 23 °C operating temperature.

In one of the reference 4T pixels the FWC is 22 ke⁻ for a CVF is 68 μV/e⁻, and despite the mean noise being lower at 1.63 e⁻ RMS due to the higher conversion gain, the DR is only 82.5 dB.

The design was characterized only in rolling shutter mode to demonstrate its operating principles, but it can also be operated in global shutter mode. Due to the signal storage under the sense gate, the readout path with high conversion gain accomplishes the same CDS and reset noise suppression as in rolling shutter mode, and should therefore exhibit the same readout noise. The reset noise in GS low gain mode is not eliminated, however this is not critical because at large signals the photon shot noise is expected to be dominant.

If not cleared before charge transfer out of the PPD, the dark current measured at the sense node would include the signal generated by interface traps under the SG because the silicon surface there is not pinned. The dark current in high gain mode as a function of VOG, shown in Fig. 7, indicates that VOG must be higher than 1.5 V for efficient clearing of the dark signal when VREF2 = 1.0 V. Under these conditions, the dark currents in low and high gain modes are nearly identical and are close to the values in the reference 4T pixels.

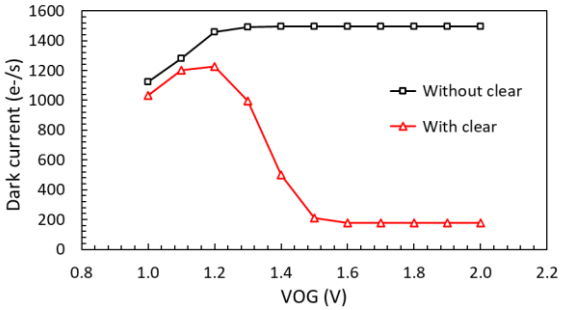

Fig. 7. Dark current in high gain mode with and without initial signal clear at VREF2 = 1.0 V and 25 °C.

Both the leading and the trailing image lag were measured because the initial dark signal clear could create a lag asymmetry. The leading edge lag was calculated as the normalized difference between the signals under steady-state illumination and in the first bright image following several dark images. Similarly, the trailing edge lag is the signal in the first dark image following sufficient number of bright ones, normalized to the signal under steady-state illumination. Experimentally it was established that a series of 5 bright and 5 dark images were more than enough to reach the steady state signal levels, as shown in the inset of Fig. 8.

The transfer out of the PPD was confirmed to be lag-free for VTG > 2.7 V when the TG pulse length is 1.5 μs. For the nominal VTG = 3.3 V the lag is negligible for TG pulses as short as 50 ns. The lag performance is very good because the transfer gate is relatively wide, and so is the SG, which behaves as a large charge collecting element.

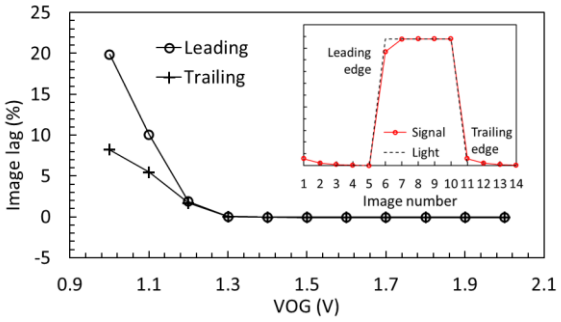

Fig. 8. Image lag as a function of VOG in high gain mode for the bias voltages listed in Section IV and signal at half FWC (≈18 ke⁻) in a pixel without buried channel.

The transfer from the SG to the SN has negligible lag for VOG ≥ 1.3 V as shown in Fig. 8 for pixels without the additional buried channel. At VOG = 1.5 V the low lag performance is maintained even for OG pulse lengths below 100 ns. The pixels implementing a buried channel have relatively low channel dopant concentration, and correspondingly low channel potential. Since the image lag for surface charge transfer pixels is already very low, they do not seem to offer any visible advantages.

V. Conclusion

In this work we present a new PPD-based pixel design using a floating gate to accomplish two consecutive signal readouts with different conversion gains. The pixel operates with a single exposure and a single charge transfer out of the PPD. The first prototype demonstrates significantly increased DR and negligible image lag. Although this implementation is for a pixel on 10 µm pitch, the proposed architecture could be scaled down to smaller pixels. Further improvements to the DR could be achieved by reducing the sense node capacitance and the readout noise, and also by increasing the effective sense gate capacitance. The proposed pixel architecture could be attractive for HDR imagers using single exposure.

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