

# Ultra-sensitive CMOS image sensor capable of operating down to 200 ulx at 60 fps

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*Abstract— This paper presents a 10 $\mu$ m pixel pitch, front side illuminated (FSI), dual electronic rolling shutter (ERS) and global shutter (GS) image sensor with a fully depleted pinned photodiode (FDPD). At 950nm a quantum efficiency (QE) of 45% and a modulation transfer function (MTF) of 54%, Nyquist frequency, is demonstrated. The circuit is operated in a flexible way embedding low level digital processing for image quality improvement such as high dynamic range (HDR) and fixed pattern noise (FPN) correction.*

**Keywords-** CMOS Image Sensor, near infrared, low-light, High Dynamic range, quantum efficiency, MTF

## I INTRODUCTION

The current technology trend for most applications is toward miniaturization of pixels compatible with high-resolution, large format CMOS image sensors. However, low-light applications require sufficient video rate and minimum signal-to-noise ratio (SNR) and spatial resolution to allow human interpretation of a complex scene. In some cases, image processing algorithms are used to enhance video while preserving details in the image [1]. Although the contribution of algorithms is effective, it is necessary that the basic information is as close to reality as possible. In low-light environments, for small pixels, ultra-low readout noise is required [2], while for larger pixels, photon shot noise quickly becomes the limiting factor in detector performance. With small pixels, the digital binning, equivalent to expanding the pixel size, augments the signal while the noise of each is added. For this reason, low light level applications require larger pixel sizes, very sensitive where the noise only contributes once: every photon matters. Therefore, the innovative FDPD was developed to maximise the signal-to-noise ratio and the Near-Infrared MTF at the same time. This work is a continuation of previous achievement [3] [4].

## II CHIP ARCHITECTURE

### A. Pixel structure

The pixel scheme is composed of a pinned photodiode and 5-transistors (5T) addressable by programmable signals allowing to operate either in RS or GS mode with exposure control. The RS mode is suitable for low light level vision requiring low readout noise. The internal sequencer also implements a GS mode with digital double sampling (DDS), alternating a reset frame and an image frame. The subtraction of the images is done off-chip. In this mode the "kTC" noise is minimized within the limit of the integration of the low frequency noise power. It was demonstrated that increasing the thickness of the detector as proposed with

FDPD will also improve the extinction ratio, confirming the benefit of using a thick silicon detector, for GS pixels [5].

### B. Analog-To-digital conversion

The circuitry includes a dual column-wise ADC that enables video rates exceeding 90fps in 12b-ERS and 50fps in 10b-GS (DDS). The ADC architecture is based on a double ramp that enables the conversion of higher pixel signal values. The differential voltage ramps are applied simultaneously on the reset and signal levels by capacitive coupling as represented Figure 1. This approach allows to cover a larger voltage dynamic at the input of the comparator.

### C. On-chip processing

The architecture includes low-level image processing that corrects residual fixed pattern noise with better than bit accuracy and offset suppression without loss of dynamic. The pixel matrix includes shielded columns and rows used to hold respectively the horizontal and vertical FPN value. The sensor embeds row memories for subtracting the FPN values within the data stream. In ERS, it is proposed to perform a high dynamic interframe exposure which is combined with a readout chain including a real time, pixel-wise tone mapping feature. A first short exposure is performed and then transferred to the floating node. Meantime, a second long exposure is integrated in the photodiode. The reading out sequence starts with the sampling of the signal value corresponding to the short exposure and then the reset. The difference is converted with a short ramp and determines when it exceeds a threshold equivalent to the dynamic range of the ADC divided by the ratio of exposures. The next step consists of a decision process of the transfer of the charges integrated during the long exposure, conditioned to the result of the previous comparison. If the threshold value is not exceeded, then the signal of long exposure overwrites the short one. In this case, the correlated double sampling (CDS) fully removes the reset noise and thus maximizes the signal-to-noise ratio in the weak signal range. Using the same approach, the FPN value corresponding to each of the long and short exposures are subtracted accordingly. The processing of the image is thereby made easier because the photon transfer curves are joined without gap, leading to an uncompressed and directly interpretable HDR display. The average temporal noise is reduced to the source follower and the ADC around 1.5 electron rms. The dynamic range with this design is proven at 110dB for an exposure ratio of 30dB.

### III DEVICE STRUCTURE

#### A. Semiconductor process

The FDPD technology is based on 180nm foundry process and cost-effective compared to other approaches [6] [7] [8]. The FDPD principle is based on negative biasing of the bulk with non-zero electrical field in the full epi and the deep depletion enhancement (DDE) diffusion for preventing front-back current leakage (Figure 2). Therefore, the image is sharp and contrasted, the MTF being very close to the theoretical value in combination with a significantly improved QE. The pinned photodiode as well as the vertical n-well-bulk diodes are reverse biased and opposed to the vertical current flow. The p-well delimiting the pixels is connected to the ground. To oppose the direct conduction, the DDE is inserted between the p-wells and the bulk to form a floating NP junction polarized in such a way that it blocks the vertical current. The operation of the readout and processing circuitry is protected from the negative biasing of the bulk by using a deep n-well that creates a p-n junction. The TCAD simulation shown Figure 3 demonstrates that the depletion extends across the entire active silicon in the presence of the VBS static polarization as opposed to the same structure biased to ground. The deep depletion  $W$  is given by the following formula [9]:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_i}{qN_D} \left( \frac{kT}{q} \ln \left( \frac{N_A N_D}{ni^2} \right) + V_{BS} \right)}$$

The two characteristics dimensioning the depletion depth are the doping or resistivity of the silicon and the  $V_{BS}$  voltage. For a depletion of some tens of microns and a voltage of some tens of volts, it is appropriate to consider a silicon doping of few  $1E12$  atoms per  $cm^3$ , as depicted in Figure 4.

### IV MEASUREMENT RESULTS

#### A. Quantum efficiency and MTF

The measurement of the quantum efficiency is performed on an optical bench comprising a monochromatic light source. The results are shown in Figure 5 in comparison with the theoretical calculation and a standard CMOS process implementation. The results are as expected. The gain in sensitivity is significant, especially in the near infra-red region, which is beneficial for the detection capacity in this spectral range, but also for the global SNR under low light level conditions. The MTF is measured using the slanting edge method and a tunnel with an optical aperture  $f/2.8$ . The value shown in Figure 6 is given for a spatial frequency of 50 lp/mm being the Nyquist limit corresponding to the pixel pitch. The effect of improving charge collection and reducing electron crosstalk is clearly visible as a function of polarization. In reference to the ground polarized silicon, this result shows a performance gain on the contrast essentially in the longest wavelengths, corresponding to the deepest penetration of the radiation.

#### B. Low light performance

The low light level performance is evaluated according to the NEI (noise equivalent irradiance) criterion, for a given exposure time and lens aperture. The NEI is calculated considering a color temperature of the light source of 2856K, an average lens transmission of 83% at  $f/1$  and an exposure time of  $1/60$  second. Given the pixel

characteristics, the corresponding integrated photo-response value is  $3 e^-/\mu lx\text{-sec}$  at the sensor plane which gives an equivalent NEI of  $175 \mu lx$  at the scene level. The silicon based NEI at 950nm wavelength is  $29 pW/cm^2$  for exposure time 33ms, making this device among the best in its category with reference to other technologies [10]. Similarly, the irradiance corresponding to an SNR equivalent to 10 dB, which is the minimum for an acceptable image according to the ISO standard, is 1.2 mlx. This level corresponds to the starlight condition.

### V CONCLUSION

The dedicated pixel technology, which includes a fully depleted photodiode in thick, ultra-high resistivity silicon, provides a signal-to-noise ratio sufficient to operate in deep darkness. The dynamic range of a single image reaches 110 dB within the scene, which allows the sensor to be flexible in many operating conditions. This circuit is the first of a new generation of CIS with enhanced performance in the near infrared. For future work, it is envisaged to combine it with a higher silicon thickness and a BSI. This opens the perspective of other applications such as medical imaging or intelligent transportation systems (ITS).

### ACKNOWLEDGMENT

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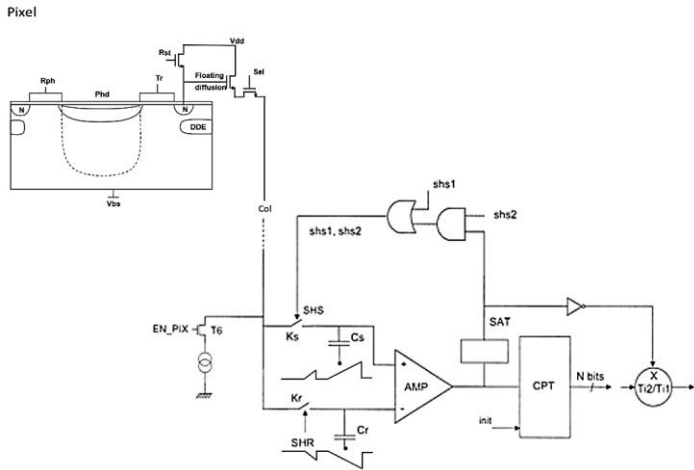


Figure 1 – HDR Pixel processing chain

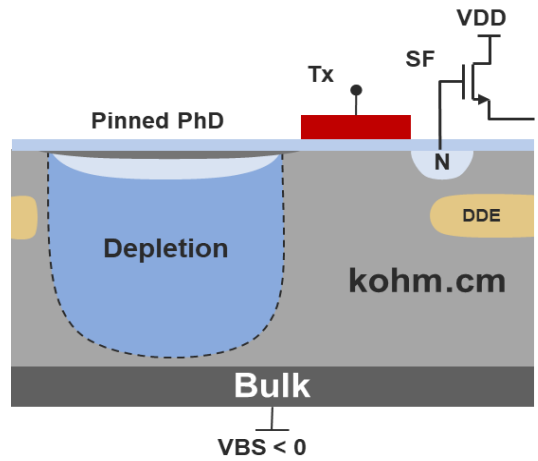


Figure 2 – Pixel structure

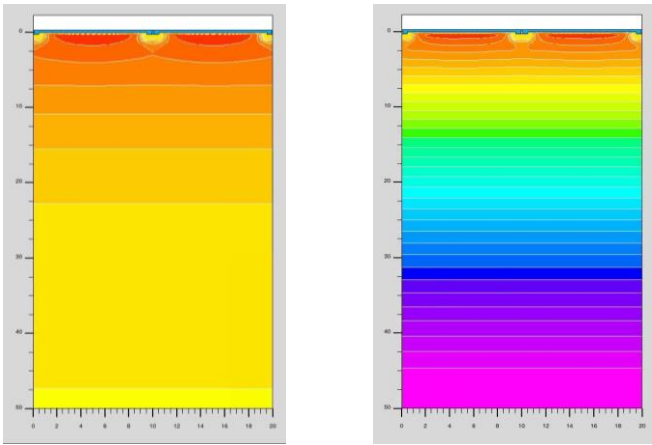


Figure 3 – FDPD equipotential, on the left grounded  $V_{BS} = 0V$ , on the right grounded  $V_{BS} < 0V$

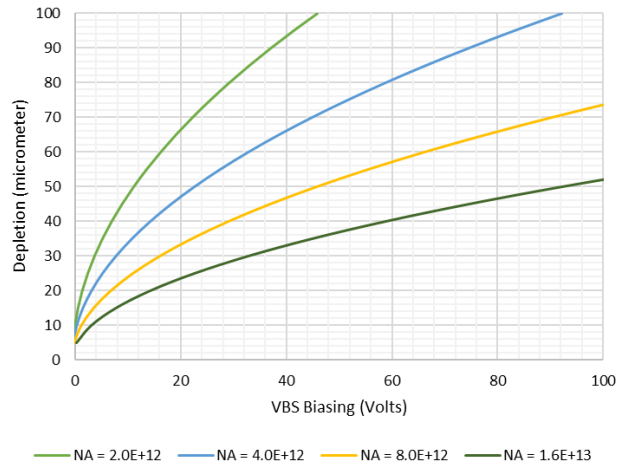


Figure 4 – Depletion depth factors

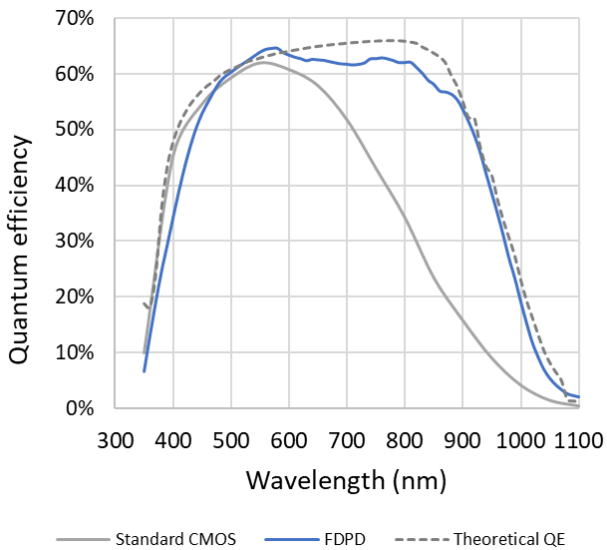


Figure 5 – FDPD Quantum efficiency

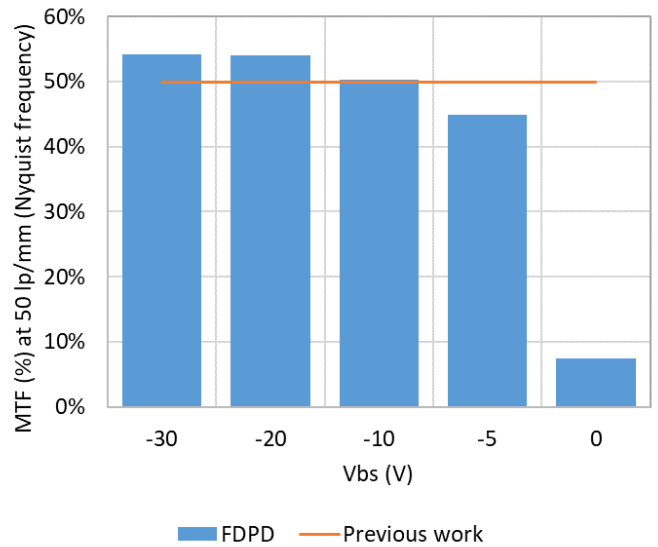


Figure 6 – MTF at 950nm