Evolution of a 4.6 µm, 512×512, ultra-low power stacked digital pixel sensor for performance and power efficiency improvement

Rimon Ikeno, Kazuya Mori, Masayuki Uno, Ken Miyauchi, Toshiyuki Isozaki, Hirofumi Abe, Masato Nagamatsu, Isao Takayanagi, Junichi Nakamura, Shou-Gwo Wuu[†], Lyle Bainbridge[‡], Andrew Berkovich[‡], Song Chen[‡], Ramakrishna Chilukuri[‡], Wei Gao[‡], Tsung-Hsun Tsai[‡], and Chiao Liu[‡],
Brillnics Japan Inc., Tokyo, Japan, [†]Brillnics Inc., Hsinchu, Taiwan, [‡]Reality Labs, Meta Platforms Inc., Redmond, WA, USA
Rimon Ikeno – tel: +81-3-6404-8801, e-mail: ikeno.rimon@brillnics.com

Abstract – We report improvement of a global shutter, stacked digital pixel sensor with 512 × 512, 4.6 µm pixels featuring an overlapped triple quantization scheme. It achieves an ultra-high dynamic range of 127 dB with reduced temporal noise and fixed pattern noise by pixel-design tuning and layout optimization. The new sensor chip achieves low power consumption of 5.8 mW, which is comparable to the original chip by design and operation optimizations despite the newly integrated voltage regulators for pixel power supply and pixel-control signals in the same die size as the original chip.

I. INTRODUCTION

Augmented Reality (AR) and Virtual Reality (VR) devices are emerging to be the next mobile computing platform. To meet the stringent performance, power and form factor requirements for AR/VR consumer devices, image sensors must be optimized for computer vision algorithms, which require global shutter (GS) operation, high sensitivity, high dynamic range (HDR), and ultra-low power consumption [1].

We have reported a GS digital pixel sensor (DPS) fabricated by a stacked process with pixel-level Cu-to-Cu hybrid-bonding (HB) interconnects between the two stacked layers [2, 3]. The sensor had a 512 × 512 pixel array with 4.6 µm DPS pixel and featured an overlapped triple quantization (3Q) scheme that performs a time-to-saturation quantization and the dual conversion gain (CG) linear ADC modes sequentially in the same frame to extend DR with a 10-bit ADC. It achieved an ultra HDR of 127 dB and low power consumption of 5.8 mW at 30 frames per second, which demonstrated the best figure of merit (FOM) among recently emerged 3D-stacked DPSs [4]-[8].

In this article, we report design and evaluation results of an improved version of the previously reported DPS. We made further circuit and process optimizations and achieved better performance than the original chip for productization. The new chip integrates on-chip voltage regulators into the 4mm × 4mm die, maintaining the same footprint as the original chip. These evolutions have made the DPS chip most suitable for battery-powered and always-on mobile computer vision applications.

II. SENSOR DESIGN AND OPERATION

Fig. 1 shows a circuit diagram and a cross-section of the stacked DPS pixel. The pixel is partitioned into two parts; a dual-CG type pixel with a backside-illuminated (BSI) pinned photodiode (PPD) in the CIS layer on the top, and an in-pixel ADC circuit with 10-bit SRAM in the ADC layer at the bottom. These two layers are connected using HB technology [9, 10] in each pixel. In Fig. 2, a detailed circuit diagram of the stacked DPS pixel illustrates the in-pixel ADC circuit and 10-bit SRAM with the logic circuit in-between them to enable the 3Q quantization scheme described hereafter.

The DPS features an overlapped 3Q scheme that performs time-to-saturation (TTS mode) quantization for high-light signal, high-CG linear ADC (so-called PD-ADC mode) for low-light signal, and low-CG linear ADC (so-called FD-ADC mode) for middle-light signal sequentially in one frame [1, 2]. The in-pixel ADC circuit automatically selects the appropriate quantization mode based on the received light of each pixel and stores the quantized value in the pixel memory. Pixel-signal timing of overlapped 3Q scheme is illustrated in Fig. 3. A typical photo-response curve of the overlapped 3Q DPS is illustrated in Fig. 4.

In the new sensor design, we made further

optimization of device sizes in the pixel and modified metal-wire layout throughout the pixel array. These changes reduce temporal noise (TN) and fixed pattern noise (FPN) by lowering and balancing the coupling capacitance between sensitive nodes.

The chip block diagram in Fig. 5 shows circuit components on the CIS and ADC layers with their HB connections. The new sensor chip integrates charge pumps to generate a higher voltage than the analog supply (2.5V) and a negative voltage lower than the ground. The charge-pump outputs and the primary voltage supplies drive on-chip low-drop-out (LDO) regulators that supply the pixel-array in the ADC layer and the pixel-signal drivers in the ADC and CIS layers. Despite the additional components for internal voltage regulation, the new chip was laid out on the same die size as the original chip (4mm × 4mm). Fig. 6 is a photomicrograph of the stacked chip in a chip-scale package (CSP).

III. CHARACTERIZATION RESULTS

Fig. 7 shows the pixel-signal histogram at the dark condition for the original and new chips. The signal distribution of the new chip is narrower than the original chip. This improvement is due to the reduced pixel-wise FPN resulting from the metal-wire layout optimization in the pixel array for coupling-capacitance reduction and balancing. SNR drop at the junction point of the high CG and low CG ADC modes is improved by tuning the DCG capacitor [11], while maintaining the 127-dB DR.

In Fig. 8, power consumption of the original and new chips is compared with different integration times (Tint). Although the on-chip voltage regulators are integrated in the new chip, its power is almost the same as that of the original chip in the 1-ms Tint case. In the longer Tint cases, the new chip consumes less power than the original chip. The lower power consumption of the new chip is due to circuit-design optimizations of the peripheral analog modules and improved PLL control which reduces the PHY power consumption.

Fig. 9 shows an image captured by the 3Q scheme.

Table 1 compares the sensor performance index for recent stacked pixel- or cluster-wise ADC sensors. In comparison with the original chip in the previous work, the new chip has smaller noise floor (TN) and FPN as expected by the pixel-design improvement discussed in this article. As a result, the new chip has better FOM than the original chip, which has superior FOM than the other references in the table.

IV. SUMMARY

We have developed the second-generation chip of a stacked digital pixel sensor with an overlapped triple quantization scheme. It integrates voltage regulators for pixel power supply and pixel-control signal drivers in the same die size as the original chip. The new chip has improved temporal noise and fixed pattern noise performance achieved by pixel-design tuning and layout optimization. The sensor realizes the best FOM among the recent stacked pixel- or cluster-wise ADC sensors.

ACKNOWLEGMENT

The authors are deeply indebted to the outstanding group of researchers and engineers, as well as technology visionaries across Meta, Brillnics, and TSMC.

REFERENCES

[1] C. Liu, et al., “Intelligent Vision Systems – Bringing Human-Machine Interface to AR/VR”, in *IEDM Tech. Dig.,* San Francisco, CA, USA, pp.218-221, 2019.

[2] C. Liu et al., “A 4.6 μm, 512×512, ultra-low power stacked digital pixel sensor with triple quantization and 127 dB dynamic range,” in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2020, pp. 327–330.

[3] R. Ikeno et al., “A 4.6-μm, 127-dB Dynamic Range, Ultra-Low Power Stacked Digital Pixel Sensor With Overlapped Triple Quantization,” *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2943-2950, Jun. 2022.

[4] K. Mori et al., “A 4.0 μm Stacked Digital Pixel Sensor Operating in a Dual Quantization Mode for High Dynamic Range,” *IEEE Trans. Electron Devices*, vol. 65, no. 69, pp. 2957-2964, Jun. 2022.

[5] M. W. Seo et al., “A 2.6 e-rms low-random-noise, 116.2 mW low-power 2-Mp global shutter CMOS image sensor with pixel-level ADC and in-pixel memory,” in *Proc. Symposium. VLSI Tech.*, Jun. 2021, pp. 1–2.

[6] M. Sakakibara et al., “A 6.9-μm pixel-pitch back-illuminated global shutter CMOS image sensor with pixel-parallel 14-bit subthreshold ADC,” *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3017–3025, Nov. 2018.

[7] T. Takahashi et al., “A stacked CMOS image sensor with array-parallel ADC architecture,” *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1061–1070, Apr. 2018.

[8] H. Sugo et al., “A dead-time free global shutter CMOS image sensor with in-pixel LOFIC and ADC using pixel-wise connections,”

in *Proc. Symp. VLSI Circuits*, Jun. 2016, pp. 1–2.
[9] C.-T. Ko, et al., "Wafer-level bonding/stacking technology for 3D integration," *Microelectron. Rel.*, vol. 50, no. 4, pp. 481–488, Apr. 2010.
[10] P. Ramm, et al., *Handbook of Wafer Bonding*. Hoboken, NJ, USA: Wiley, 2012.
[11] N. Akahane, et al., "Optimum Design of Conversion Gain and Full Well Capacity in CMOS Image Sensor With Lateral Overflow Integration Capacitor," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2429-2435, Nov.. 2009.

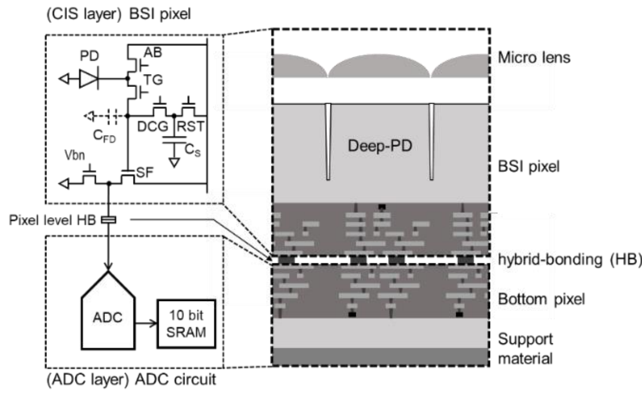

Fig. 1. Circuit/Block diagram and cross sectional view of the stacked digital pixel sensor.

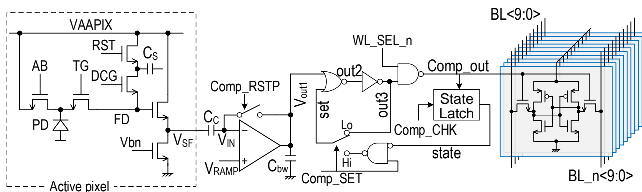

Fig. 2. Detailed circuit digram of the stacked DPS pixel.

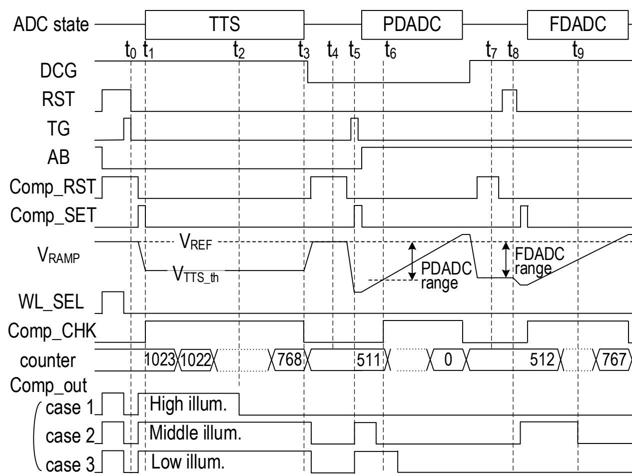

Fig. 3. Timing diagram of overlapped 3Q operation.

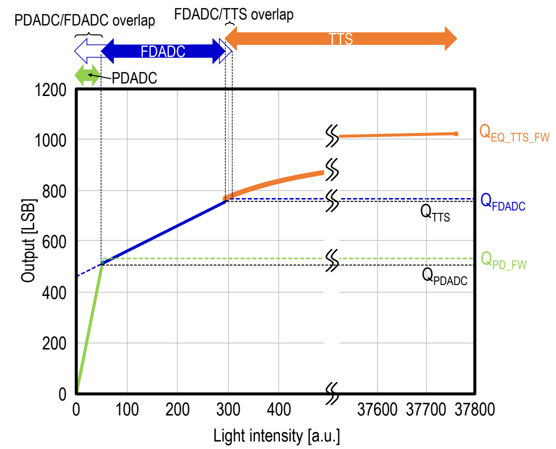

Fig. 4. Photo-response curve of the overlapped 3Q DPS.

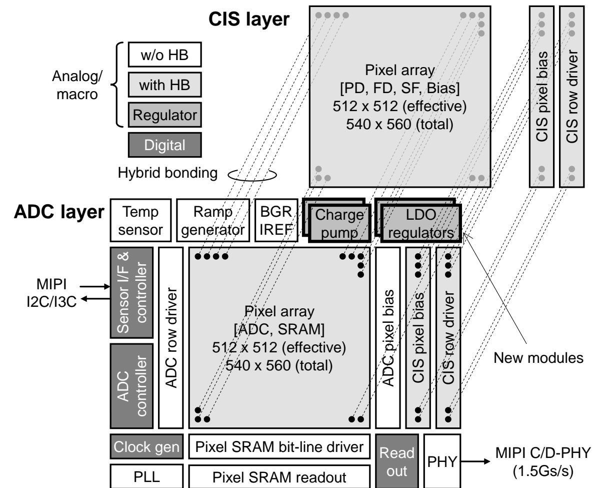

Fig. 5. Sensor chip block diagram.

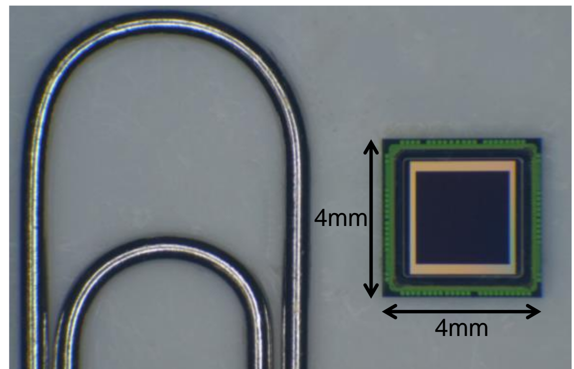

Fig. 6. Sensor chip photomicrograph with a paper clip.

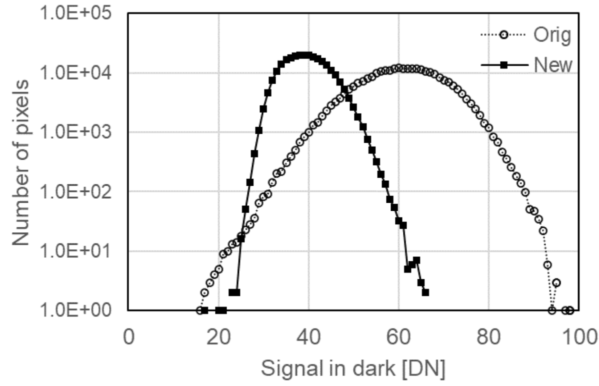

Fig. 7. Dark histogram showing the FPN improvement in the new chip in this work.

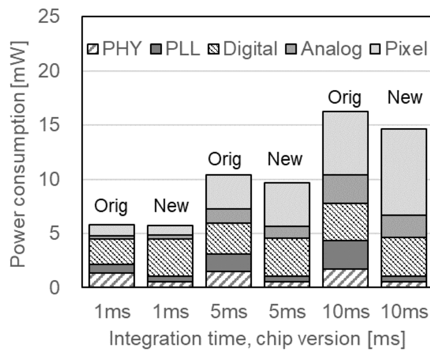

Fig. 8. Power consumption of the original and new chips. at different integration times

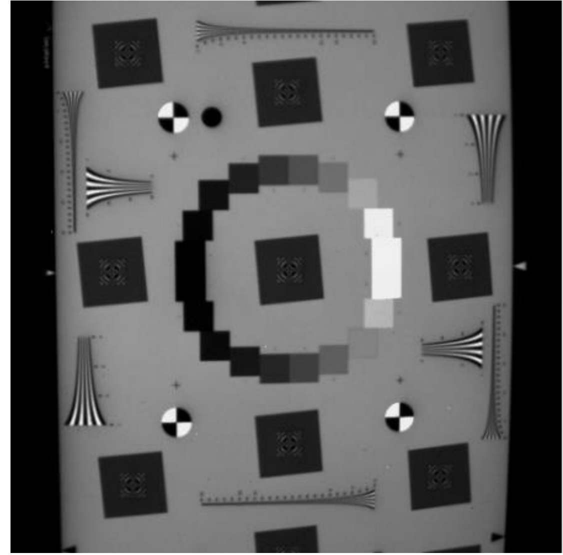

Fig 9. A test chart image captured using 3Q scheme.

Table. 1 Sensor performance matrix for recent stacked pixel wise ADC system.

Specification	This work	Previous work [2,3]	VLSI2021 [5]	ISSCC 2018 [6]	JSSC2018 [7]	VLSI2016 [8]
Process technology	45nm/65nm	45nm/65nm	65nm/28nm	90nm/65nm	90nm/55nm	45nm/65nm
Pixel size [µm]	4.6	4.6	4.95	6.9	4.8	1.65
# of pixels (H×V)	$512^{H}\times512^{V}$	$512^{H}\times512^{V}$	$1668^{H}\times1364^{V}$	$1632^{H}\times896^{V}$	$2360^{H}\times1728^{V}$	$2576^{H}\times1920^{V}$
In-pixel memory bit #	10b (1 pixel/ADC)	10b (1 pixel/ADC)	22b (1 pixel/ADC)	14b (1 pixel/ADC)	12b (160 pixels/ADC)	12b (16 pixels/ADC)
QE (@530nm) max [%]	96 (Mono)	96 (Mono)	NA	NA	N/A	NA
Dynamic range [dB]	127	127	74[(1)]	70.2	69	NA
Conversion gain [µV/e-]	170/12	170/7	132	NA	65	NA
Linear full well [ke-]	5/34/9000[(2)]	3.8/51/9000[(2)]	14	16.6	6.8	220
Noise floor [e-]	4.0	4.2	2.6 (24dB gain)	5.15	2.4 (24dB gain)	NA
Dark FPN [e-]	27	47	1.94/0.45	NA	N/A	NA
Power [mW]	5.8	5.8	497.8	746	1340	NA
FOM[(3)]	0.0608[(4)] 0.0013[(5)]	0.1809[(4)] 0.0014[(5)]	1.74 (24dB gain)	1.24	15.84 (24dB gain)	NA

(Notes) (1) Estimation / (2) Equivalent FWC estimated with photo response plot

(3) Figure of Merit (FOM) is based on the following formula [5]; $\mathrm{FOM} = \frac{(\text{power})\times(\text{noise})}{(\text{\# of pixels})\times(\text{frame rate})\times(\text{DRU})}$, $\mathrm{DRU} = \frac{(\text{saturation})/(\text{gain})}{(\text{noise})}$

(4) Without FPN correction / (5) With FPN correction