Trends and Developments in State-of-the-Art CMOS Image Sensors

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***Abstract*— The state-of-the-art in CMOS image sensors (CIS) is constantly evolving. Backside, stacked imagers are now well established and global shutter and dynamic range are priorities. The industry continues to reduce pixel pitch and increase array resolution. A snapshot of the current pitch (now entering the sub-0.6 μm generation) and resolution is provided. Elements of the signal path required for high quality images are described along the transduction path, beginning with Phase Detection Autofocus (PDAF) pixels and Color Filter Arrays (CFA). The aperture grid and trench technologies required for effective isolation are reviewed followed by the critical pixel transistors; the transfer FET and the Source Follower. The analog signal is moved off-chip using Direct Bond Interface (DBI) and Through Silicon Vias (TSV) to the underlying Image Signal Processor (ISP) where digitization and signal processing is performed; trends in these topics are discussed.**

I. Introduction

Originally developed to exploit the economics of mass production CMOS processes, CMOS image sensors (CIS) are now highly specialized devices with process steps customized for optical detection. In an interesting reversal the technology being developed for a sensor is being applied to high volume CMOS; for example, Direct (Hybrid) Bonding Interface (DBI), driven by stacked CIS devices is widely used in processor design. Phase Detection Autofocus (PDAF) and Color Filter Arrays (CFA) augment camera performance. Pixel pitches are now below 0.6 μm (Samsung and OmniVision) and need optical grid apertures and deep trench isolation. Trends in these elements and the subsequent transfer FET and Source-Follower are reviewed, followed by pitch reduction in the DBI and the often-overlooked Image Signal Processor (ISP). The ISP performs an increasingly important role in analog-to-digital conversion and front-end processing.

Driven by mobile devices, CIS sensors are rapidly developing customized technologies for other applications. A brief review of automotive (high dynamic range) and security sensors (infra-red) is provided.

II. Pixel Pitch in Mobile Devices

Pixel scaling continues to trend down, with Samsung, Sony and OmniVision leading the push to smaller pitches. Consulting Fig. 1, showing the pixel pitch with time, the 0.6 μm generation entered the marketplace in 2021.

Samsung presented a 0.64 μm device with its JN1 sensor and OmniVision followed suit with the 0.61 μm OV60A. The first 0.56 μm sensor was identified in 2022; the Samsung 0.56 μm HPX [1] and OmniVision has announced a sensor at the same pitch, the OVB0A,to bereleased in 2023. Sony reduces pitch conservatively, announcing a 0.7 μm design in 2021 (IEDM 2021) analyzed in early 2023; the IMX758. Sensor resolution also trends to larger values and Fig. 2 shows the sensor resolution versus the pixel pitch for rear facing cameras.

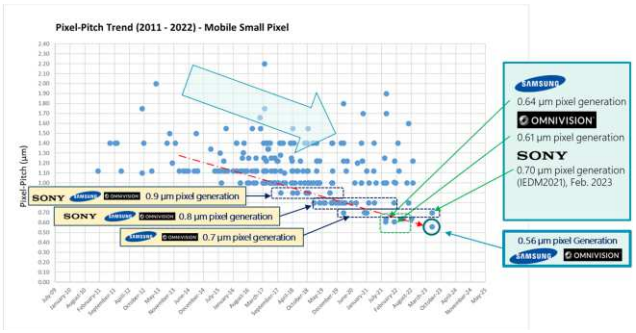

Fig. 1. Pixel pitch vs year of analysis, years 2021- March 2023.

Sensor resolution has been pushed by Samsung and OmniVision with 50 MP arrays followed by 64 MP, 108 MP and now 200 MP. Broadly speaking there are two strategies at play; high resolution/small pixel pitch devices and lower resolution devices with larger pixels. These two approaches maintain signal dynamic range and noise performance in different ways; the smaller pitches often use several pixels in parallel to collect low signal levels that are averaged or binned. The larger pixels use a high-quality analog signal path to resolve low light signal quality. In particular, Apple iPhones use a large pixel, lower resolution strategy with 12 MP sensors, only recently moving to 48 MP in the iPhone 14 generation.

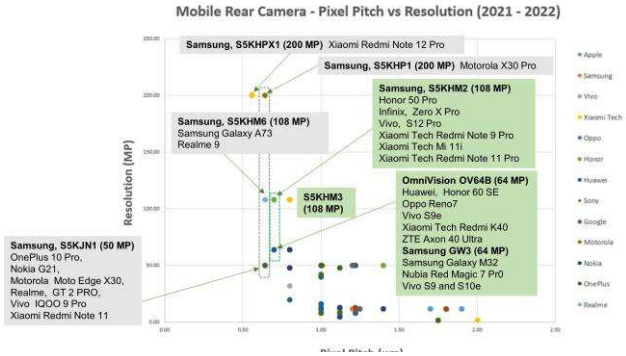

Fig. 2. Array resolution vs Pixel Pitch for back facing cameras.

III. Phase Detection Autofocus and Color Filter Arrays

The pixel pitch has direct implications for both Phase Detection Auto Focus (PDAF) and the Color Filter Arrays (CFA). There are three basic strategies for PDAF; masked, dual-photodiode, and On Chip Lens (OCL). Manufacturers continue to use these approaches and occasionally combine them. Rapid focusing using different regions of the field requires PDAF pixels covering as much of the array as possible while not compromising the light collecting efficiency. This is a particular problem for masked PDAF where half the PDAF pixel is covered with metal. Fig. 3 shows

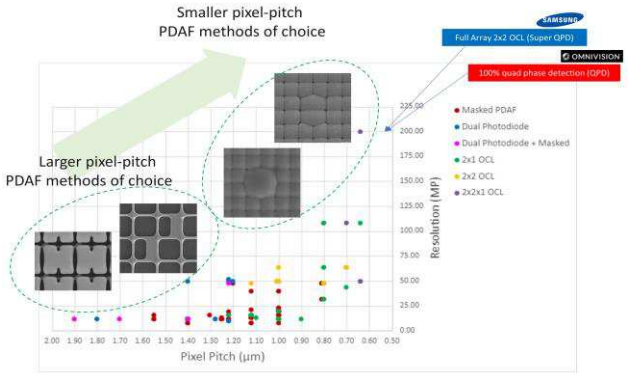

Fig. 3. PDAF pixels use On Chip Lenses as pixel pitch is reduced.

the PDAF strategy trending towards On Chip Lenses (OCL) as the pitch is reduced and the resolution increases.

Fig. 4 shows the trend in Color Filter Array Mosaics. As the pixel pitch decreases, the CFA pitch remains at approximately 2.4 µm. Current pixel pitches use 4 by 4

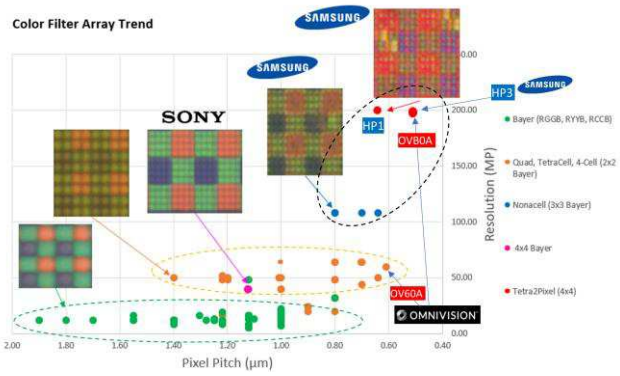

Fig. 4. Color Filter Arrays are grouped as pixel pitch decreases.

groupings of color filters, and the aperture grid is placed between each pixel using a buried color filter between the aperture metal.

IV. Deep Trench and Aperture Grid Isolation

Trench Isolation and Aperture Grids both serve the objective of pixel isolation. The aperture grid above the

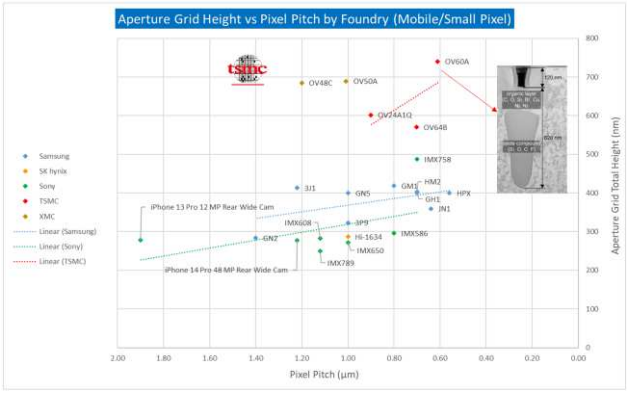

Fig. 5. Aperture grid height vs pixel pitch.

photodiode surface does this by ensuring light enters only the target photodiode under the aperture. The grid increases in height and complexity with smaller pitches, shown in Fig. 5.

The grid increases quantum efficiency by reflecting high angle light back into the photodiode. The grid should be optically reflective to do this and also be electrically conductive to discharge optically generated residual electrons. Manufacturers have been shifting to composite grid structures as the pixel pitch is reduced and the height is now comparable to or exceeds the pixel pitch.

The trench between the photodiodes isolates each diode electrically and optically. As well, trench backfill material selection increases well capacity and reduces dark current noise. Samsung typically uses Front Trench Isolation for mobile pixels, while Sony and OmniVision (TSMC) use Back Deep Trench Isolation. Fig. 6 shows trench depth versus

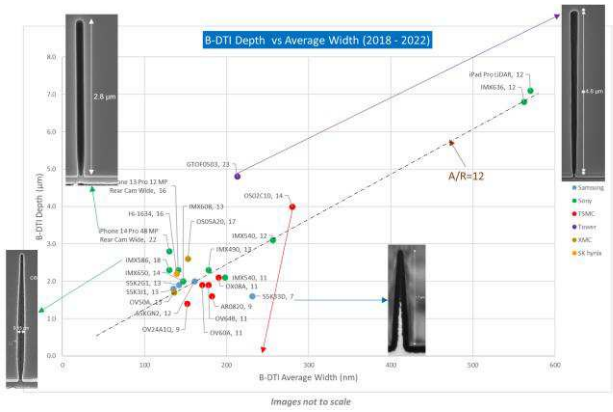

Fig. 6. Back Deep Trench Depth vs Average Width.

average trench width for different applications and foundries. Each data point is labelled by the device and aspect ratio of depth to width; most devices have and aspect ratio of approximately 12.

Table 1 summarizes the representative layer trench material for recent small pixel sensors, typically a composite structure of high K oxides.

TABLE I. Deep Trench Isolation Liner Materials.

Foundry/ Device	XMC/ OV50 A	TSMC/ OV60 A	Sony/ iPhone 14	Hynix/ Hi-1634	Samsung/ JN1
DTI	B-DTI	B-DTI	B-DTI	B-DTI	F-DTI
Pixel Pitch (µm)	1.00	0.64	1.22	1.00	0.64
DTI Depth (µm)	1.7	1.9	2.8	2.2	3.8
Liner	AlOSi-TaoSi-SiO	AlO-HfO-TaO-SiO	AlO-TaO-SiO	AlO-Hf-SiO	N+ poly/Liner

V. Transfer FET and Source Follower

Once the photodiode has converted the input light to electric charge, the electric signal is transferred off the array with minimal noise. The two critical devices in this signal chain are the transfer gate and the sourcefollower. The transfer gate should shift all photodiode charge to a storage

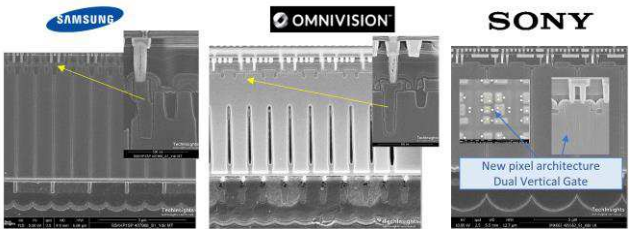

Fig. 7. Vertical Transfer Gates by Samsung, OmniVision and Sony.

node and at small pitches the preferred approach is a Vertical Transfer Gate. Fig. 7 shows the vertical transfer gates in recent small pixel pitch sensors. The Sony device (STARVIS-2 Security and Surveillance device, the IMX 662) uses a dual Vertical Transfer Gate to improve charge transfer. Samsung's most recent 200 MP sensor, the HP2 found in the Galaxy S23 Ultra, also uses a Dual Vertical Gate [2].

The source-follower drives the output column and a large transconductance (W/L) is desirable. As well, the transistor area has a direct impact on temporal noise, random telegraph noise, fixed pattern noise and pixel linearity. Increasing the area (WxL) can decrease these effects but also reduces the effective gain of the pixel. Several strategies are available to designers to optimize performance; thin silicon nitrides are

Fig. 8. Source-Follower Width to Length Ratio vs Pixel Pitch.

increasingly common, and photodiodes are grouped and output through the same SourceFollower device. Transistors are often placed in parallel to increase transconductance and reduce noise. Fig. 8 shows the gate width to length ratio, which is maintained as pixel pitch is reduced to conserve the drive capacity.

VI. Direct Bonding Interface and the Image Signal Processor

Almost all mobile image sensors are now stacked with an Image Signal Processor (ISP), and the underlying ISP has served a mechanical function to support the thinned CIS. The ISP provides control signals to the array and receives analog outputs that are digitized; this is done through either a Direct (Hybrid) Bonding Interface (DBI) or Through Silicon Vias (TSV) for backside imagers. DBI pitch is decreasing with an objective to create pixel pitch hybrid bonds; this would allow pixel circuitry to be moved to the ISP. Currently, pixel hybrid bond pitches have been seen only in larger pixels; three Sony devices (iPad Pro 10 µm pitch LiDAR, the IMX990 SWIR sensor, and the IMX636 event-based sensor analyzed in 2022)

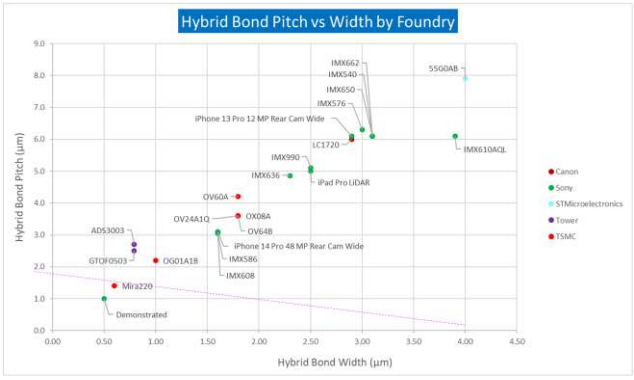

Fig. 9. Decreasing direct bond pitch vs width.

and the current smallest in-pixel device, the OmniVision voltage domain global shutter (OG01A1B) with 2.2 um pitch. Fig. 9 shows the decreasing bonding pitch led by specialized sensors (Near Infra-Red, Time of Flight), the current smallest pitch seen is in the ams OSRAM Mira220 global shutter Near Infra-Red sensor. Sony has demonstrated a 1.0 µm DBI.

The ISP die controls the CIS array, converts the array output from analog to digital and performs front end digital

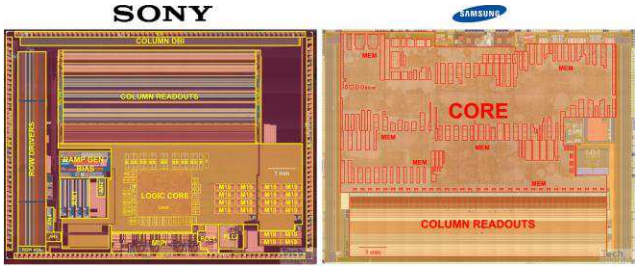

Fig. 10. Image Signal Processor floorplan, iPhone 14 (standard cell logic only in the "Logic Core" box) and Galaxy S23 (light brown regions of logic core are unused).

processing. Fig. 10 shows the ISP for two major main (wide) smartphone cameras; the iPhone 14 Pro Max and the Samsung S23 Ultra. Note two features; the large area required to perform analog to digital conversion of the columns (approximately 35%) and also the sparse circuit density in the standard cell logic area . The latter suggests much more digital processing can be added in the future.

VII. Automotive, Security

Until recently, automotive image sensors were off-the-shelf designs repurposed as automotive imagers but the major manufacturers are now custom designing sensors for this market. Specific requirements include flicker mitigation and

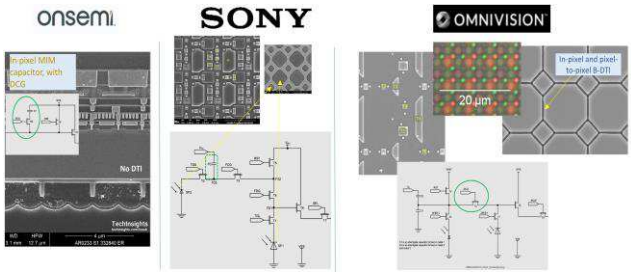

Fig. 11. High dynamic range pixel structures; onsemi, Sony, OmniVision.

high dynamic range. Gains of 120-140 dB are common, and several techniques are used including multiple exposure times and, as shown in Fig. 11 dual gain pixels (onsemi) and dual photodiode sizes (Sony and OmniVision).

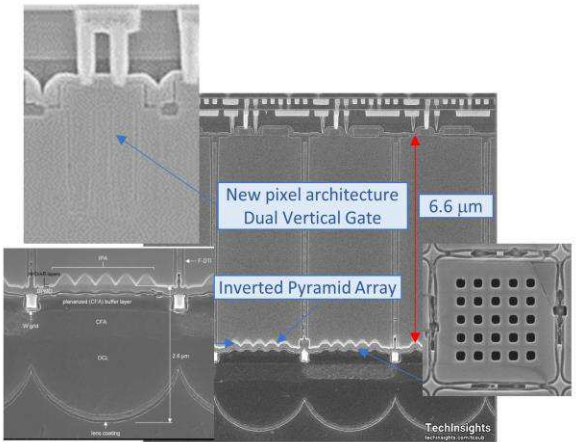

Fig. 12. Sony IMX662 STARVIS 2 Near Infra-Red Sensor

Security devices need high performance in the infra-red. The Sony STARVIS 2 IMX662 (Fig. 12) uses techniques common to other manufacturers including Inverted Pyramid Arrays [3] at the silicon surface, a 6.6 µm thick epi layer and Front trench isolation as well as a new dual vertical gate pixel architecture.

ACKNOWLEDGMENTS

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High Full Well Capacity and Low Noise Characteristics in 0.6 μm Pixels via Buried Sublocal Connections in a 2-Layer Transistor Pixel Stacked CMOS Image Sensor

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Abstract

Herein, we demonstrate the development of a 2-Layer Transistor Pixel stacked CMOS image sensor (CIS) that possesses a high full-well capacity (FWC) and low random noise (RN). A high FWC was achieved by increasing the photodiode (PD) volume by fabricating PDs and pixel transistors on different silicon (Si) layers in a 3D sequential integration process and introducing a single vertical gate (SVG). Buried sublocal connections (BSCs) that connect multiple floating diffusions (FD) and Pixel FinFETs were introduced to improve the conversion gain and random noise (RN). We have demonstrated a 2-Layer Pixel with a 0.6 μm pixel with an RN of 0.99, an FWC of 8000e-, and a dynamic-range of 78.1 dB.

Ⅰ. Introduction

Ensuring high dynamic range (D-range) for pixel shrinkage is important for image capture. Pixel shrinkage makes it difficult to ensure a high FWC owing to the inability to secure PD area and low noise because of the size reduction of the pixel transistors. A two-layer transistor pixel stacked CMOS image sensor (“2-Layer Pixel”) has been proposed as a promising technology for capturing images with low noise and high D-range and achieving Pixel shrinkage in CMOS image sensors. [1-2] Schematic diagrams of the 2-Layer Pixel are shown in Figs. 1 and 2.

The 2-Layer Pixel comprises an Si layer on which the PDs and transfer gates are arranged. the second layer contains t pixel transistors, such as amplifier transistors, select gates, reset gates, and deep contacts, to connect the PDs and pixel transistors. Additionally, full trench isolations (FTIs) are formed to separate the pixels. In a previous study, we developed a three-dimensional (3D) sequential integration process to realize the 2-Layer Pixel. [2]

This paper presents a 2-Layer Pixel with a 0.6 μm Pixel by introducing a single vertical transfer gate (SVG), buried sublocal connections (BSCs), and Pixel FinFETs.

Ⅱ. Improvement of FWC

The major performance requirements for PDs and transfer gate (TRG) are high FWC with no-lag and no-blooming. In this device, the PDs were completely separated by introducing full trench isolation (FTI) in the 1st Si Layer that formed the PDs, resulting in a structure with no-blooming. TRG optimization is performed only for no-lag and FWC, and the degree of freedom of the TRG design are improved compared with the case where FTI is not applied. The 2-Layer Pixel structure enlarges the TRG layout area as shown in Fig. 3(a-b). The introduction of SVG expands the area available for TRG placement because it causes a change in the PD configuration which eliminates the need for a shallow PD to achieve a high FWC and no-lag, as shown in Fig. 3(b-c). An FWC of 8000e- was achieved with the SVG by optimizing its geometry and placement.

Ⅲ. Improvement of RN

Reducing the FD capacitance is important for improving RN and conversion gain. BSCs were introduced to reduce the diffusion layer capacitance, and Pixel FinFETs was introduced to shrink the FD sharing unit.

In the conventional 2-Layer-Pixels, SCs are used to connect multiple floating diffusions. SCs are structures formed between 1st-Layer and 2nd-Layer, which contacts to the Si surface of the 1st layer and have ohmic conductivity. The BSCs are structures in which the contact area changes from the Si surface to the Si sidewall, as shown in Fig. 4(b). Compared with SCs, BSCs can be separated from TGs and the capacitance of TGs can be lowered. By optimizing the layout and depth of the BSCs, the FD capacitance was reduced by 46%, as shown in Fig. 5(a). The BSCs exhibited Ohmic conductivity, and the resistance is plotted in Fig. 5(b). To shrink the FD-sharing unit from 2x4 to 2x2, we adopted Pixel-FinFETs. Introducing BSCs and changing the FD sharing unit increased the conversion gain by 2.26 times and decreased the RN by 67%, as shown in Fig. 6(a)and(b).

V. Conclusions

We fabricated a 2-Layer Pixel with 0.6 μm Pixel, as shown in Fig. 7. Figure 8 shows the relationship between the pixel size and D-range, wherein the FWC and RN of PD CISs reported in previous studies [3-7] are compared with those obtained in this study. The performance parameters and comparison with prior studies are summarized in Table I.

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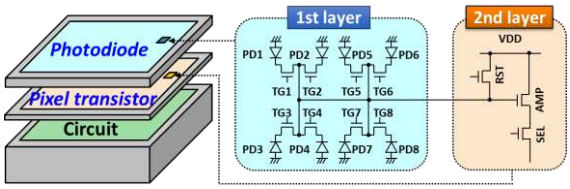

Fig. 1 Schematics of the 2-Layer Pixel based on a three-dimensional sequential integration process [1]

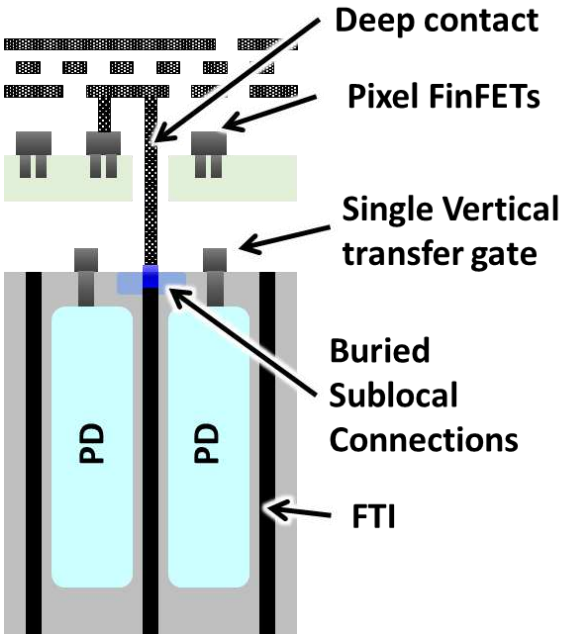

Fig. 2 Cross-sectional structure of the photodiode (PD) and pixel transistor.

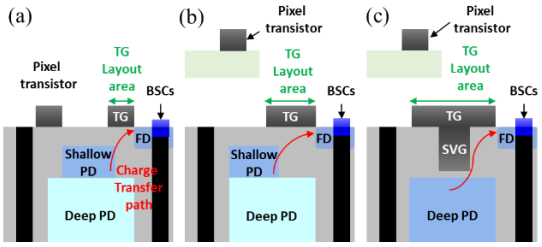

Fig. 3(a—c) Schematics of enlargement TG layout area by 2-Layer Pixel structure and the introduction of SVG

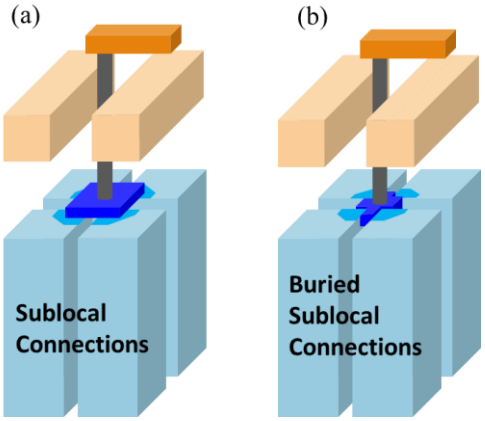

Fig. 4 Design optimization based on sublocal connections to connect multiple floating diffusions (FDs). (a, b) Schematics of device structures (a) with the sublocal connections [2] and (b) with the buried sublocal connections.

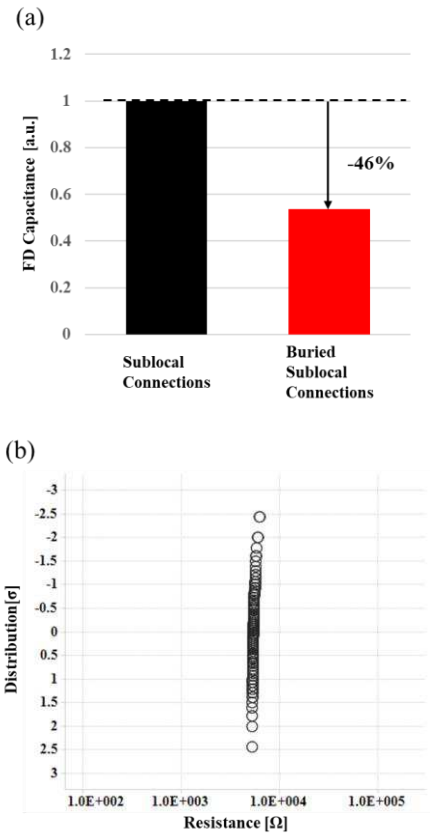

Fig. 5 (a) Comparison of FD Capacitance between the 2-Layer Pixels with the buried sublocal connections and the sublocal connections. (b) Resistance of the buried

sublocal connections.

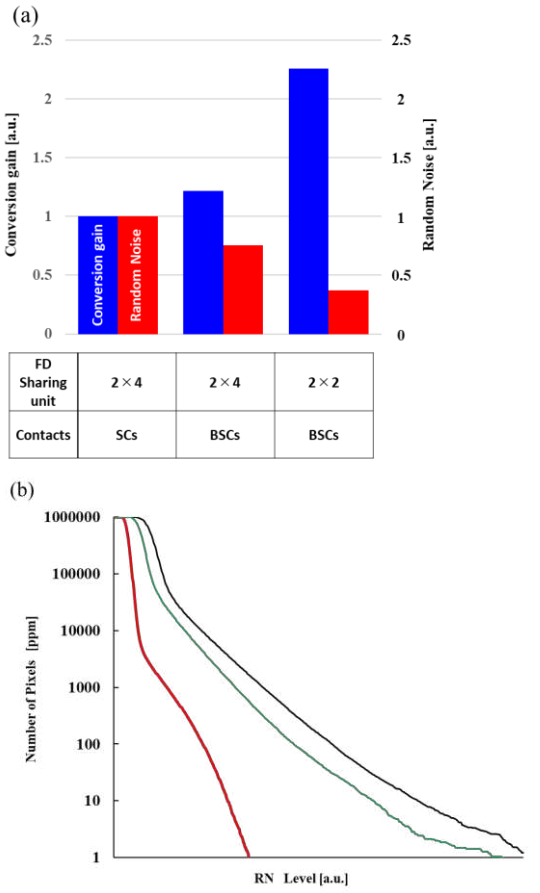

Fig. 5 (a) Comparison of conversion gain and random noise between FD sharing units and contacts. (b) Comparison of RN histogram between FD Sharing units and contacts.

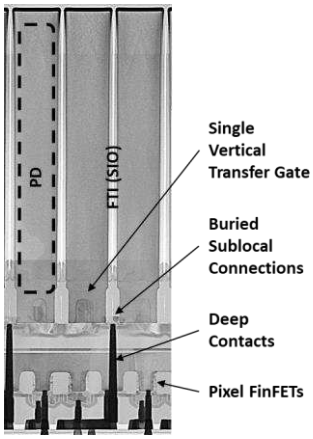

Fig. 6 Cross-sectional image of the 2-Layer Pixel with 0.6 µm PDs

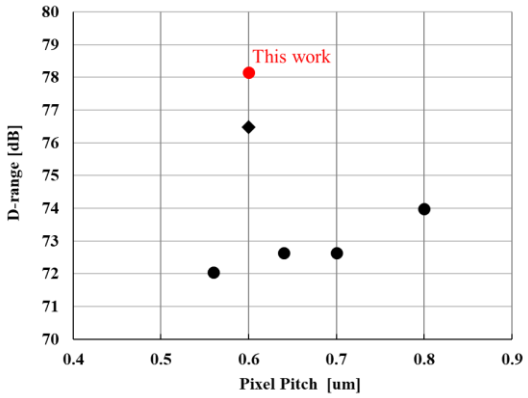

Fig. 7 Relationships between the pixel size and D-range in this work compared with those in previous studies. [3-7] D-range=20*log10(FWC/RN)

Table. 1 Performance comparison table

	unit	This work	Ref[7]	Ref[6]
Pixel Pitch	µm	0.6	0.6	0.56
Transfer Gate	-	Single VTG	Dual VTG	Single VTG
FD unit	-	2×2	-	-
FWC	e-	8000	10000	6000
RN	e-	0.99	1.5	1.5
D-range	dB	78.1	76.5	72.1
lag	e-	<1	-	-
RTS@10ppm	erms	<6	-	-

World smallest 200Mp CMOS Image Sensor with 0.56µm pixel equipped with novel Deep Trench Isolation structure for better sensitivity and higher CG

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***Abstract*—** We present the world smallest 200 megapixel (MP) CMOS Image Sensor equipped with newly developed 0.56µm pixel. Apart from the conventional full-depth deep trench isolation (FDTI), our 2x4 shared pixel structure incorporated novel DTI structure to minimize the light absorption from polysilicon which is used to fill DTI and suppress dark current when biased. With new DTI structure, the relative QE is improved by 14%. Furthermore we were able to control the potential barrier between 4 pixels that share new DTI structure to improve the image quality in summation mode. The new structure also increased conversion gain (CG) by 38% and further process optimization resulted in additional 14%improvement.

I. INTRODUCTION

Over the past decade, we have witnessed tremendous development in CMOS image sensor (CIS) technology for better image quality. For CIS for mobile phones, in particular, we are able to see two major directions for development of pixels.

One of the major direction was developing smaller submicron pixels with the aim of achieving higher resolution by capturing more details of the object [1-2]. With the help of new technologies such as full-depth deep trench isolation (FDTI) and vertical transfer gate (VTG), the pixel pitch has shrunk continuously from over 1.0 um up to 0.56µm in just few years [3-8] and the resolution has reached up to 200MP [7]. This trend has garnered a favorable response from the CIS market and most of the flagship mobile phones are now equipped with CIS with 50MP~200Mp. However it is very difficult to avoid the physical limit of smaller size of pixels in very low light conditions and the image quality deteriorates as soon as the light gets too dim. A simple solution is to combining the signals from several neighboring pixels together. This leads to the development of prevalent 2x2 color filter (CF) patterns and underlying pixel circuitry as well as various image signal processing algorithms. Recently we observed 4x4 CF patterns where 16 pixels are merged.

Another direction of major CIS development is the auto-focus (AF) technology. Since the emergence of phase detection AF, fast AF system became the indispensable feature even in mobile phones. The accuracy and speed of AF heavily rely on the density of the PDAF pixels. Therefore two types of major technologies, which are dual PD (2PD) [9-10] and Quad cell (i.e. Qcell) [11, 7], have been developed to utilize all the pixel as AF pixel. While each technology has its own pros and cons, both of them offer essentially 100% AF pixels and are able to bring a superior AF user experience.

In this paper, we introduce a new CIS in order to meet the all aspects of the previous demands. The pixel based on a recently developed 0.56um pixel employed a unique DTI structure which enables us to maintain the superior AF performance and minimize the QE loss simultaneously. The physical structure also enables us to keep the photo electrons from overflowing to FD and maintain the linearity at binning mode. In addition, the structure helped us to increase the conversion gain (CG) of the system to reduce the readout noise to achieve high image quality.

II. PIXEL TECHNOLOGY

Our sensor, a world smallest 200MP CIS, is built with a recently developed 0.56um pixel with 2x4 shared structure where we employed 32nm BEOL process for pixels. Due to the world smallest 0.56um pixel, we are able to shrink the chip size by 22% compared to the previous generation of 200MP CIS with 0.64um pixel from our company. The resolution is 16320 x 12288 with optical format of 1/1.4”.

0.56um pixel presented in ref. [8] with conventional technology, however, contains several limitations. While a conventional FDTI structure offers great performances such as higher FWC and low optical crosstalk, it is not suitable for Qcell technology. As shown in Fig. [1] and Fig. [2], Qcell with FDTI structure has single microlens over 4 pixels and an incident light focuses on the intersection of FDTI filled with polysilicon which is chosen to reduce dark current from the wall of FDTI. Therefore it is difficult to avoid the quantum efficiency (QE) loss from photon absorption by polysilicon. Another disadvantage of having FDTI structure for Qcell is that the physical separation of FDTI prevents from excess electrons to migrate between microlens-shared pixels before overflowing to FD as in dual PD pixels. This results in the output non-linearity of charge summation of binning mode. Finally, it is not convenient to extract a high conversion gain in conventional FDTI structure since the FD junctions are isolated from each other. Typically one needs complicated metal layout with longer metal lines and a number of contacts as well as increased junction capacitance which result in lower conversion gain.

Therefore we devised new FDTI structure with DTI center cut (DCC) in order to overcome the challenges we mentioned above as shown in Fig. [3]. As soon as we remove the DTI from the center of 4 pixels and connect them from each other, we are able to tackle several problems simultaneously.

Fig. [4] shows that the TCAD simulation of optical intensity between conventional No-DCC structure and DCC structure. We can see that DCC structure not only prevents optical loss at the center of 4 pixels but also scattering from DTI is reduced. Still the optical cross talk cannot be avoided. In Fig. [5], the schematic diagram of inter-pixel overflow (IPO) structure is presented. By controlling the size of DCC and n-type doping concentration for photodiode carefully, we are able to control IPO potential. Fig. [6] shows the TCAD simulation of potential profile of photodiode and IPO potential. We can see that IPO arises in the deep photodiode region. In addition we designed the location of floating diffusion (FD) to be at the center of DCC. Fig. [7] shows the schematics of pixel layout between No-DCC structure and DCC structure. By merging FD, we are able to reduce the number of FD junctions and contacts on FD by a quarter with shorter FD metal connection. Since FD is located at the center of DCC, the doping and potential profiles should be managed carefully to prevent second IPO path due to FD implantation while enhancing the charge transfer to FD.

III. Results and Discussion

First, we can improve QE significantly over Qcell with conventional DTI structure by minimizing optical loss from polysilicon where light is most focused. Fig. [8] shows the comparison of normailzed QE spectrum between No-DCC and DCC structure. We are able to observe increase of QE by 14% from DCC structure. In Fig. [9] the change of sensitivity relative to DCC size shows 0.6% per 10nm. Because of the DTI removal, optical crosstalk is expected to increase slightly between pixels under the same microlens as we can see from TCAD simulation. However, these pixels share the same color filter, therefore, the crosstalk does not impact the performance when operated in binning mode where signals are summed for low light conditions. In high resolution scenes where each pixels are operated separately, the major cause of signal difference between these pixels are from the misalignment of microlens rather than the crosstalk between pixels and is compensated by proper ISP algorithm.

Second, the IPO level change according to DCC size is shown in Fig. [10]. As one can imagine, IPO level is sensitive to the change of DCC size since p-type doping provided by PLAD along the DTI wall and n-type doping by photodiode decides the IPO level.

Finally, the conversion gain is compared between No-DCC and DCC structure. As shown in Fig. [11], DCC structure has conversion gain increased by 38%. After analyzing data we figured that the reduction of both junction capacitance and metallic capacitance contributes similarly. We also was able to optimize the process for our sensor which gives us additional 14% of CG increase. Eventually conversion gain of our sensor become comparable to the reference product even though adopting 2x4 shared structure compared to 2x2 shared structure of reference.

The overall performance of our sensor is summarized in Table 1.

IV. Conclusion

In summary, we have developed a 200Mp CIS with 0.56um pixel. The new CIS incorporated a new DTI structure, which enables Qcell technology with better overall performance. While main sensor properties are comparable to the previous generation, the new Qcell technology with DCC structure enables us to improve AF performance and random noise for extremely low light conditions. We will continue to search for the sub-micron-pixel mobile CIS technology based our new sensor.

Acknowledgement

We are grateful to Samsung S.LSI Division's Sensor Business Team for the analog and digital design and Samsung Foundry Division's Process Architecture Group for technical support for fabrication.

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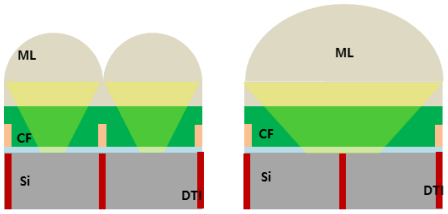


(a) (b)

Figure 1. A schematic diagram of (a) Tetra and (b) Qcell structures.

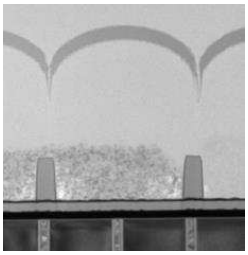
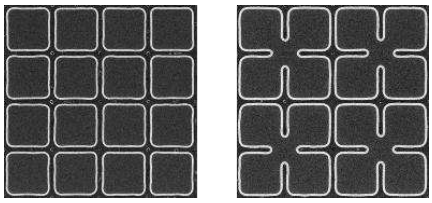


Figure 2. VSEM image of optical stack and DTI.



(a) (b)

Figure 3. (a) A cross section of conventional FDTI structure (b) new FDTI with DCC structure.

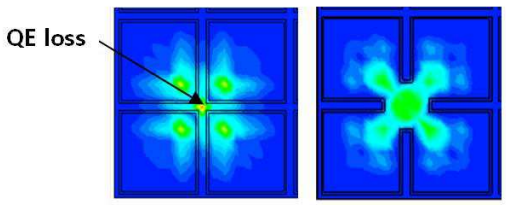


Figure 4. TCAD simulation of conventional FDTI and DCC structure.

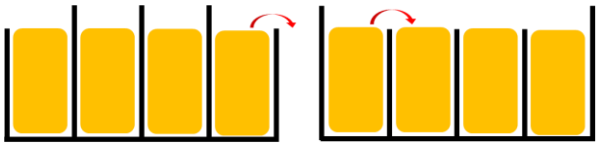


Figure 5. Schematic diagram of Non-IPO (Left) and IPO (Right) potential structure

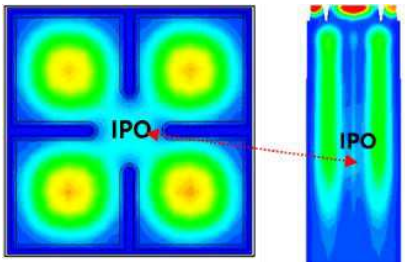
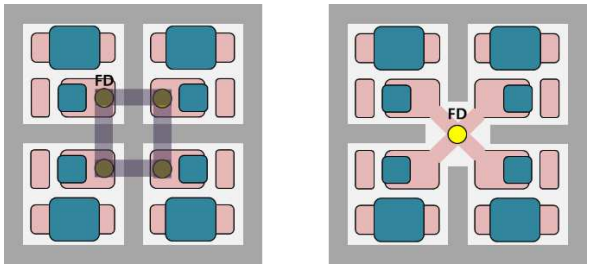


Figure 6. TCAD simulation of photodiode and IPO potential



(a) (b)

Figure 7. Schematic pixel structure (a) with no DCC and (b) with DCC.

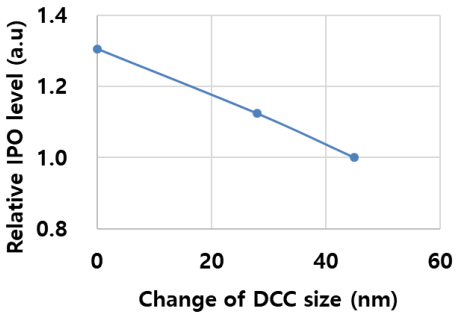


Figure 10. IPO level change according to DCC size

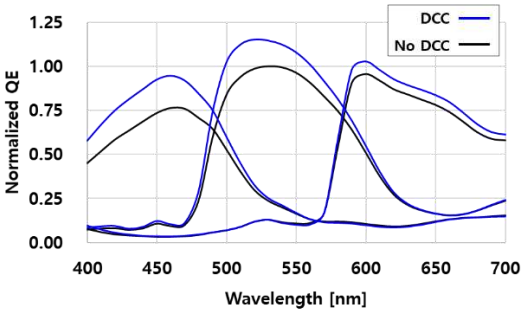


Figure 8. Normalized QE comparison between DCC (blue) and no DCC (black).

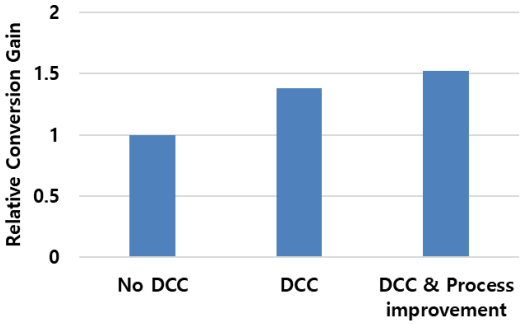


Figure 11. Comparison of conversion gain between No DCC and DCC.

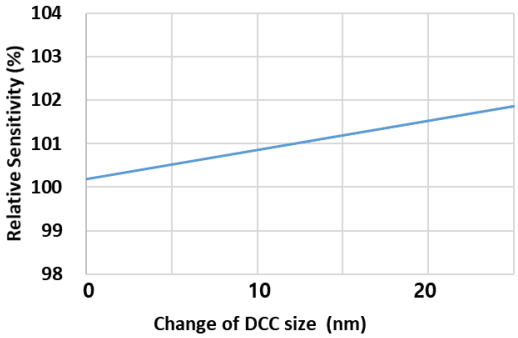


Figure 9. Change of Sensitivity relative to DCC size.

Items	Unit	Reference	This work
Pixel pitch	um	0.64	0.56
Linear FWC (1Pixel)	e-	6000	4700
Linear FWC (Binning)	e-	96000	75000
RN (multiple sampling on/off)	e-	2.2/3.4	1.6/2.3
RTS	ppm	4	1
Sensitivity / area	e-/lux.s/um^2	3784	3746
YSNR [20lux]	dB	30.7	29.9

Table 1. Summary of performance

0.56µm-pitch CMOS image sensor for high resolution application

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***Abstract*—In this paper we describe a 200Mpixel CMOS image sensor with 0.56µm pixels implemented in a 28nm process. This pixel technology is the next generation development after our 0.61µm pixel. The sensor demonstrates a full well capacity of 5.5ke- with lower dark current and read noise than our previous generation pixel. In addition, this sensor demonstrates similar quantum efficiency (QE) and phase detection autofocus (PDAF) performance in comparison to our previous generation pixels. This sensor also implements multiple functions including switched conversion gain and high-speed readout.**

Keywords—CMOS image sensor, 0.56 µm pixel, small pixel, 200Mp

I. INTRODUCTION

In the field of CMOS image sensors (CIS), pixel miniaturization drives product innovation. The pursuit of continuously shrinking pixel sizes, while maintaining performance, forms the foundation of CIS development in recent history. Demand for high-resolution mobile image sensors have escalated, with mobile CIS product resolutions increasing from 24Mp to 200Mp in under 5 years. Despite attaining pixel pitch scaling below the wavelength of visible light, better image quality is consistently achieved due to progressive improvements in image signal processing [1]. While pixel downscaling offers higher pixel counts in smaller form factors, there is a trade-off between pixel miniaturization and overall performance, as the reduction of light-receiving areas contributes to CIS performance degradation [2].

High-resolution image sensors are almost exclusively realized using wafer stacking, in which pixel and read-out circuitry are separated onto independent wafers. Additionally, high-resolution pixel read-out requires more select-lines for control, which increases capacitance, causing lower read-out rates. Dual-Row selection enables fast pixel binning without increasing the number of bit-lines, achieving fast read-out without additional circuitry.

Small-pixel image sensors suffer often from lower full well capacity (FWC). Therefore strong isolation potential barriers are required to mitigate this problem. In this paper, we present a 0.56µm pixel, 200MP stacked CMOS image sensor, developed using a new, CIS-dedicated 28nm process. Shrinking the process node frees up chip space, providing room for additional devices and functions, such as switchable conversion gain (SCG) and circuitry for low noise and high speed readout.

The 0.56um pixel developed in this work achieved high FWC without sacrificing dark performance. Compared to its 0.61µm predecessor, a higher FWC is obtained without image lag or blooming, while dark current and white pixels (WP) remain comparable. This device is capable of pixel binning mode with switchable conversion gain, which provides high dynamic range and FWC to produce higher image quality. Shared floating diffusion (FD) is utilized for 16C binning mode to lower read noise.

II. PIXEL ARCHITECTURE AND TECHNOLOGY

A. Pixel Stacking Process technology

The 0.56µm pixel development discussed in this work adopts a new, CIS-dedicated 28nm process node for the pixel wafer, instead of the 45nm process node employed in previous generation devices. The logic wafer follows the 40nm process node used in our previous small pixel stacking sensors [3,4]. Compared with the 0.61µm pixel design, the 0.56µm-pitch device benefits from increased design flexibility, enabled by the CIS-dedicated 28nm process node. Due to the chip space conserved by the 28nm node, the device implements an additional row select transistor to achieve fast readout. Additional layout strategies are applied for improved noise performance and higher FWC. Figure 1 shows the pixel transistor layout comparison between 0.61µm [Figure 1a] and the 0.56µm [Figure 1b] used in this work. Each transistor is isolated by shallow trench isolation (STI), while each pixel is separated by an improved backside deep trench isolation (BDTI), minimizing leakage and optical cross-talk, respectively [3]. By adopting CIS-dedicated 28nm process node, each group of pixels implements parallel-connected SFs to increase SF width, which works together with the 2-Row Select transistors design to maximize readout in the large, 200MP device. Without such strategies, such a large device may suffer from slow readout; A vertical transfer gate (VTG) architecture is implemented to shift the photodiode deeper into the silicon region, 28nm pixel process provides more flexibility for the design and placement of transistors in the limited space of the 0.56µm-pitch pixel [3,4,5]. This also enables the placement of an additional transistor within the pixel to support switchable conversion gain for high-dynamic applications.

B. Pixel architecture

The pixel array size is 200 mega-pixels (16384(H) x 12288(V)), with an optical format of 1/1.395" and a pixel pitch of 0.56µm. A 2x4 shared pixel architecture is utilized, as shown in the circuit schematic in Figure 2a. A new 2-Row Select transistor design is implemented, in which each 2x4 shared pixel is independently controlled by separate control signals, RS0 and RS1. In full-size or 4-cell mode, RS0 is

active for both left and right shared pixels, and their signals at FD are separately and concurrently readout through two separate bit-lines. In 16C mode, RS1 is active for both left and right shared pixels, with the RS1 of both shared pixels connected to the same bit-line. The RS1 of alternating rows connect to separate bit-lines (labeled as "A" and "B"-cells in Figure 2b), keeping the same loading for both bit-lines. This alternating bit-line control scheme reads out two 16-cell binned signals through the two-bit lines and two column ADCs. This enables 16 cell-binning mode for 0.56µm device achieves faster readout speed without increasing the number of bit-lines. Table I shows a comparison of the 0.61µm and 0.56µm device architectures.

C. QPD and Color filter pattern

Due to smaller on-chip lens (OCL) fill factor, small pitch pixels suffer from significant QE degradation. The QPD, or Quad-Bayer coding with 2x2 OCL, is a design that uses one OCL and the same color filter in a 2x2-pixel array, producing high-resolution and high dynamic range image sensors [6]. The QPD is an important technology to improve QE for small pixel image sensors and was implemented in this work [Figure 3].

III. EXPERIMENTAL RESULT

Figure 4 shows the FWC trend with respect to pixel pitch. The dotted line represents the FWC achieved by simple pixel area scaling, based on a 1.0µm pixel. The empty circles show data from our previous generation 0.7µm and 0.61µm technologies. The actual FWC demonstrated by the 0.7µm, 0.61µm, and 0.56um devices are much higher than the value predicted by simple scaling. This FWC enhancement was achieved by deep photodiode technology, in which the photodiode potential is situated in the deeper silicon region. Through adopting this technology, the 0.56µm device achieved 5.5ke- FWC without lag or blooming. Although we increased the n-type/p-type ion-implantation dose, creating higher electric fields, our improved BDTI technology mitigates the impact of surface defects, achieving dark current and WPs comparable to the previous generation. Table II shows the performance comparison between the 0.61µm- and 0.56µm-pitch devices; the 0.56µm-pitch pixel shows better performance than the 0.61µm-pitch device in all aspects, including very low noise level and phase detection auto focus (PDAF) performance.

Figure 5 presents the optical performance results, which shows the 0.56µm-pitch pixel's QE and cross-talk improves from the 0.61um-pitch reference pixel, while the image quality remains consistent. Figure 6 shows a sample color image taken with the 0.56um pixel in 4-cell mode.

IV. CONCLUSION

In this work, we developed a new 28/40nm 200 mega-pixel stacked image sensor with 0.56µm pixel pitch. This device achieved a FWC of 5.5ke- without image lag or blooming, and with dark performance comparable to the previous generation 0.61µm-pitch device. We demonstrated better QPD QE performance than the 0.61µm in the visible light range. A Dual-Row Select layout is employed to improve readout speed without adding circuitry (bit-lines), resulting in an increased frame rate compared to previous generation devices. A switchable conversion gain is enabled, such that the 0.56µm device reaches a 16C2 FWC 2x higher than the previous 0.61µm device.

ACKNOWLEDGMENT

We are grateful to Taiwan Semiconductor Manufacturing Company, Ltd. for chip fabrication and their technological support for both sensor and logic wafers to achieve 200 mega-pixel CIS with 0.56µm pixel.

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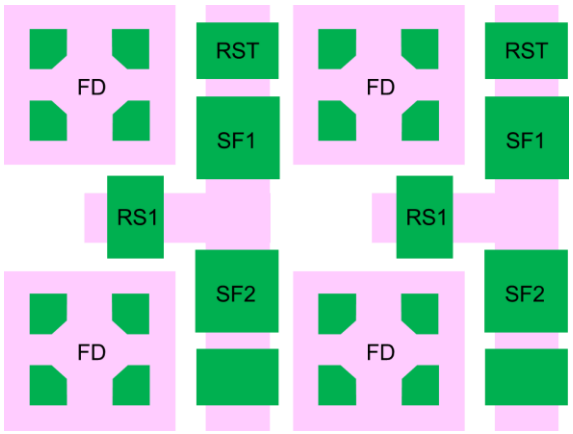

Figure 1a: 0.61um pitch pixel architecture

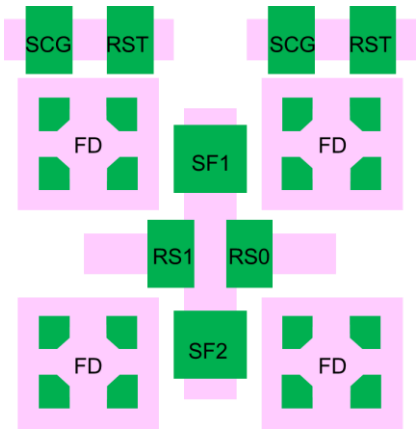

Figure 1b: 0.56um pitch pixel architecture

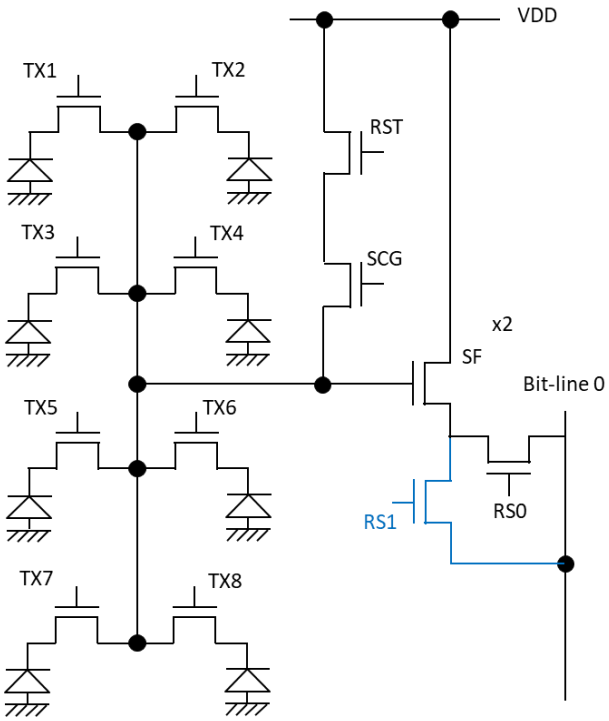

Figure 2a: Circuit schematic of the 0.56µm pixel.

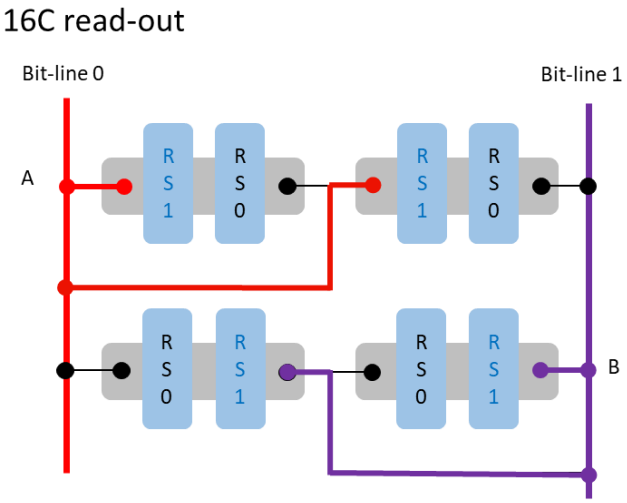

Figure 2b: 2-Row Select readout sequence on 16C mode

Table I: 0.61µm v.s 0.56µm architecture comparison

Pixel size	0.61um	0.56um
Resolution	200M/50M/12.5M	200M/50M/12.5M
Frame rate	8/24/90	8/30/120
Pixel Tech.	45nm	28nm
ASIC Tech.	40nm	40nm
Readout speed	1RS	2RS
Noise/RTS	2SF	2SF
Multi CG switch	No	Yes

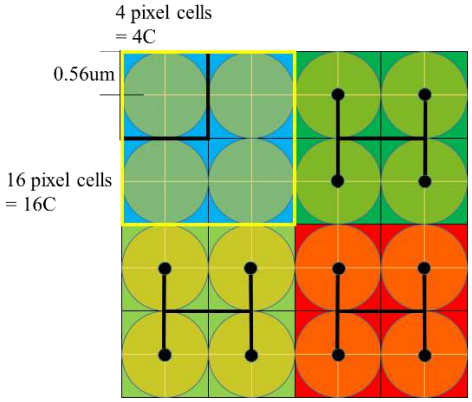

Figure 3: Schematic of color and cells definition

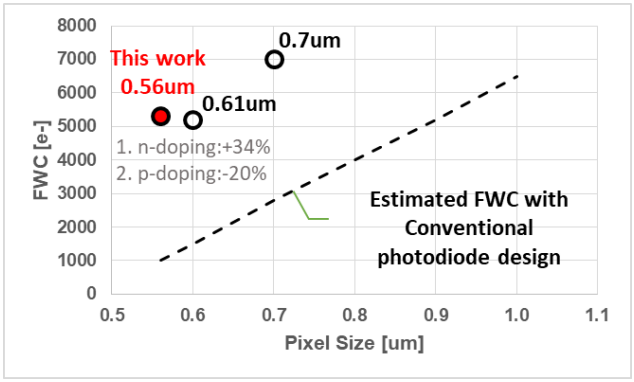

Figure 4: FWC trend with respect to pixel pitch

Table II: Performance comparison 0.61µm v.s 0.56 µm

		Unit	0.61um	0.56um
Full-well	1 pixel	e-	5.3K	5.5K
	16C binning	e-	49K	72K
Lag		e-	<1	<1
Blooming		%	<1	<1
DC		e-	18.6	17.6
Read Noise	1x Gain	e-	23.6	20.2
	16x Gain	e-	4.5	4.1
	64x Gain	e-	NA	1.6**
DR	1x Gain	[dB]	64.4	71
PDAF	Selectivity	ratio (Normalized)	1	1.05

** Low Noise mode

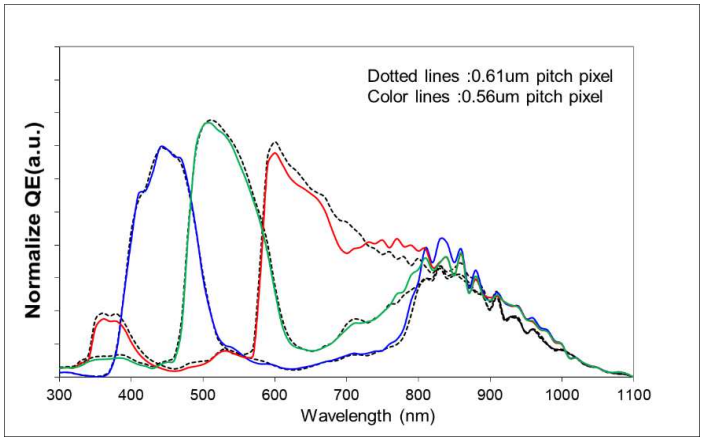

Figure 5: QE curve comparison

Figure 6: Picture demonstration of 12.5M pixels

0.64 µm 200 MP Stacked CIS with Switchable Pixel Resolution

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***Abstract*—This paper presents a 0.64 µm 200 MP stacked CMOS Image Sensor (CIS) in 65/28 nm process. The implemented sensor provides 200 MP, 50 MP, and 12.5 MP with switching pixel resolution through optimized readout scheme and remosaic algorithm based on same color filter in 4 x 4 pixels. During dark conditions, the 2.56 µm 12.5 MP resolution maximizes the pixel sensitivity whereas the 0.64 µm 200 MP resolution provides the most detailed image during bright conditions. Additionally, grid pattern and flatness of color filter material help to improve the pixel sensitivity by 8% with 0.64 um pixel. Especially, the 16,384 ADCs operate simultaneously to convert pixel outputs to Image Signal Process (ISP) chain and the sensor provides fast videos for both 4K 120 frame per second (fps) and 8K 30 fps through 3-lane CPHY 4 Gsps/lane. The measured random noise of the implemented chip is 2.4e- at analog gain of x16. The proposed 200 MP stacked CIS provides support for lossless zoom, adaptive region of interest, and switchable resolution for better User eXperience (UX).**

Keywords—CMOS Image Sensor (CIS), 200 MP CIS, switchable pixel resolution.

I. INTRODUCTION

In the last twenty years, the CMOS Image Sensor (CIS) in mobile applications has been developed by using VGA up to 200MP. Moreover, the pixel size has decreased by 1/1000 times from 5.6 um to 0.56 µm. Fig. 1 illustrates the pixel resolution trend of Samsung CIS products for smartphones used in the previous decade. Since 2015, tetra pixel (2 x 2 pattern) [1] has been adapted by 16 MP, 24 MP, and 48 MP. After that, the nona pixel (3 x 3 pattern) [2] is matched with 108 MP and the tetra square pixel (4 x 4 pattern) is a proper pixel arrangement for 200 MP. Each pattern has same colors such as blue, red, and green. Samsung has achieved the world's first mass production of 0.64 µm 200 MP sensor. The pixel pitch is successfully reduced to implement 0.6 µm and 0.56 µm with 200 MP.

The proposed 200 MP sensor has the following three advantages:

- Switchable pixel resolution helps to provide various camera modes such as still image of 12.5 MP, 50 MP, and 200 MP or 4K and 8K videos. Especially, this sensor can provide the detailed image with 200 MP and the bright image with 12.5 MP.
- Tetra square pixel is easy to enhance sensitivity as changing from sixteen 0.64-µm pixel into one 2.56-µm pixel with re-mosaic algorithms. Additionally, the sensitivity is improved by 8% after changing grid structure and optimizing color filter material.
- There is no loss in image quality when zoom in by x2 and x 4 or cropping any region of interest because digital zoom is not applied.

This paper describes the implementation of 65/28nm stacked CIS which consists of 0.64 µm tetra square 200 MP on the top chip and logics on the bottom chip. The measured Random Noise (RN) is 2.4e- with multiple sampling at 16x analog gain.

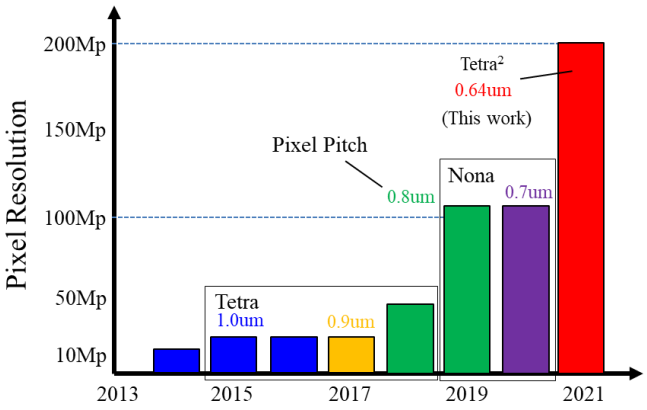


Fig. 1. CIS Pixel Resoultion and Pitch Trend with Pixel type

II. PROPOSED SENSOR ARCHITECTURE

Fig. 2 illustrates a block diagram of the implemented CIS that consists of a top chip for pixel array and a bottom chip for logic circuits throughout Through Silicon Via (TSV).

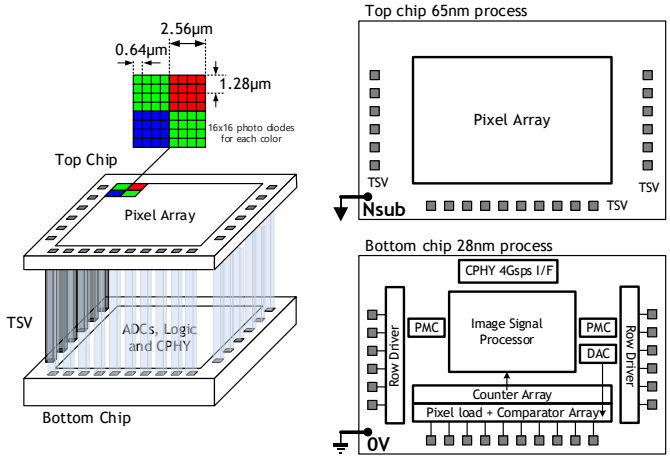
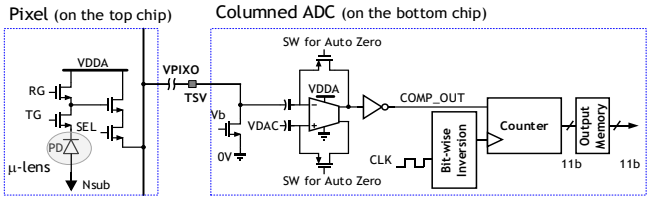


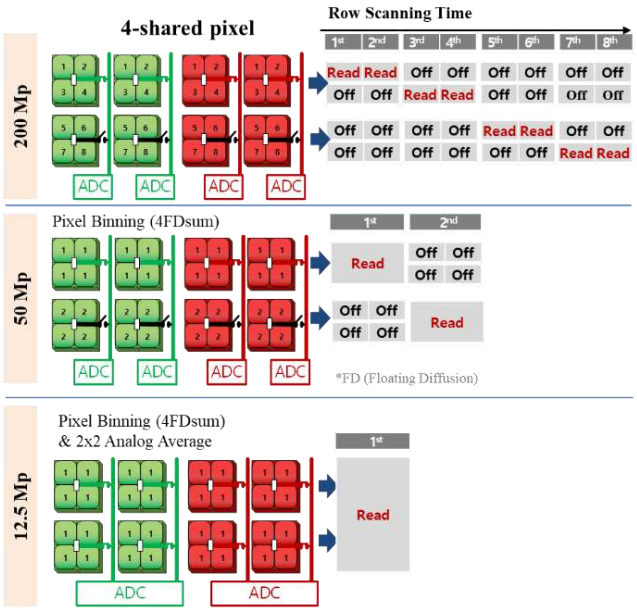
Fig. 2. Architecture of Proposed Stacked Sensor

The top chip consists of 16,384 x 12,288 pixels with -0.6V Negative voltage Substrate (Nsub) to reduced power consumption. The output signal from pixels on the top chip is transferred to the input of 16,384 comparators on the bottom chip. Each comparator is operated as a single-slope Analog-to-Digital Converter (ADC). To enhance noise and shading, two row drivers and Power Management Circuits (PMCs) are adapted. An Image Signal Processor (ISP) and three lanes CPHY serial interface circuit with 4Gsps/lane are implemented for various functions and camera modes.

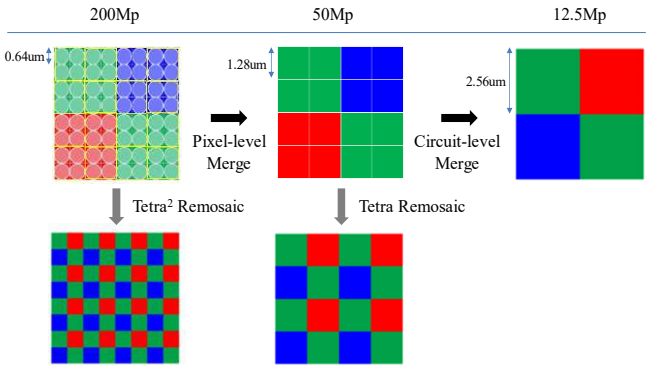
Fig. 3(a) illustrates the signal chain for readout of Photo-Diode (PD) under one micro-lens. After PD exposure period, the SEL transistor is turned on for PD readout. During initial reset of the ADC, auto-zeroing scheme is adapted to cancel reset noise of pixel and column Fixed Pattern Noise (FPN). Then, a reset code is inverted by Bit-Wise Inversion (BWI) for digital Correlated Double Sampling (CDS) operation in the counter. After TG is turned on, the differential value between the signal and the previous offset during ADC reset period is used to convert the signal from PD and transfer it to counter output memory. Fig. 3(b) illustrates the readout scheme of 200 MP, 50 MP, and 12.5 MP modes. During rolling the scanning sequence, all pixels from 4-shared pixel are separately transferred by the SEL transistor for 200 MP, four merged photodiodes on Floating Diffusion (FD) are summed up for 50 MP, and additional analog average scheme with four FD summation is applied for 12.5 MP. Fig. 3(c) illustrates how to obtain Bayer color pattern from each resolution with switchable pixel resolution.



(a) Column of Schematic



(b) Readout Details



(c) Bayer Pattern for Modes

Fig. 3. Mode Change Scheme for 200 MP, 50 MP, and 12 MP

III. Evaluation Results

Table I summarizes the specifications of the designed sensor. This sensor was fabricated with a 65nm NMOS process with 5-metal layers for the top chip and a 28nm CMOS process with 8-metal layers for the bottom chip. The pixel array consists of 200 M (16,388 × 12,288) pixels with 0.64-µm pixel pitch. The output of 200 MP provides eight frame per second (fps) with full well capacity of 6,000e-. With tetra readout, 50 MP reaches 30 fps with full well capacity of 24,000e- and 12.5 MP reaches 60 fps with full well capacity of 96,000e- with tetra square. The power supply of 2.2V, 1.8V and 1.0V are used for pixel/analog circuits, PLL/DPHY/IO, and digital circuits, respectively. RN is 2.2e- with multiple sampling at analog gain of x16 while it is 3.4e- without multiple sampling. In this paper, there is no information provided for staggered High Dynamic Range (HDR) and iDCG (intra-scene dual conversion gain) HDR even though HDR features are embedded for mass production.

TABLE I. Specification

Parameter	Value
Process technology	Pixel: 65nm 1P5M Logic: 28nm 1P8M
Number of effective pixels	16,384 (H) x 12,288 (V)
Pixel size	0.64µm
Maximum frame rate	8fps for 200MP 30fps for 50MP 60fps for 12.5MP
Supply voltage	Pixel/Analog circuit: 2.2V (PD GND -0.6V) PLL/CPHY/IO 1.8V Logic: 1.0V
Full well capacity	6,000e- @ 200MP 24,000e- @50MP 96,000e- @12.5MP
Random noise	3.4e- w/o multiple sampling @ analog gain x16 2.2e- w/ multiple sampling @ analog gain x16

There were several design challenges that we faced during the implementation of 0.64 µm 200 MP sensor.

- First of all, the power consumption is crucial. To reduce the power consumption, 200 MP tetra square remosaic is implemented by S/W in Application Processor (AP) instead of embedded H/W in the sensor. Therefore, the image processing speed is limited by channel lag. Note that the remosaic algorithm complexity has increased due to the image quality enhancement technique.

- Secondly, the pixel and analog circuit co-simulation is hardly performed. For example, dark shading simulation takes longer time even though the full resolution is not included. Thus, the proper results with 200 MP cannot be obtained because of nodal complexity of current simulation environment. In coming days, the model hardware correlation will be improved by trying different methods.

- Last, the designed columned comparator layout is very narrow inside 0.64 µm column pitch. Therefore, the comparator is more sensitive not only to avoid crosstalk by shielding metals but also to balance parasitic capacitance in each comparator by routing freedom limit.

In day light, resolution of 200 MP provides the more detailed image. Fig. 4 presents the results of zoom mode between 200 MP and 50 MP. The pixel can maintain the same image quality when the region of interest is changed when in zoom mode at 200 MP. Fig. 5 shows the experimental result of the implemented 200 MP chip with evaluation board and SLR lens. The printed image size is 28m x 22m and it maintains the proper image quality. Therefore, it provides a clear and proper image.

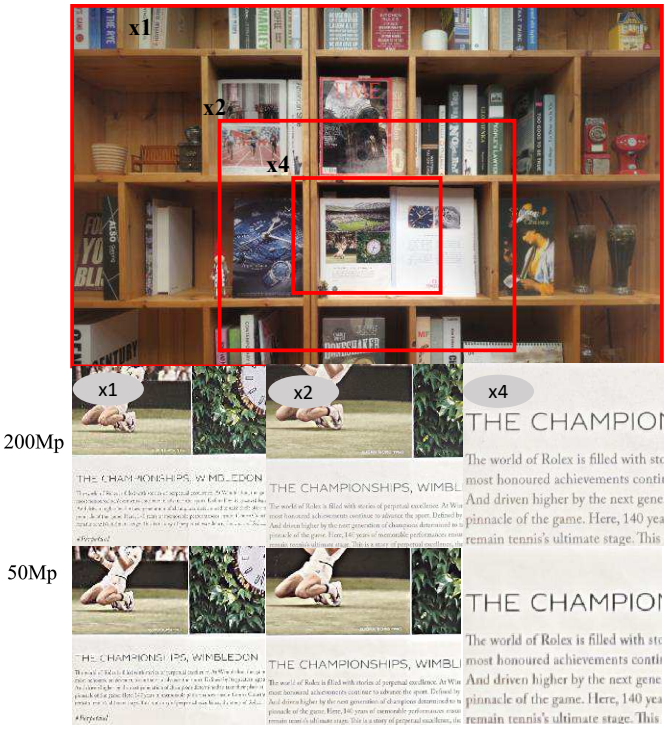


Fig. 4. Comparison between 200 MP and 50 MP with zoom x1, x2, and x4

Fig. 5. Detailed Captured Image with 200 MP (Deimensions of 28m x 22m)

Fig. 6 illustrates a chip microphotography of the implemented 200 MP stack sensor. The chip size is 11,799 µm x 10,758 µm. The top chip consists of pixels and the bottom chip consists of the columned ADC (comparator array, counter array, and a DAC), two row drivers, two PMUs, logics, and a CPHY.

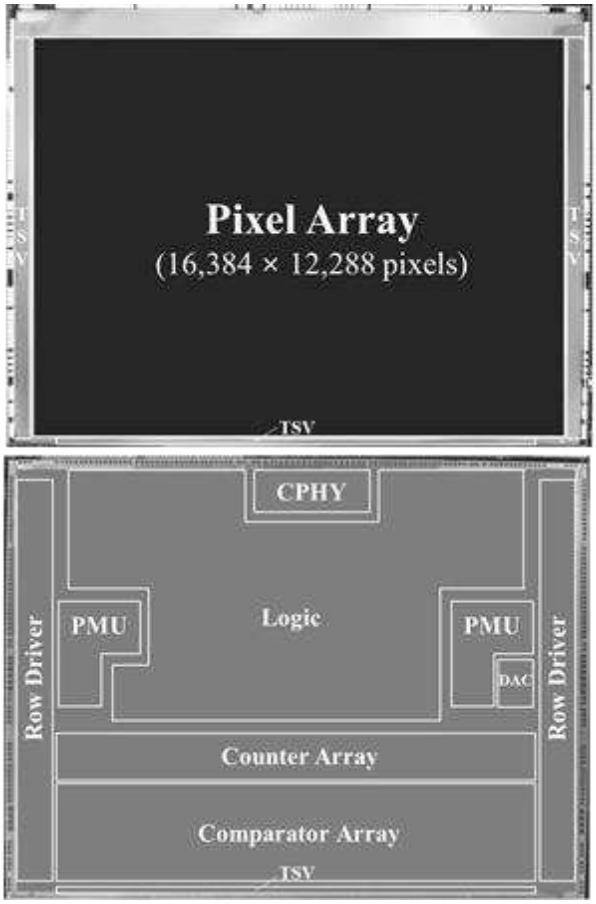


Fig. 6. Chip Microphotograph

Table II describes the comparison with other works [3]-[4]. This work is the first mass production 200 MP sensor for mobile applications. As of now, mass production of 200 MP sensor has been produced by 0.56 µm.

TABLE II. COMPARISON

Parameter	This work	[3]	[4]
Stack process	Top: 65nm Bottom: 28nm	Top: 40nm Bottom: 22nm	Top: 65nm Bottom: 28nm
Number of pixels	200MP	200MP	200MP
Pixel pitch	0.64μm	0.61μm	0.60μm
Full well capacity	6,000e-	5,000e-	10,000e-
Pixel shared type	4-shared	8-shared	8-shared
Trench type	Frontside deep trench isolation	Backside deep trench isolation	Frontside deep trench isolation
Transfer gate type	Single VTG	Single VTG	Dual VTG

IV. CONCLUSIONS

This paper presents the first mass production implementation of 200 MP stacked CIS with 0.64 μm-pitch pixels. The super resolution sensor over 200 MP is suitable to take pictures of objects on earth from satellites or adapt user experiences with various machine learning algorithms for the next generation sensors.

ACKNOWLEDGEMENT

The authors would like to thank the HP1 product development participants in Sensor Business Team for enduring a hard work during mass production.

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Image sensor family with 1.40 µm pixel, 10ke- LFW, NIR-enhanced QE, extended dynamic range, and low power consumption

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Abstract*— *We are reporting on an image sensor family with 1.40 µm pixel size, multiple resolutions (5 MP, 8 MP, 20 MP), stacked backside illuminated, fabricated in 65 nm technology, with 6 µm silicon epitaxial thickness. The 1.40 µm pixel is the smallest pixel for low light surveillance imaging performance, combining low noise, increased near-infrared quantum efficiency, enhanced dynamic range and low power consumption for integration in energy-efficient battery-operated camera systems.

I. Introduction

We have developed a rolling shutter low power consumption image sensor family with 1.40 µm pixel size and array resolutions of 5 MP, 8 MP, and 20 Mp. Sensor design combined advanced technology features to address demanding requirements for surveillance, consumer and industrial imaging application. It demonstrates good low light performance, high responsivity in near infrared (NIR), and enhanced dynamic range. To the best of our knowledge this is the smallest pixel size to date to meet performance requirements for low light surveillance applications [1].

II. Pixel design and Operation

The pixel was designed in stacked backside illuminated (BSI) CMOS 65 nm technology, with 6 µm silicon epi and partial backside deep trench isolation (BDTI). To further increase the pixel quantum efficiency (QE) in the NIR spectrum for surveillance imaging, the backside process included a variant with inverted pyramids to extend the optical path of NIR photons [2]. The 1.40 µm pixel size was chosen for optimized trade-off between spatial resolution, signal-to-noise ratio (SNR) in low light conditions, and dynamic range.

Photodiode (PD) implants, potential profile, and layout were optimized through Technology Computer-Aided Design (TCAD) simulations and through silicon design-of-experiment (DOE) work to achieve 10 ke- linear full well (LFW) capacity while: (a) Maintaining a limited signal swing at the floating diffusion (FD) for reduced power consumption [3] and (b) Avoiding charge lag. Figure 1 presents vertical cross-section and top view of the PD in TCAD. The optimal PD pinning voltage allowed sufficient FD signal swing at a pixel supply voltage (Vaapix) not higher than 2.8V, which was essential in order to maintain low power consumption. Figure 2 presents LFW vs Vaapix curves in low conversion-gain (LCG) and high conversion-gain (HCG) modes. DOE analysis was also focused on ensuring pixel isolation, passivation of Si/SiO2 interface with the BDTI, and for preventing bright pixels - in order to minimize dark signal non-uniformity (DSNU) at elevated temperature conditions.

Figure 3 presents simplified schematics of the pixel circuit. The architecture is 1×2 shared row-wise with a dual conversion gain (DCG) transistor, TX1 and TX2 are the transfer gates, SF is the source follower transistor, RS is the row-select line, Pixout is the output pixel voltage, and SHR and SHS are the sample-and-hold reset and signal lines, respectively. Linear mode output is in 10-bit data format. Dual gain readout [4]- [5] is used for the enhanced dynamic range (eDR) mode. In eDR mode, the intra-scene dynamic range, which is defined as the ratio between the effective LFW and the total noise in the dark with 16.7 ms integration time, is up to 72.5 dB, and the data format is 12-bit.

Figure 4 presents the timing diagram of the circuit in eDR mode. In this mode, after charge integration, each pixel is read twice in two consecutive reads with high and low conversion gain, respectively. The HCG readout is correlated double sampling to cancel *kTC* noise on FD. The LCG readout is double sampling, which doesn't cancel the *kTC* noise component. Since *kTC* noise is lower than photon shot noise when the photo-signal is high, its unwanted contribution to the drop in signal-to-noise ratio (SNR) at the transition point between the HCG and the LCG reads is very small.

III. Pixel performance Characterization

Pixel characterization was conducted by methodologies that are used to evaluate signal and noise properties [6]. Figure 5 presents dark signal histogram at junction temperature, Tj, of 80C and 33 ms integration time. The standard deviation of the measurement, after conversion to charge units using the corresponding system gain, is the dark signal non-uniformity (DSNU) which equals 1.5 e-. Figure 6 shows read noise histogram at 25C with maximum gain, where the root mean square (RMS) of the distribution is 1.3 e-. Figure 7 presents photon-transfer curve (PTC) measurement at gain that is sufficiently low to extract the PD LFW. To highlight eDR mode dynamic range, Figure 8 is showing the eDR SNR curve and compares it to the SNR curve in linear mode with low conversion gain.

Three color filter array (CFA) variants were implemented to address specific image quality requirements in targeted markets: Bayer ('RGGB'), RGB-IR with 4x4 unit cell, and monochrome ('Mono'). The quantum efficiency (QE) curves of

the three variants are shown in Figure 9. The RGB-IR variant was developed with a backside process skipping the inverted pyramids for ensuring maximum dynamic range in the R, G, B channels. NIR QE enhancement was not required as NIR absorption in the silicon epi was sufficiently high to fulfill the requirements of the specific RGB-IR applications [2].

Figure 10 presents images that were captured in low light conditions under (a) visible and (b) NIR illumination. Both images were captured when the sensors were activated with maximum gain and integration time of 16.7 ms, where illumination conditions at the scene were (a) 5500K, 0.66 lux, and (b) 940 nm, 26.3 nW/cm2. Images are presented in signal range of 0 – 330 DN. The F#2 lens that was used during image capture had a VIS/940 nm dual-band filter with transmission greater than 95% in the visible band and at 940 nm. Figure 11 shows photos of the packaged image sensor products, where the 5 MP and 8 MP products are in a chip-scale package (CSP) and the 20 MP product is in a mixed-pitch ball grid array (MPBGA) package.

The SNR1s metric was introduced by Sony Semiconductor Solutions Corporation for quantitative evaluation of SNR of security cameras at low illumination [1]. SNR1s is defined as the illuminance on a gray target with 18% reflectance under 3,200K illumination for which SNR of the green channel equals 1, or 0 dB, when the camera is activated at room temperature with 1/60 sec exposure time and a F#1.4 lens that has 95% transmission and a CM500 infrared-cut filter. Figure 12 presents SNR1s values versus pixel size for various Sony STARVIS sensors – with smallest pixel size of 1.45 µm [1], and for the sensor family developed in this work. The SNR1s values are distributed along a curve decreasing with pixel size - as expected from the contribution of responsivity, i.e., the smaller the pixel the more challenging the low light performance and hence the more elevated values of SNR1s. The SNR1s performance of the 1.40 µm pixel developed in this work is improved versus the model described by the pixel area fit line.

The main performance parameters of the pixel array, applicable to the three array resolutions, are summarized in Table 1. The table presents SNR1 values as calculated for different conditions, such as at 80C and under 940 nm illumination.

IV. Conclusion

In summary, we are reporting on the development of a rolling shutter, low power consumption image sensor family with 1.40 µm pixel size, multiple resolution variants (5 Mp, 8 Mp, 20 Mp), BSI stacked, 65 nm technology, with 6 µm epi silicon, partial BDTI, and backside process option for enhancement of NIR QE. Sensor performance has demonstrated meeting the most demanding requirements for imaging in low light conditions in surveillance, consumer and industrial applications.

Acknowledgment

The authors gratefully acknowledge the contributions of Purnendu Kumar, Muhammad Rahman and Frank Chen and other onsemi engineering team members.

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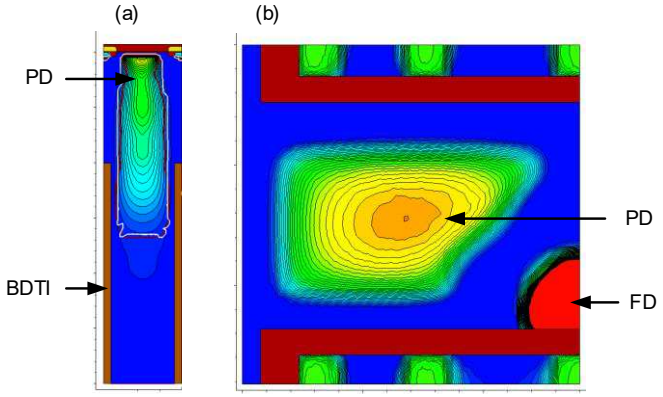

Figure 1. TCAD simulation: (a) Vertical cross-section in the middle of the PD;(b) Top view of the PD in the shallow region. As it can be seen, the PD is completely isolated from neighboring pixel.

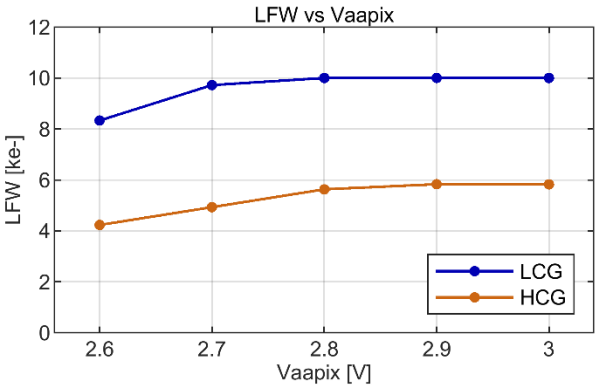

Figure 2. LFW vs Vaapix in LCG and HCG modes.

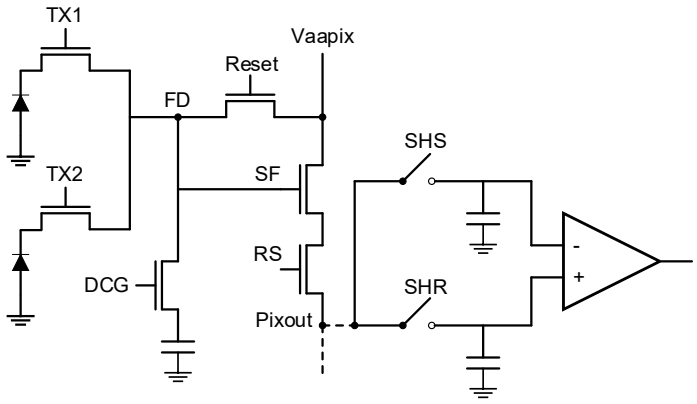

Figure 3. Simplified schematics of the pixel architecture, which is a 1x2 shared with a DCG transistor.

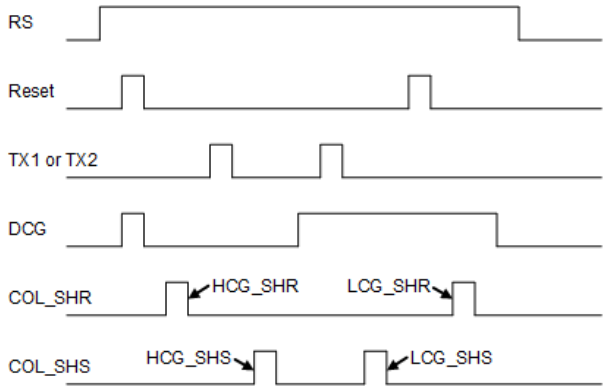

Figure 4. Timing diagram in eDR mode.

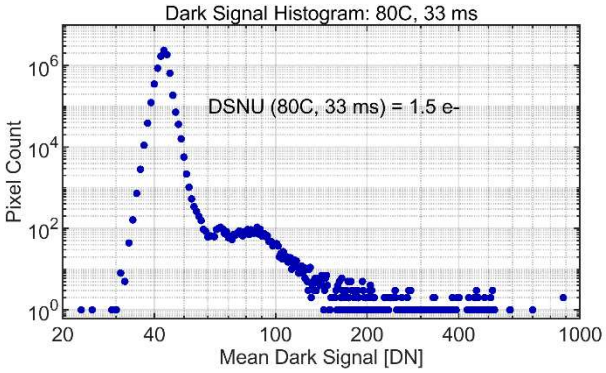

Figure 5. Dark-signal distribution at 80C, high gain, and 33 ms integration time. DSNU equals 1.5 e-.

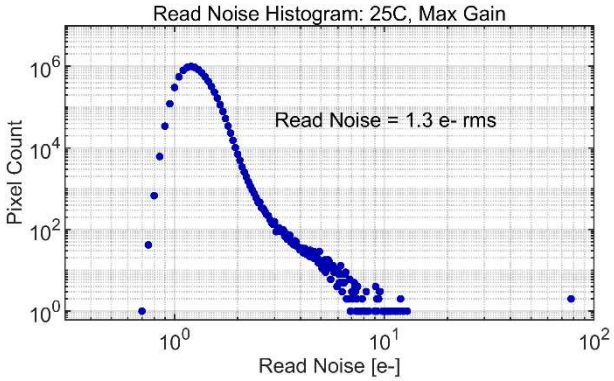

Figure 6. Read noise distribution at 25C.

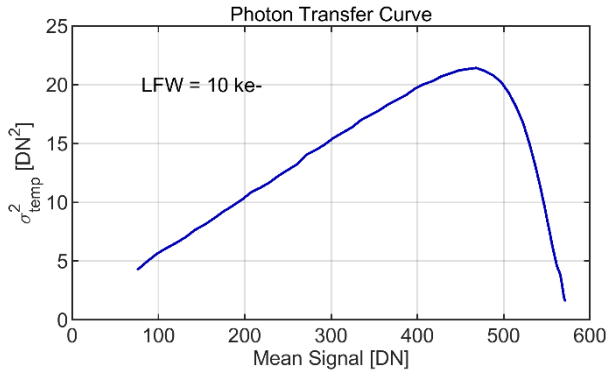

Figure 7. Photon transfer curve at low gain.

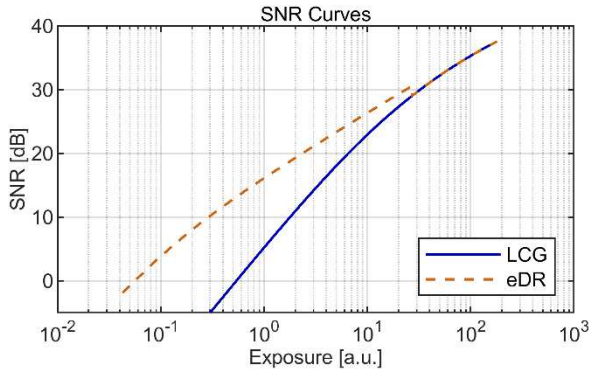

Figure 8. SNR curves in LCG and eDR modes.

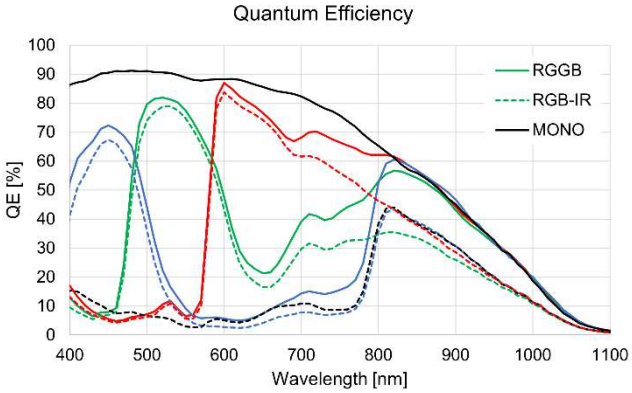

Figure 9. QE curves of the RGGB, RGB-IR, and mono CFA variants of the product.

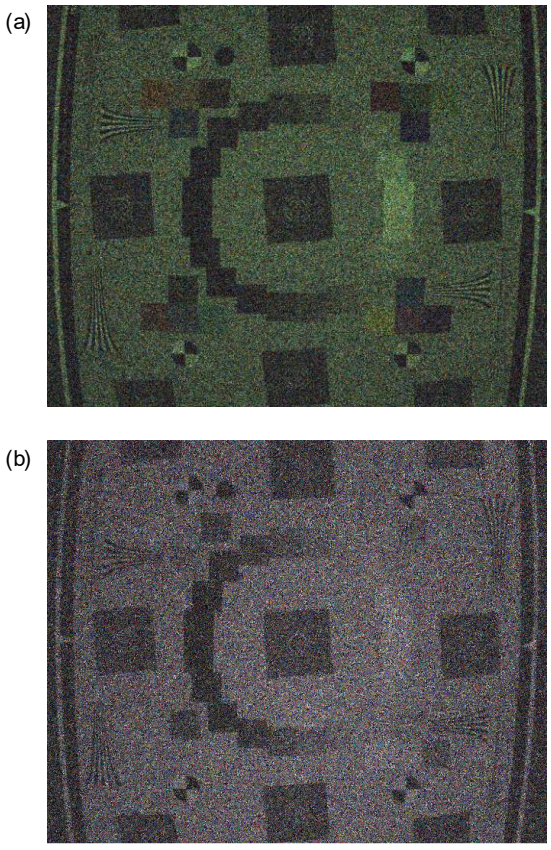

Figure 10. Color and NIR images in low illumination conditions: (a) 5,500K, 0.66 lux, and (b) 940 nm, 26.3 nW/cm^2

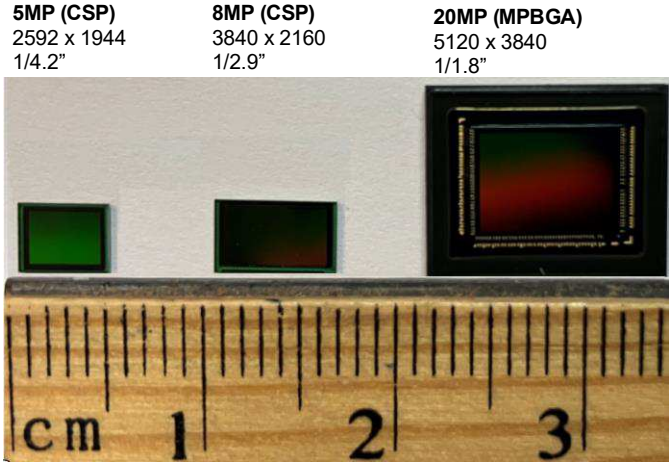

Figure 11. Photos of the 5, 8, and 20 MP image sensor products.

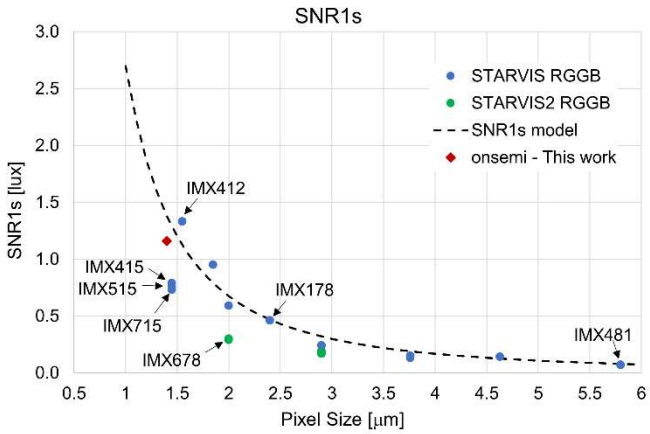

Figure 12. SNR1s of various security image sensor products versus pixel size.

Table 1. Sensor performance parameters

Parameter	Units	Typical values
LFW	ke-	10.0
DSNU, 33 ms, 80C	e-	1.5
Dark current, 80C	e-/s/pixel	66.0
Read noise, max gain, 25C	e- rms	1.3
eDR mode intra-scene dynamic range	dB	72.5
SNR1s at scene, 25C, 3200K, CM500, 16.7 ms, max gain	lux	1.2
SNR1 at image plane, 25C, 16.7 ms, max gain	e-/pixel	2.1
SNR1 at image plane, 80C, 940 nm, 16.7 ms, max gain	µW/cm^2	4.5
SNR1 at image plane, 80C, 16.7 ms, max gain	e-/pixel	2.3
Power consumption, 10-bit, 30fps, full resolution	mW	5 Mp: 100 8 Mp: <180 20 Mp: <280