Trends and Developments in State-of-the-Art CMOS Image Sensors

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***Abstract*— The state-of-the-art in CMOS image sensors (CIS) is constantly evolving. Backside, stacked imagers are now well established and global shutter and dynamic range are priorities. The industry continues to reduce pixel pitch and increase array resolution. A snapshot of the current pitch (now entering the sub-0.6 µm generation) and resolution is provided. Elements of the signal path required for high quality images are described along the transduction path, beginning with Phase Detection Autofocus (PDAF) pixels and Color Filter Arrays (CFA). The aperture grid and trench technologies required for effective isolation are reviewed followed by the critical pixel transistors; the transfer FET and the Source Follower. The analog signal is moved off-chip using Direct Bond Interface (DBI) and Through Silicon Vias (TSV) to the underlying Image Signal Processor (ISP) where digitization and signal processing is performed; trends in these topics are discussed.**

I. INTRODUCTION

Originally developed to exploit the economics of mass production CMOS processes, CMOS image sensors (CIS) are now highly specialized devices with process steps customized for optical detection. In an interesting reversal the technology being developed for a sensor is being applied to high volume CMOS; for example, Direct (Hybrid) Bonding Interface (DBI), driven by stacked CIS devices is widely used in processor design. Phase Detection Autofocus (PDAF) and Color Filter Arrays (CFA) augment camera performance. Pixel pitches are now below 0.6 µm (Samsung and OmniVision) and need optical grid apertures and deep trench isolation. Trends in these elements and the subsequent transfer FET and Source-Follower are reviewed, followed by pitch reduction in the DBI and the often-overlooked Image Signal Processor (ISP). The ISP performs an increasingly important role in analog-to-digital conversion and front-end processing.

Driven by mobile devices, CIS sensors are rapidly developing customized technologies for other applications. A brief review of automotive (high dynamic range) and security sensors (infra-red) is provided.

II. PIXEL PITCH IN MOBILE DEVICES

Pixel scaling continues to trend down, with Samsung, Sony and OmniVision leading the push to smaller pitches. Consulting Fig. 1, showing the pixel pitch with time, the 0.6 µm generation entered the marketplace in 2021.

Samsung presented a 0.64 µm device with its JN1 sensor and OmniVision followed suit with the 0.61 µm OV60A. The first 0.56 µm sensor was identified in 2022; the Samsung 0.56 µm HPX [1] and OmniVision has announced a sensor at the same pitch, the OVB0A,to bereleased in 2023. Sony reduces pitch conservatively, announcing a 0.7 µm design in 2021 (IEDM 2021) analyzed in early 2023; the IMX758. Sensor resolution also trends to larger values and Fig. 2 shows the sensor resolution versus the pixel pitch for rear facing cameras.

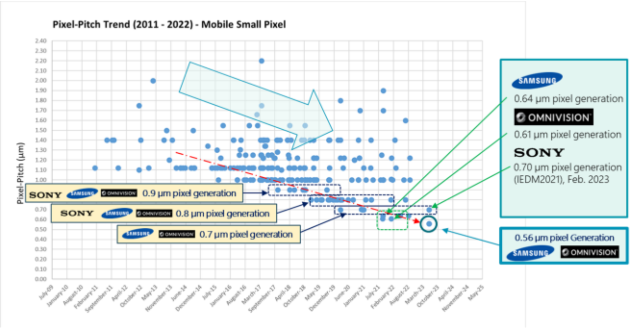


Fig. 1. Pixel pitch vs year of analysis, years 2021- March 2023.

Sensor resolution has been pushed by Samsung and OmniVision with 50 MP arrays followed by 64 MP, 108 MP and now 200 MP. Broadly speaking there are two strategies at play; high resolution/small pixel pitch devices and lower resolution devices with larger pixels. These two approaches maintain signal dynamic range and noise performance in different ways; the smaller pitches often use several pixels in parallel to collect low signal levels that are averaged or binned. The larger pixels use a high-quality analog signal path to resolve low light signal quality. In particular, Apple iPhones use a large pixel, lower resolution strategy with 12 MP sensors, only recently moving to 48 MP in the iPhone 14 generation.

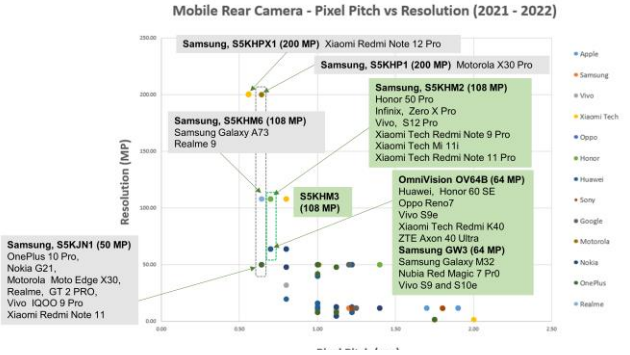


Fig. 2. Array resolution vs Pixel Pitch for back facing cameras.

III. PHASE DETECTION AUTOFOCUS AND COLOR FILTER ARRAYS

The pixel pitch has direct implications for both Phase Detection Auto Focus (PDAF) and the Color Filter Arrays (CFA). There are three basic strategies for PDAF; masked, dual-photodiode, and On Chip Lens (OCL). Manufacturers continue to use these approaches and occasionally combine them. Rapid focusing using different regions of the field requires PDAF pixels covering as much of the array as possible while not compromising the light collecting efficiency. This is a particular problem for masked PDAF where half the PDAF pixel is covered with metal. Fig. 3 shows

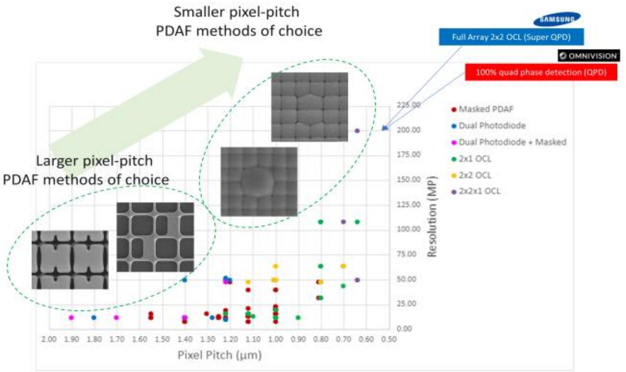


Fig. 3. PDAF pixels use On Chip Lenses as pixel pitch is reduced.

the PDAF strategy trending towards On Chip Lenses (OCL) as the pitch is reduced and the resolution increases.

Fig. 4 shows the trend in Color Filter Array Mosaics. As the pixel pitch decreases, the CFA pitch remains at approximately 2.4 µm. Current pixel pitches use 4 by 4 groupings of color filters, and the aperture grid is placed between each pixel using a buried color filter between the aperture metal.

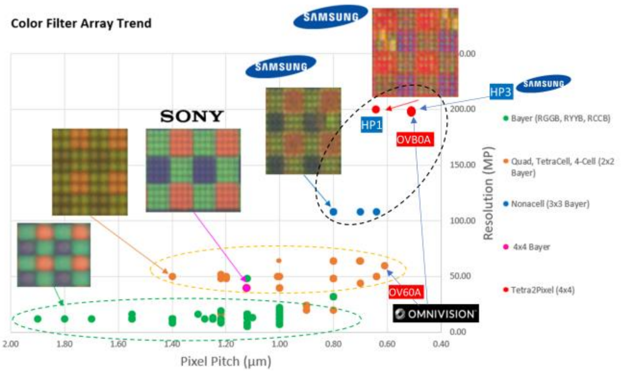


Fig. 4. Color Filter Arrays are grouped as pixel pitch decreases.

IV. DEEP TRENCH AND APERTURE GRID ISOLATION

Trench Isolation and Aperture Grids both serve the objective of pixel isolation. The aperture grid above the photodiode surface does this by ensuring light enters only the target photodiode under the aperture. The grid increases in height and complexity with smaller pitches, shown in Fig. 5.

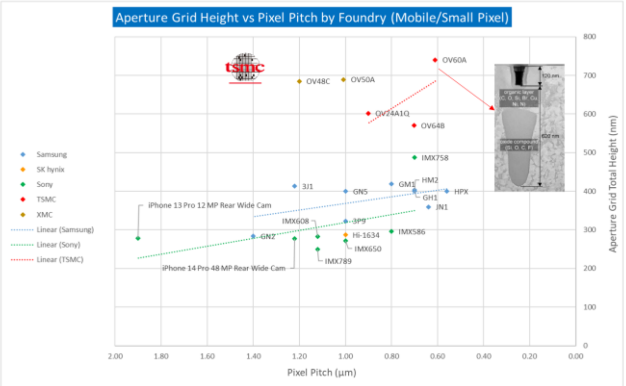
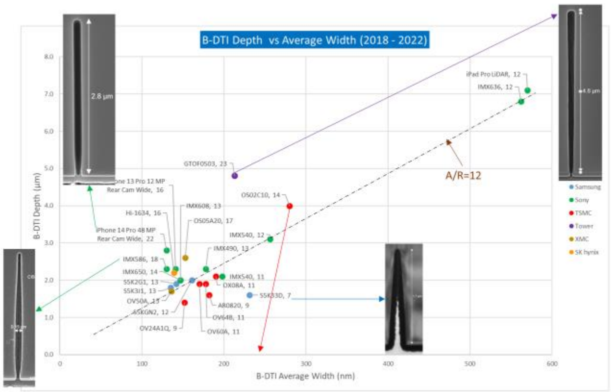


Fig. 5. Aperture grid height vs pixel pitch.

The grid increases quantum efficiency by reflecting high angle light back into the photodiode. The grid should be optically reflective to do this and also be electrically conductive to discharge optically generated residual electrons. Manufacturers have been shifting to composite grid structures as the pixel pitch is reduced and the height is now comparable to or exceeds the pixel pitch.

The trench between the photodiodes isolates each diode electrically and optically. As well, trench backfill material selection increases well capacity and reduces dark current noise. Samsung typically uses Front Trench Isolation for mobile pixels, while Sony and OmniVision (TSMC) use Back Deep Trench Isolation. Fig. 6 shows trench depth versus average trench width for different applications and foundries. Each data point is labelled by the device and aspect ratio of depth to width; most devices have and aspect ratio of approximately 12.



Images not to scale

Fig. 6. Back Deep Trench Depth vs Average Width.

Table 1 summarizes the representative layer trench material for recent small pixel sensors, typically a composite structure of high K oxides.

TABLE I. DEEP TRENCH ISOLATION LINER MATERIALS.

FOUNDRY/ DEVICE	XMC/ OV50A	TSMC/ OV60A	SONY/ IPHONE 14	HYNIX/ HI-1634	SAMSUNG/ JN1
DTI	B-DTI	B-DTI	B-DTI	B-DTI	F-DTI
Pixel Pitch (µm)	1.00	0.64	1.22	1.00	0.64
DTI Depth (µm)	1.7	1.9	2.8	2.2	3.8
Liner	AlOSi-TaoSi-SiO	AlO-HfO-TaO-SiO	AlO-TaO-SiO	AlO-Hf-SiO	N+ poly/Liner

V. TRANSFER FET AND SOURCE FOLLOWER

Once the photodiode has converted the input light to electric charge, the electric signal is transferred off the array with minimal noise. The two critical devices in this signal chain are the transfer gate and the sourcefollower. The transfer gate should shift all photodiode charge to a storage

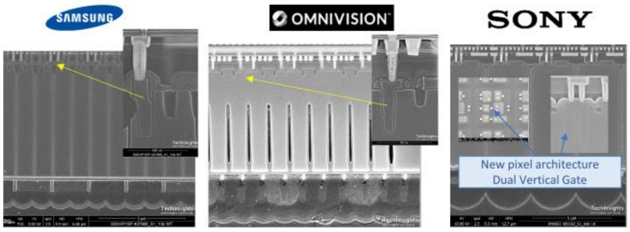


Fig. 7. Vertical Transfer Gates by Samsung, OmniVision and Sony.

node and at small pitches the preferred approach is a Vertical Transfer Gate. Fig. 7 shows the vertical transfer gates in recent small pixel pitch sensors. The Sony device (STARVIS-2 Security and Surveillance device, the IMX 662) uses a dual Vertical Transfer Gate to improve charge transfer. Samsung's most recent 200 MP sensor, the HP2 found in the Galaxy S23 Ultra, also uses a Dual Vertical Gate [2].

The source-follower drives the output column and a large transconductance (W/L) is desirable. As well, the transistor area has a direct impact on temporal noise, random telegraph noise, fixed pattern noise and pixel linearity. Increasing the area (WxL) can decrease these effects but also reduces the effective gain of the pixel. Several strategies are available to designers to optimize performance; thin silicon nitrides are increasingly common, and photodiodes are grouped and output through the same SourceFollower device. Transistors are often placed in parallel to increase transconductance and reduce noise. Fig. 8 shows the gate width to length ratio, which is maintained as pixel pitch is reduced to conserve the drive capacity.

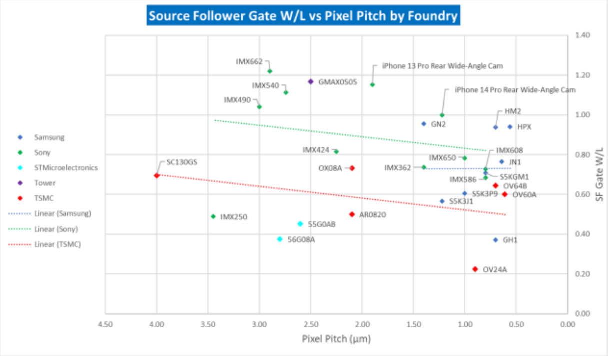


Fig. 8. Source-Follower Width to Length Ratio vs Pixel Pitch.

VI. DIRECT BONDING INTERFACE AND THE IMAGE SIGNAL PROCESSOR

Almost all mobile image sensors are now stacked with an Image Signal Processor (ISP), and the underlying ISP has served a mechanical function to support the thinned CIS. The ISP provides control signals to the array and receives analog outputs that are digitized; this is done through either a Direct (Hybrid) Bonding Interface (DBI) or Through Silicon Vias (TSV) for backside imagers. DBI pitch is decreasing with an objective to create pixel pitch hybrid bonds; this would allow pixel circuitry to be moved to the ISP. Currently, pixel hybrid bond pitches have been seen only in larger pixels; three Sony devices (iPad Pro 10 µm pitch LiDAR, the IMX990 SWIR sensor, and the IMX636 event-based sensor analyzed in 2022) and the current smallest in-pixel device, the OmniVision voltage domain global shutter (OG01A1B) with 2.2 um pitch. Fig. 9 shows the decreasing bonding pitch led by specialized sensors (Near Infra-Red, Time of Flight), the current smallest pitch seen is in the ams OSRAM Mira220 global shutter Near Infra-Red sensor. Sony has demonstrated a 1.0 µm DBI.

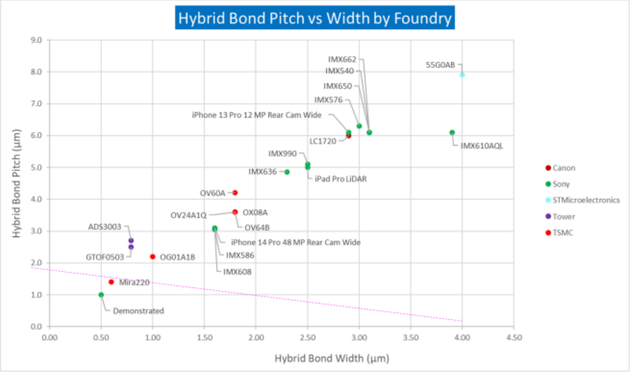


Fig. 9. Decreasing direct bond pitch vs width.

The ISP die controls the CIS array, converts the array output from analog to digital and performs front end digital processing. Fig. 10 shows the ISP for two major main (wide) smartphone cameras; the iPhone 14 Pro Max and the Samsung S23 Ultra. Note two features; the large area required to perform analog to digital conversion of the columns (approximately 35%) and also the sparse circuit density in the standard cell logic area . The latter suggests much more digital processing can be added in the future.

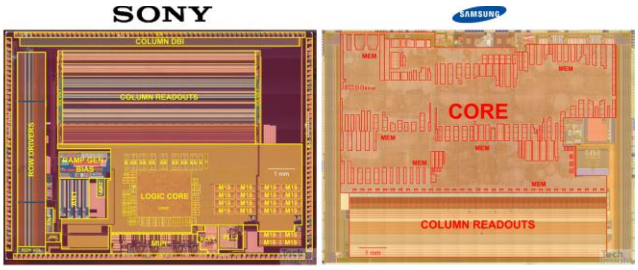


Fig. 10. Image Signal Processor floorplan, iPhone 14 (standard cell logic only in the "Logic Core" box) and Galaxy S23 (light brown regions of logic core are unused).

VII. AUTOMOTIVE, SECURITY

Until recently, automotive image sensors were off-the-shelf designs repurposed as automotive imagers but the major manufacturers are now custom designing sensors for this market. Specific requirements include flicker mitigation and

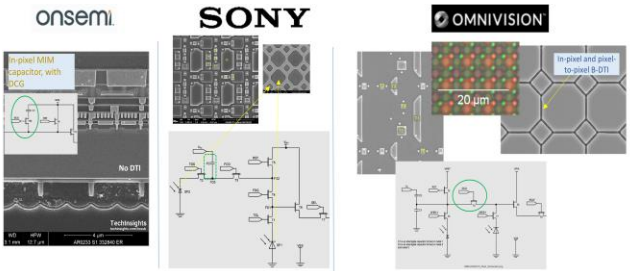


Fig. 11. High dynamic range pixel structures; onsemi, Sony, OmniVision.

high dynamic range. Gains of 120-140 dB are common, and several techniques are used including multiple exposure times and, as shown in Fig. 11 dual gain pixels (onsemi) and dual photodiode sizes (Sony and OmniVision).

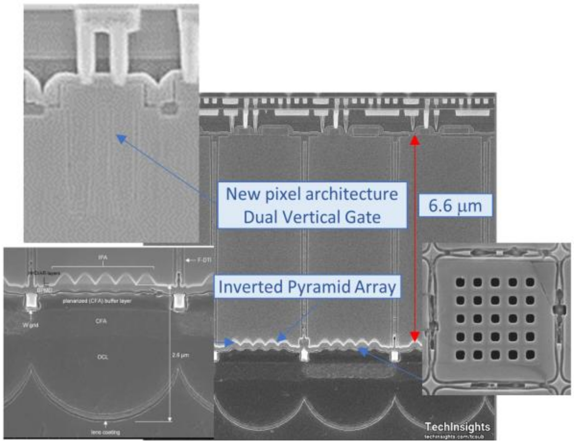


Fig. 12. Sony IMX662 STARVIS 2 Near Infra-Red Sensor

Security devices need high performance in the infra-red. The Sony STARVIS 2 IMX662 (Fig. 12) uses techniques common to other manufacturers including Inverted Pyramid Arrays [3] at the silicon surface, a 6.6 µm thick epi layer and Front trench isolation as well as a new dual vertical gate pixel architecture.

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