High Full Well Capacity and Low Noise Characteristics in 0.6 μm Pixels via Buried Sublocal Connections in a 2-Layer Transistor Pixel Stacked CMOS Image Sensor

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Abstract

Herein, we demonstrate the development of a 2-Layer Transistor Pixel stacked CMOS image sensor (CIS) that possesses a high full-well capacity (FWC) and low random noise (RN). A high FWC was achieved by increasing the photodiode (PD) volume by fabricating PDs and pixel transistors on different silicon (Si) layers in a 3D sequential integration process and introducing a single vertical gate (SVG). Buried sublocal connections (BSCs) that connect multiple floating diffusions (FD) and Pixel FinFETs were introduced to improve the conversion gain and random noise (RN). We have demonstrated a 2-Layer Pixel with a 0.6 μm pixel with an RN of 0.99, an FWC of 8000e-, and a dynamic-range of 78.1 dB.

Ⅰ. Introduction

Ensuring high dynamic range (D-range) for pixel shrinkage is important for image capture. Pixel shrinkage makes it difficult to ensure a high FWC owing to the inability to secure PD area and low noise because of the size reduction of the pixel transistors. A two-layer transistor pixel stacked CMOS image sensor (“2-Layer Pixel”) has been proposed as a promising technology for capturing images with low noise and high D-range and achieving Pixel shrinkage in CMOS image sensors. [1-2] Schematic diagrams of the 2-Layer Pixel are shown in Figs. 1 and 2.

The 2-Layer Pixel comprises an Si layer on which the PDs and transfer gates are arranged. the second layer contains t pixel transistors, such as amplifier transistors, select gates, reset gates, and deep contacts, to connect the PDs and pixel transistors. Additionally, full trench isolations (FTIs) are formed to separate the pixels. In a previous study, we developed a three-dimensional (3D) sequential integration process to realize the 2-Layer Pixel. [2]

This paper presents a 2-Layer Pixel with a 0.6 μm Pixel by introducing a single vertical transfer gate (SVG), buried sublocal connections (BSCs), and Pixel FinFETs.

Ⅱ. Improvement of FWC

The major performance requirements for PDs and transfer gate (TRG) are high FWC with no-lag and no-blooming. In this device, the PDs were completely separated by introducing full trench isolation (FTI) in the 1st Si Layer that formed the PDs, resulting in a structure with no-blooming. TRG optimization is performed only for no-lag and FWC, and the degree of freedom of the TRG design are improved compared with the case where FTI is not applied. The 2-Layer Pixel structure enlarges the TRG layout area as shown in Fig. 3(a-b). The introduction of SVG expands the area available for TRG placement because it causes a change in the PD configuration which eliminates the need for a shallow PD to achieve a high FWC and no-lag, as shown in Fig. 3(b-c). An FWC of 8000e- was achieved with the SVG by optimizing its geometry and placement.

Ⅲ. Improvement of RN

Reducing the FD capacitance is important for improving RN and conversion gain. BSCs were introduced to reduce the diffusion layer capacitance, and Pixel FinFETs was introduced to shrink the FD sharing unit.

In the conventional 2-Layer-Pixels, SCs are used to connect multiple floating diffusions. SCs are structures formed between 1st-Layer and 2nd-Layer, which contacts to the Si surface of the 1st layer and have ohmic conductivity. The BSCs are structures in which the contact area changes from the Si surface to the Si sidewall, as shown in Fig. 4(b). Compared with SCs, BSCs can be separated from TGs and the capacitance of TGs can be lowered. By optimizing the layout and depth of the BSCs, the FD capacitance was reduced by 46%, as shown in Fig. 5(a). The BSCs exhibited Ohmic conductivity, and the resistance is plotted in Fig. 5(b). To shrink the FD-sharing unit from 2x4 to 2x2, we adopted Pixel-FinFETs. Introducing BSCs and changing the FD sharing unit increased the conversion gain by 2.26 times and decreased the RN by 67%, as shown in Fig. 6(a)and(b).

V. Conclusions

We fabricated a 2-Layer Pixel with 0.6 μm Pixel, as shown in Fig. 7. Figure 8 shows the relationship between the pixel size and D-range, wherein the FWC and RN of PD CISs reported in previous studies [3-7] are compared with those obtained in this study. The performance parameters and comparison with prior studies are summarized in Table I.

Reference

[1] K. Nakazawa et al, IEDM, 2021
[2] K. Zaitsu et al, VLSI, 2022
[3] Y. Oh et al, IEDM, 2020
[4] H. Kim et al, ISSCC, 2020
[5] J. Park et al, ISSCC, 2021
[6] J. Yun et al, VLSI, 2022
[7] S. Park et al, ISSCC, 2022

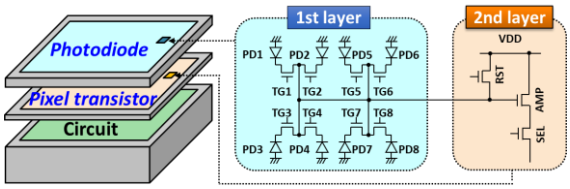

Fig. 1 Schematics of the 2-Layer Pixel based on a three-dimensional sequential integration process [1]

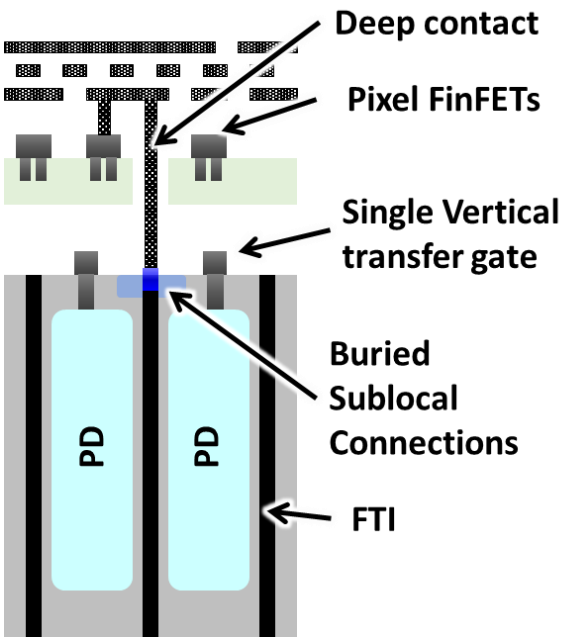

Fig. 2 Cross-sectional structure of the photodiode (PD) and pixel transistor.

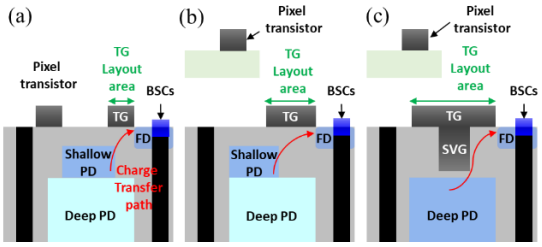

Fig. 3(a—c) Schematics of enlargement TG layout area by 2-Layer Pixel structure and the introduction of SVG

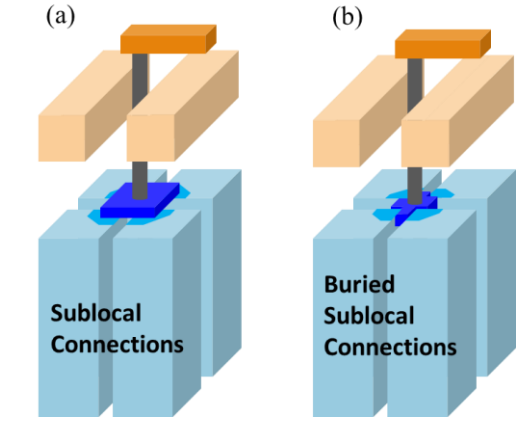

Fig. 4 Design optimization based on sublocal connections to connect multiple floating diffusions (FDs). (a, b) Schematics of device structures (a) with the sublocal connections [2] and (b) with the buried sublocal connections.

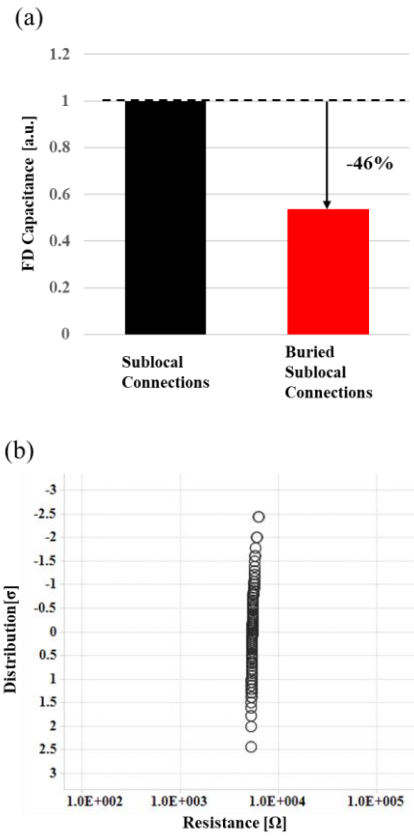

Fig. 5 (a) Comparison of FD Capacitance between the 2-Layer Pixels with the buried sublocal connections and the sublocal connections. (b) Resistance of the buried

sublocal connections.

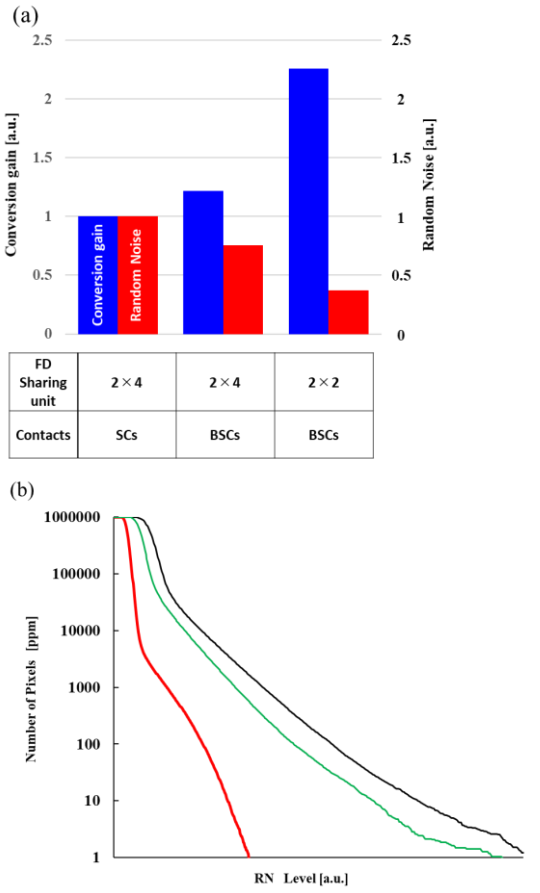

Fig. 5 (a) Comparison of conversion gain and random noise between FD sharing units and contacts. (b) Comparison of RN histogram between FD Sharing units and contacts.

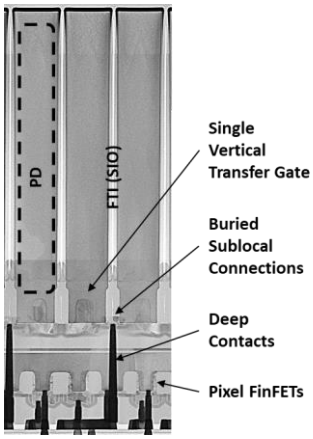

Fig. 6 Cross-sectional image of the 2-Layer Pixel with 0.6 µm PDs

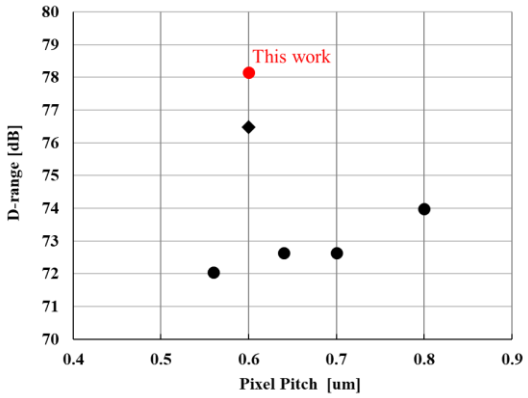

Fig. 7 Relationships between the pixel size and D-range in this work compared with those in previous studies. [3-7] D-range=20*log10(FWC/RN)

Table. 1 Performance comparison table

	unit	This work	Ref[7]	Ref[6]
Pixel Pitch	µm	0.6	0.6	0.56
Transfer Gate	-	Single VTG	Dual VTG	Single VTG
FD unit	-	2×2	-	-
FWC	e-	8000	10000	6000
RN	e-	0.99	1.5	1.5
D-range	dB	78.1	76.5	72.1
lag	e-	<1	-	-
RTS@10ppm	erms	<6	-	-