# World smallest 200Mp CMOS Image Sensor with 0.56µm pixel equipped with novel Deep Trench Isolation structure for better sensitivity and higher CG

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***Abstract*—** We present the world smallest 200 megapixel (MP) CMOS Image Sensor equipped with newly developed 0.56µm pixel. Apart from the conventional full-depth deep trench isolation (FDTI), our 2x4 shared pixel structure incorporated novel DTI structure to minimize the light absorption from polysilicon which is used to fill DTI and suppress dark current when biased. With new DTI structure, the relative QE is improved by 14%. Furthermore we were able to control the potential barrier between 4 pixels that share new DTI structure to improve the image quality in summation mode. The new structure also increased conversion gain (CG) by 38% and further process optimization resulted in additional 14%improvement.

## I. INTRODUCTION

Over the past decade, we have witnessed tremendous development in CMOS image sensor (CIS) technology for better image quality. For CIS for mobile phones, in particular, we are able to see two major directions for development of pixels.

One of the major direction was developing smaller submicron pixels with the aim of achieving higher resolution by capturing more details of the object [1-2]. With the help of new technologies such as full-depth deep trench isolation (FDTI) and vertical transfer gate (VTG), the pixel pitch has shrunk continuously from over 1.0 um up to 0.56µm in just few years [3-8] and the resolution has reached up to 200MP [7]. This trend has garnered a favorable response from the CIS market and most of the flagship mobile phones are now equipped with CIS with 50MP~200Mp. However it is very difficult to avoid the physical limit of smaller size of pixels in very low light conditions and the image quality deteriorates as soon as the light gets too dim. A simple solution is to combining the signals from several neighboring pixels together. This leads to the development of prevalent 2x2 color filter (CF) patterns and underlying pixel circuitry as well as various image signal processing algorithms. Recently we observed 4x4 CF patterns where 16 pixels are merged.

Another direction of major CIS development is the auto-focus (AF) technology. Since the emergence of phase detection AF, fast AF system became the indispensable feature even in mobile phones. The accuracy and speed of AF heavily rely on the density of the PDAF pixels. Therefore two types of major technologies, which are dual PD (2PD) [9-10] and Quad cell (i.e. Qcell) [11, 7], have been developed to utilize all the pixel as AF pixel. While each technology has its own pros and cons, both of them offer essentially 100% AF pixels and are able to bring a superior AF user experience.

In this paper, we introduce a new CIS in order to meet the all aspects of the previous demands. The pixel based on a recently developed 0.56um pixel employed a unique DTI structure which enables us to maintain the superior AF performance and minimize the QE loss simultaneously. The physical structure also enables us to keep the photo electrons from overflowing to FD and maintain the linearity at binning mode. In addition, the structure helped us to increase the conversion gain (CG) of the system to reduce the readout noise to achieve high image quality.

## II. PIXEL TECHNOLOGY

Our sensor, a world smallest 200MP CIS, is built with a recently developed 0.56um pixel with 2x4 shared structure where we employed 32nm BEOL process for pixels. Due to the world smallest 0.56um pixel, we are able to shrink the chip size by 22% compared to the previous generation of 200MP CIS with 0.64um pixel from our company. The resolution is 16320 x 12288 with optical format of 1/1.4".

0.56um pixel presented in ref. [8] with conventional technology, however, contains several limitations. While a conventional FDTI structure offers great performances such as higher FWC and low optical crosstalk, it is not suitable for Qcell technology. As shown in Fig. [1] and Fig. [2], Qcell with FDTI structure has single microlens over 4 pixels and an incident light focuses on the intersection of FDTI filled with polysilicon which is chosen to reduce dark current from the wall of FDTI. Therefore it is difficult to avoid the quantum efficiency (QE) loss from photon absorption by polysilicon. Another disadvantage of having FDTI structure for Qcell is that the physical separation of FDTI prevents from excess electrons to migrate between microlens-shared pixels before overflowing to FD as in dual PD pixels. This results in the output non-linearity of charge summation of binning mode. Finally, it is not convenient to extract a high conversion gain in conventional FDTI structure since the FD junctions are isolated from each other. Typically one needs complicated metal layout with longer metal lines and a number of contacts as well as increased junction capacitance which result in lower conversion gain.

Therefore we devised new FDTI structure with DTI center cut (DCC) in order to overcome the challenges we mentioned above as shown in Fig. [3]. As soon as we remove the DTI from the center of 4 pixels and connect them from each other, we are able to tackle several problems simultaneously.

Fig. [4] shows that the TCAD simulation of optical intensity between conventional No-DCC structure and DCC structure. We can see that DCC structure not only prevents optical loss at the center of 4 pixels but also scattering from DTI is reduced. Still the optical cross talk cannot be avoided. In Fig. [5], the schematic diagram of inter-pixel overflow (IPO) structure is presented. By controlling the size of DCC and n-type doping concentration for photodiode carefully, we are able to control IPO potential. Fig. [6] shows the TCAD simulation of potential profile of photodiode and IPO potential. We can see that IPO arises in the deep photodiode region. In addition we designed the location of floating diffusion (FD) to be at the center of DCC. Fig. [7] shows the schematics of pixel layout between No-DCC structure and DCC structure. By merging FD, we are able to reduce the number of FD junctions and contacts on FD by a quarter with shorter FD metal connection. Since FD is located at the center of DCC, the doping and potential profiles should be managed carefully to prevent second IPO path due to FD implantation while enhancing the charge transfer to FD.

## III. Results and Discussion

First, we can improve QE significantly over Qcell with conventional DTI structure by minimizing optical loss from polysilicon where light is most focused. Fig. [8] shows the comparison of normailzed QE spectrum between No-DCC and DCC structure. We are able to observe increase of QE by 14% from DCC structure. In Fig. [9] the change of sensitivity relative to DCC size shows 0.6% per 10nm. Because of the DTI removal, optical crosstalk is expected to increase slightly between pixels under the same microlens as we can see from TCAD simulation. However, these pixels share the same color filter, therefore, the crosstalk does not impact the performance when operated in binning mode where signals are summed for low light conditions. In high resolution scenes where each pixels are operated separately, the major cause of signal difference between these pixels are from the misalignment of microlens rather than the crosstalk between pixels and is compensated by proper ISP algorithm.

Second, the IPO level change according to DCC size is shown in Fig. [10]. As one can imagine, IPO level is sensitive to the change of DCC size since p-type doping provided by PLAD along the DTI wall and n-type doping by photodiode decides the IPO level.

Finally, the conversion gain is compared between No-DCC and DCC structure. As shown in Fig. [11], DCC structure has conversion gain increased by 38%. After analyzing data we figured that the reduction of both junction capacitance and metallic capacitance contributes similarly. We also was able to optimize the process for our sensor which gives us additional 14% of CG increase. Eventually conversion gain of our sensor become comparable to the reference product even though adopting 2x4 shared structure compared to 2x2 shared structure of reference.

The overall performance of our sensor is summarized in Table 1.

## IV. Conclusion

In summary, we have developed a 200Mp CIS with 0.56um pixel. The new CIS incorporated a new DTI structure, which enables Qcell technology with better overall performance. While main sensor properties are comparable to the previous generation, the new Qcell technology with DCC structure enables us to improve AF performance and random noise for extremely low light conditions. We will continue to search for the sub-micron-pixel mobile CIS technology based our new sensor.


## Acknowledgement

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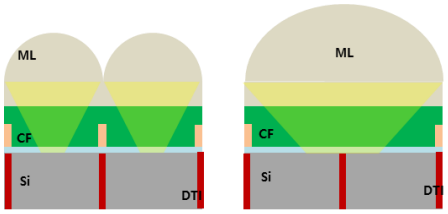



(a) (b)

Figure 1. A schematic diagram of (a) Tetra and (b) Qcell structures.

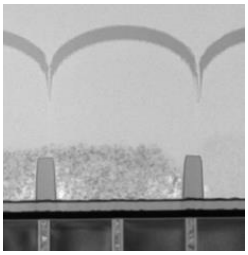
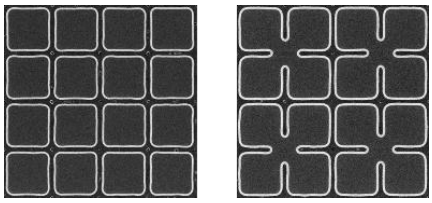


Figure 2. VSEM image of optical stack and DTI.



(a) (b)

Figure 3. (a) A cross section of conventional FDTI structure (b) new FDTI with DCC structure.

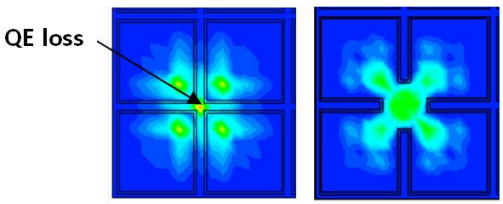



Figure 4. TCAD simulation of conventional FDTI and DCC structure.

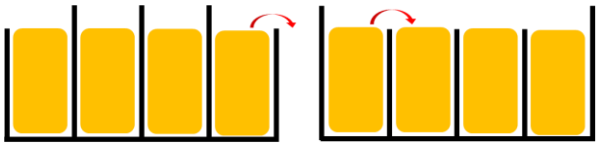


Figure 5. Schematic diagram of Non-IPO (Left) and IPO (Right) potential structure

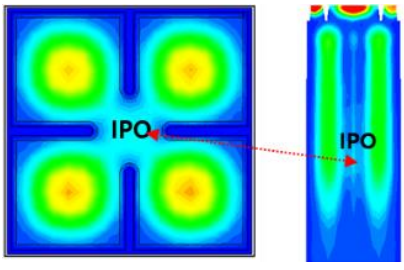
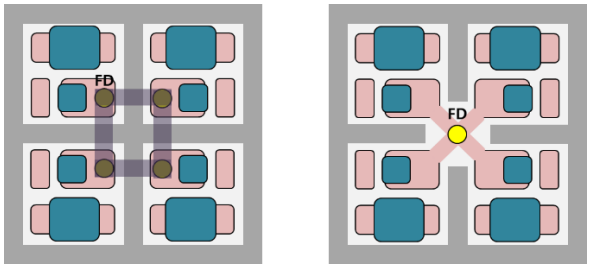



Figure 6. TCAD simulation of photodiode and IPO potential




(a) (b)

Figure 7. Schematic pixel structure (a) with no DCC and (b) with DCC.

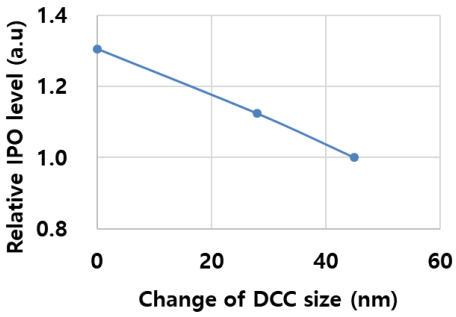



Figure 10. IPO level change according to DCC size

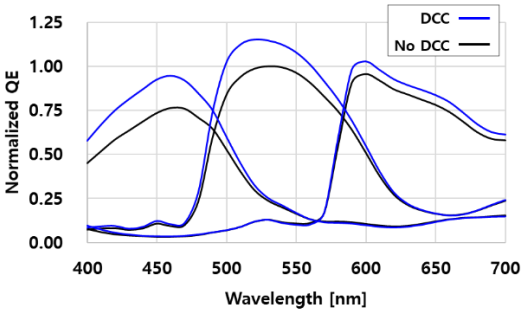



Figure 8. Normalized QE comparison between DCC (blue) and no DCC (black).

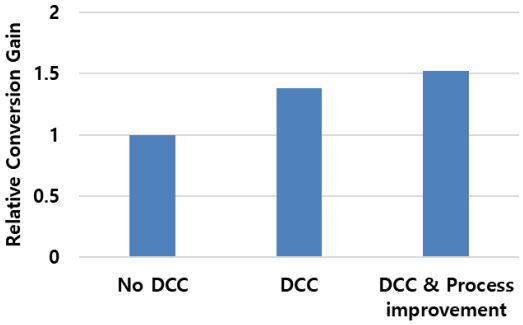



Figure 11. Comparison of conversion gain between No DCC and DCC.

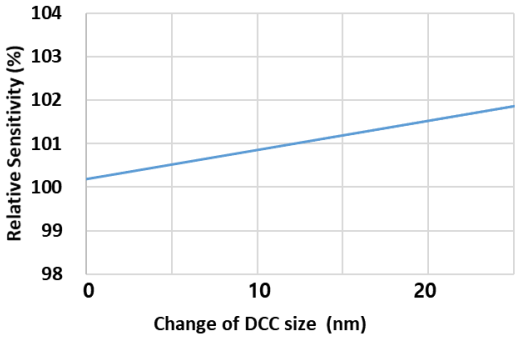



Figure 9. Change of Sensitivity relative to DCC size.

| Items | Unit | Reference | This work |
|---|---|---|---|
| Pixel pitch | um | 0.64 | 0.56 |
| Linear FWC (1Pixel) | e- | 6000 | 4700 |
| Linear FWC (Binning) | e- | 96000 | 75000 |
| RN (multiple sampling on/off) | e- | 2.2/3.4 | 1.6/2.3 |
| RTS | ppm | 4 | 1 |
| Sensitivity / area | e-/lux.s/um$^2$ | 3784 | 3746 |
| YSNR [20lux] | dB | 30.7 | 29.9 |

Table 1. Summary of performance