0.56µm-pitch CMOS image sensor for high resolution application

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***Abstract*—In this paper we describe a 200Mpixel CMOS image sensor with 0.56µm pixels implemented in a 28nm process. This pixel technology is the next generation development after our 0.61µm pixel. The sensor demonstrates a full well capacity of 5.5ke- with lower dark current and read noise than our previous generation pixel. In addition, this sensor demonstrates similar quantum efficiency (QE) and phase detection autofocus (PDAF) performance in comparison to our previous generation pixels. This sensor also implements multiple functions including switched conversion gain and high-speed readout.**

Keywords—CMOS image sensor, 0.56 µm pixel, small pixel, 200Mp

I. INTRODUCTION

In the field of CMOS image sensors (CIS), pixel miniaturization drives product innovation. The pursuit of continuously shrinking pixel sizes, while maintaining performance, forms the foundation of CIS development in recent history. Demand for high-resolution mobile image sensors have escalated, with mobile CIS product resolutions increasing from 24Mp to 200Mp in under 5 years. Despite attaining pixel pitch scaling below the wavelength of visible light, better image quality is consistently achieved due to progressive improvements in image signal processing [1]. While pixel downscaling offers higher pixel counts in smaller form factors, there is a trade-off between pixel miniaturization and overall performance, as the reduction of light-receiving areas contributes to CIS performance degradation [2].

High-resolution image sensors are almost exclusively realized using wafer stacking, in which pixel and read-out circuitry are separated onto independent wafers. Additionally, high-resolution pixel read-out requires more select-lines for control, which increases capacitance, causing lower read-out rates. Dual-Row selection enables fast pixel binning without increasing the number of bit-lines, achieving fast read-out without additional circuitry.

Small-pixel image sensors suffer often from lower full well capacity (FWC). Therefore strong isolation potential barriers are required to mitigate this problem. In this paper, we present a 0.56µm pixel, 200MP stacked CMOS image sensor, developed using a new, CIS-dedicated 28nm process. Shrinking the process node frees up chip space, providing room for additional devices and functions, such as switchable conversion gain (SCG) and circuitry for low noise and high speed readout.

The 0.56um pixel developed in this work achieved high FWC without sacrificing dark performance. Compared to its 0.61µm predecessor, a higher FWC is obtained without image lag or blooming, while dark current and white pixels (WP) remain comparable. This device is capable of pixel binning mode with switchable conversion gain, which provides high dynamic range and FWC to produce higher image quality. Shared floating diffusion (FD) is utilized for 16C binning mode to lower read noise.

II. PIXEL ARCHITECTURE AND TECHNOLOGY

A. Pixel Stacking Process technology

The 0.56µm pixel development discussed in this work adopts a new, CIS-dedicated 28nm process node for the pixel wafer, instead of the 45nm process node employed in previous generation devices. The logic wafer follows the 40nm process node used in our previous small pixel stacking sensors [3,4]. Compared with the 0.61µm pixel design, the 0.56µm-pitch device benefits from increased design flexibility, enabled by the CIS-dedicated 28nm process node. Due to the chip space conserved by the 28nm node, the device implements an additional row select transistor to achieve fast readout. Additional layout strategies are applied for improved noise performance and higher FWC. Figure 1 shows the pixel transistor layout comparison between 0.61µm [Figure 1a] and the 0.56µm [Figure 1b] used in this work. Each transistor is isolated by shallow trench isolation (STI), while each pixel is separated by an improved backside deep trench isolation (BDTI), minimizing leakage and optical cross-talk, respectively [3]. By adopting CIS-dedicated 28nm process node, each group of pixels implements parallel-connected SFs to increase SF width, which works together with the 2-Row Select transistors design to maximize readout in the large, 200MP device. Without such strategies, such a large device may suffer from slow readout; A vertical transfer gate (VTG) architecture is implemented to shift the photodiode deeper into the silicon region, 28nm pixel process provides more flexibility for the design and placement of transistors in the limited space of the 0.56µm-pitch pixel [3,4,5]. This also enables the placement of an additional transistor within the pixel to support switchable conversion gain for high-dynamic applications.

B. Pixel architecture

The pixel array size is 200 mega-pixels (16384(H) x 12288(V)), with an optical format of 1/1.395" and a pixel pitch of 0.56µm. A 2x4 shared pixel architecture is utilized, as shown in the circuit schematic in Figure 2a. A new 2-Row Select transistor design is implemented, in which each 2x4 shared pixel is independently controlled by separate control signals, RS0 and RS1. In full-size or 4-cell mode, RS0 is

active for both left and right shared pixels, and their signals at FD are separately and concurrently readout through two separate bit-lines. In 16C mode, RS1 is active for both left and right shared pixels, with the RS1 of both shared pixels connected to the same bit-line. The RS1 of alternating rows connect to separate bit-lines (labeled as "A" and "B"-cells in Figure 2b), keeping the same loading for both bit-lines. This alternating bit-line control scheme reads out two 16-cell binned signals through the two-bit lines and two column ADCs. This enables 16 cell-binning mode for 0.56µm device achieves faster readout speed without increasing the number of bit-lines. Table I shows a comparison of the 0.61µm and 0.56µm device architectures.

C. QPD and Color filter pattern

Due to smaller on-chip lens (OCL) fill factor, small pitch pixels suffer from significant QE degradation. The QPD, or Quad-Bayer coding with 2x2 OCL, is a design that uses one OCL and the same color filter in a 2x2-pixel array, producing high-resolution and high dynamic range image sensors [6]. The QPD is an important technology to improve QE for small pixel image sensors and was implemented in this work [Figure 3].

III. EXPERIMENTAL RESULT

Figure 4 shows the FWC trend with respect to pixel pitch. The dotted line represents the FWC achieved by simple pixel area scaling, based on a 1.0µm pixel. The empty circles show data from our previous generation 0.7µm and 0.61µm technologies. The actual FWC demonstrated by the 0.7µm, 0.61µm, and 0.56um devices are much higher than the value predicted by simple scaling. This FWC enhancement was achieved by deep photodiode technology, in which the photodiode potential is situated in the deeper silicon region. Through adopting this technology, the 0.56µm device achieved 5.5ke- FWC without lag or blooming. Although we increased the n-type/p-type ion-implantation dose, creating higher electric fields, our improved BDTI technology mitigates the impact of surface defects, achieving dark current and WPs comparable to the previous generation. Table II shows the performance comparison between the 0.61µm- and 0.56µm-pitch devices; the 0.56µm-pitch pixel shows better performance than the 0.61µm-pitch device in all aspects, including very low noise level and phase detection auto focus (PDAF) performance.

Figure 5 presents the optical performance results, which shows the 0.56µm-pitch pixel's QE and cross-talk improves from the 0.61um-pitch reference pixel, while the image quality remains consistent. Figure 6 shows a sample color image taken with the 0.56um pixel in 4-cell mode.

IV. CONCLUSION

In this work, we developed a new 28/40nm 200 mega-pixel stacked image sensor with 0.56µm pixel pitch. This device achieved a FWC of 5.5ke- without image lag or blooming, and with dark performance comparable to the previous generation 0.61µm-pitch device. We demonstrated better QPD QE performance than the 0.61µm in the visible light range. A Dual-Row Select layout is employed to improve readout speed without adding circuitry (bit-lines), resulting in an increased frame rate compared to previous generation devices. A switchable conversion gain is enabled, such that the 0.56µm device reaches a 16C2 FWC 2x higher than the previous 0.61µm device.

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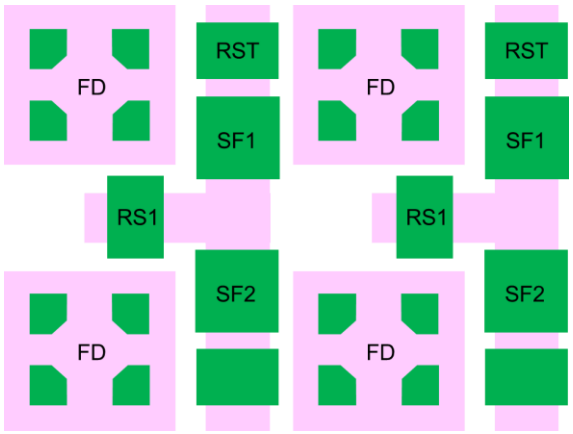

Figure 1a: 0.61um pitch pixel architecture

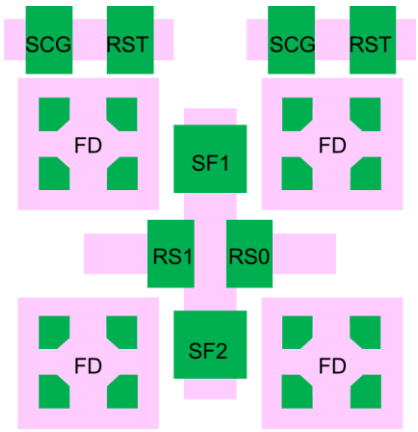

Figure 1b: 0.56um pitch pixel architecture

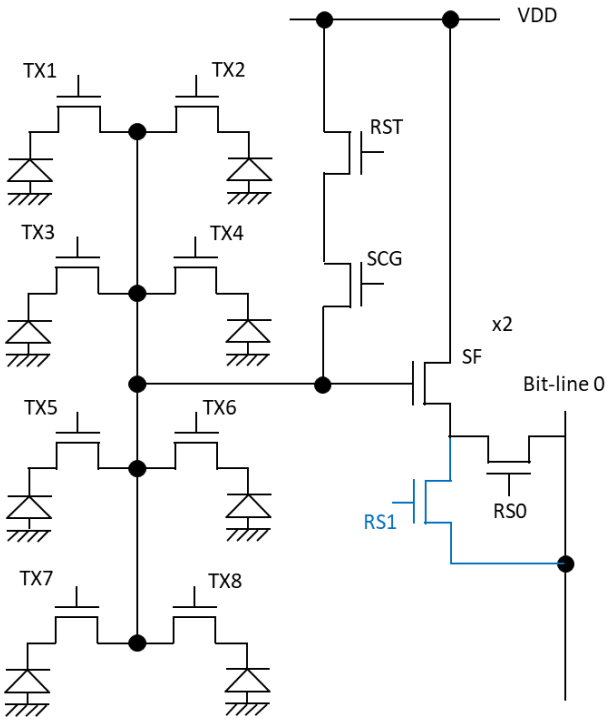

Figure 2a: Circuit schematic of the 0.56µm pixel.

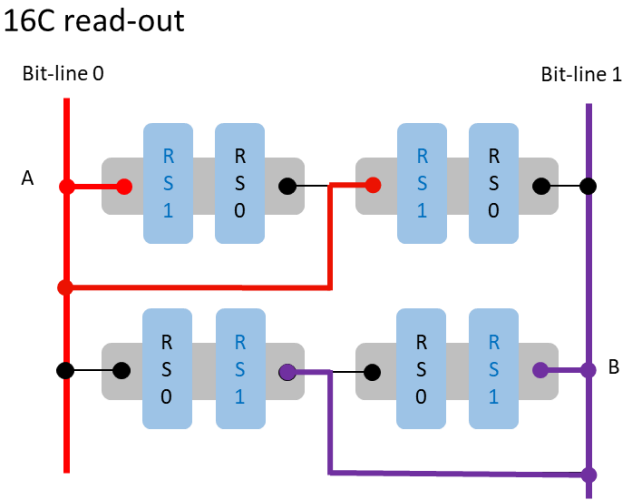

Figure 2b: 2-Row Select readout sequence on 16C mode

Table I: 0.61µm v.s 0.56µm architecture comparison

Pixel size	0.61um	0.56um
Resolution	200M/50M/12.5M	200M/50M/12.5M
Frame rate	8/24/90	8/30/120
Pixel Tech.	45nm	28nm
ASIC Tech.	40nm	40nm
Readout speed	1RS	2RS
Noise/RTS	2SF	2SF
Multi CG switch	No	Yes

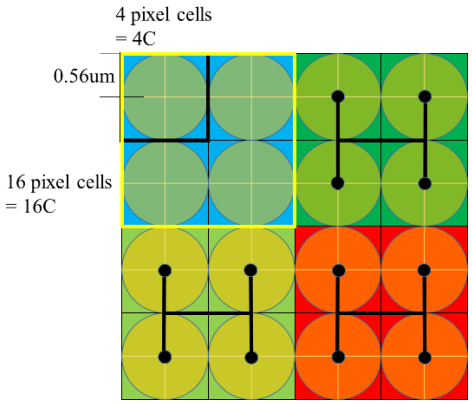

Figure 3: Schematic of color and cells definition

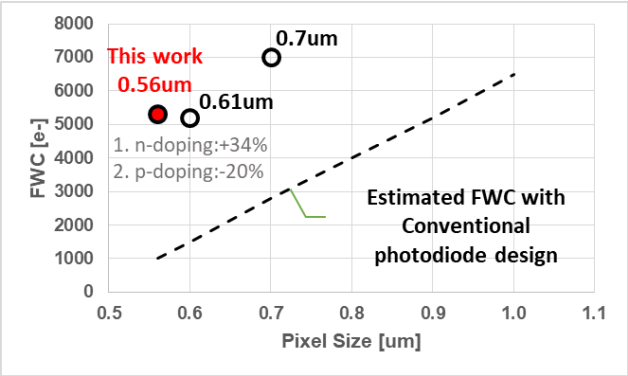

Figure 4: FWC trend with respect to pixel pitch

Table II: Performance comparison 0.61µm v.s 0.56 µm

		Unit	0.61um	0.56um
Full-well	1 pixel	e-	5.3K	5.5K
	16C binning	e-	49K	72K
Lag		e-	<1	<1
Blooming		%	<1	<1
DC		e-	18.6	17.6
Read Noise	1x Gain	e-	23.6	20.2
	16x Gain	e-	4.5	4.1
	64x Gain	e-	NA	1.6**
DR	1x Gain	[dB]	64.4	71
PDAF	Selectivity	ratio (Normalized)	1	1.05

** Low Noise mode

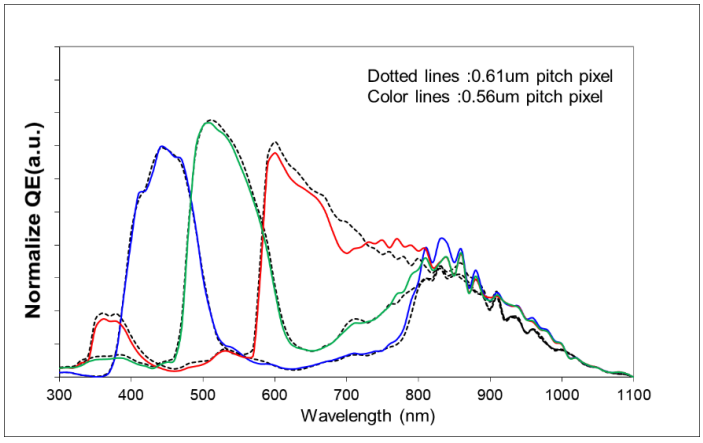

Figure 5: QE curve comparison

Figure 6: Picture demonstration of 12.5M pixels