0.64 µm 200 MP Stacked CIS with Switchable Pixel Resolution

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***Abstract*—This paper presents a 0.64 µm 200 MP stacked CMOS Image Sensor (CIS) in 65/28 nm process. The implemented sensor provides 200 MP, 50 MP, and 12.5 MP with switching pixel resolution through optimized readout scheme and remosaic algorithm based on same color filter in 4 x 4 pixels. During dark conditions, the 2.56 µm 12.5 MP resolution maximizes the pixel sensitivity whereas the 0.64 µm 200 MP resolution provides the most detailed image during bright conditions. Additionally, grid pattern and flatness of color filter material help to improve the pixel sensitivity by 8% with 0.64 um pixel. Especially, the 16,384 ADCs operate simultaneously to convert pixel outputs to Image Signal Process (ISP) chain and the sensor provides fast videos for both 4K 120 frame per second (fps) and 8K 30 fps through 3-lane CPHY 4 Gsps/lane. The measured random noise of the implemented chip is 2.4e- at analog gain of x16. The proposed 200 MP stacked CIS provides support for lossless zoom, adaptive region of interest, and switchable resolution for better User eXperience (UX).**

Keywords—CMOS Image Sensor (CIS), 200 MP CIS, switchable pixel resolution.

I. INTRODUCTION

In the last twenty years, the CMOS Image Sensor (CIS) in mobile applications has been developed by using VGA up to 200MP. Moreover, the pixel size has decreased by 1/1000 times from 5.6 um to 0.56 µm. Fig. 1 illustrates the pixel resolution trend of Samsung CIS products for smartphones used in the previous decade. Since 2015, tetra pixel (2 x 2 pattern) [1] has been adapted by 16 MP, 24 MP, and 48 MP. After that, the nona pixel (3 x 3 pattern) [2] is matched with 108 MP and the tetra square pixel (4 x 4 pattern) is a proper pixel arrangement for 200 MP. Each pattern has same colors such as blue, red, and green. Samsung has achieved the world's first mass production of 0.64 µm 200 MP sensor. The pixel pitch is successfully reduced to implement 0.6 µm and 0.56 µm with 200 MP.

The proposed 200 MP sensor has the following three advantages:

- Switchable pixel resolution helps to provide various camera modes such as still image of 12.5 MP, 50 MP, and 200 MP or 4K and 8K videos. Especially, this sensor can provide the detailed image with 200 MP and the bright image with 12.5 MP.
- Tetra square pixel is easy to enhance sensitivity as changing from sixteen 0.64-µm pixel into one 2.56-µm pixel with re-mosaic algorithms. Additionally, the sensitivity is improved by 8% after changing grid structure and optimizing color filter material.
- There is no loss in image quality when zoom in by x2 and x 4 or cropping any region of interest because digital zoom is not applied.

This paper describes the implementation of 65/28nm stacked CIS which consists of 0.64 µm tetra square 200 MP on the top chip and logics on the bottom chip. The measured Random Noise (RN) is 2.4e- with multiple sampling at 16x analog gain.

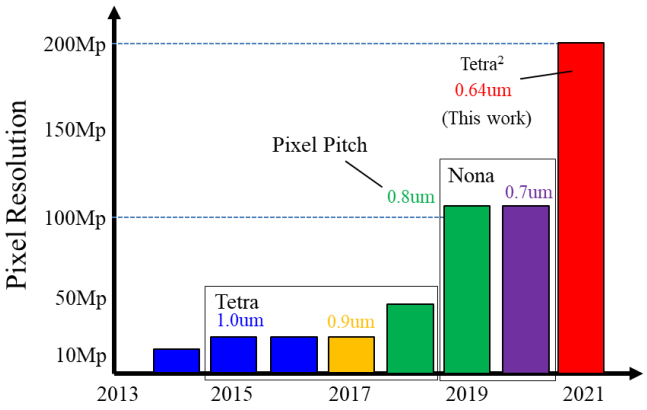


Fig. 1. CIS Pixel Resoultion and Pitch Trend with Pixel type

II. PROPOSED SENSOR ARCHITECTURE

Fig. 2 illustrates a block diagram of the implemented CIS that consists of a top chip for pixel array and a bottom chip for logic circuits throughout Through Silicon Via (TSV).

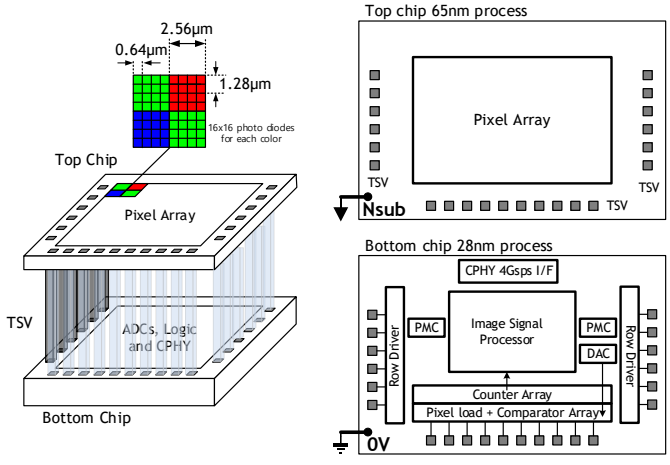
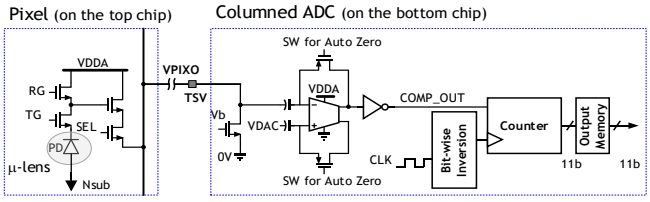


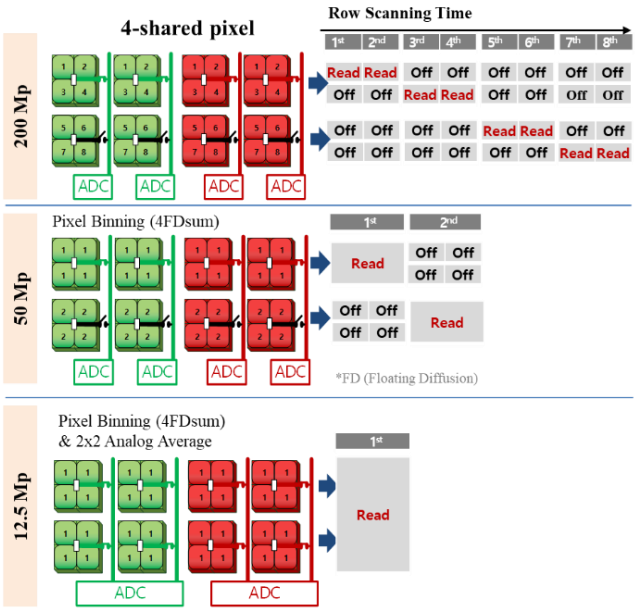
Fig. 2. Architecture of Proposed Stacked Sensor

The top chip consists of 16,384 x 12,288 pixels with -0.6V Negative voltage Substrate (Nsub) to reduced power consumption. The output signal from pixels on the top chip is transferred to the input of 16,384 comparators on the bottom chip. Each comparator is operated as a single-slope Analog-to-Digital Converter (ADC). To enhance noise and shading, two row drivers and Power Management Circuits (PMCs) are adapted. An Image Signal Processor (ISP) and three lanes CPHY serial interface circuit with 4Gsps/lane are implemented for various functions and camera modes.

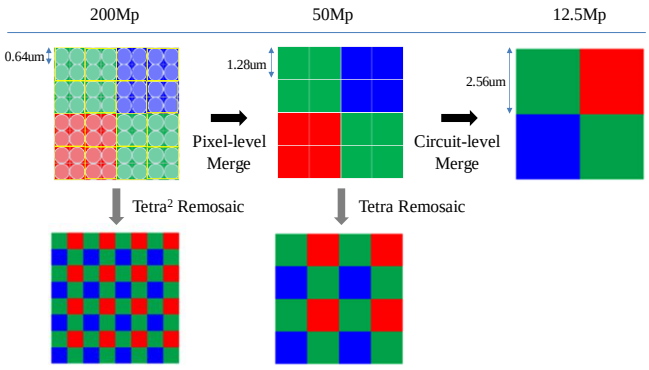
Fig. 3(a) illustrates the signal chain for readout of Photo-Diode (PD) under one micro-lens. After PD exposure period, the SEL transistor is turned on for PD readout. During initial reset of the ADC, auto-zeroing scheme is adapted to cancel reset noise of pixel and column Fixed Pattern Noise (FPN). Then, a reset code is inverted by Bit-Wise Inversion (BWI) for digital Correlated Double Sampling (CDS) operation in the counter. After TG is turned on, the differential value between the signal and the previous offset during ADC reset period is used to convert the signal from PD and transfer it to counter output memory. Fig. 3(b) illustrates the readout scheme of 200 MP, 50 MP, and 12.5 MP modes. During rolling the scanning sequence, all pixels from 4-shared pixel are separately transferred by the SEL transistor for 200 MP, four merged photodiodes on Floating Diffusion (FD) are summed up for 50 MP, and additional analog average scheme with four FD summation is applied for 12.5 MP. Fig. 3(c) illustrates how to obtain Bayer color pattern from each resolution with switchable pixel resolution.



(a) Column of Schematic



(b) Readout Details



(c) Bayer Pattern for Modes

Fig. 3. Mode Change Scheme for 200 MP, 50 MP, and 12 MP

III. Evaluation Results

Table I summarizes the specifications of the designed sensor. This sensor was fabricated with a 65nm NMOS process with 5-metal layers for the top chip and a 28nm CMOS process with 8-metal layers for the bottom chip. The pixel array consists of 200 M (16,388 × 12,288) pixels with 0.64-µm pixel pitch. The output of 200 MP provides eight frame per second (fps) with full well capacity of 6,000e-. With tetra readout, 50 MP reaches 30 fps with full well capacity of 24,000e- and 12.5 MP reaches 60 fps with full well capacity of 96,000e- with tetra square. The power supply of 2.2V, 1.8V and 1.0V are used for pixel/analog circuits, PLL/DPHY/IO, and digital circuits, respectively. RN is 2.2e- with multiple sampling at analog gain of x16 while it is 3.4e- without multiple sampling. In this paper, there is no information provided for staggered High Dynamic Range (HDR) and iDCG (intra-scene dual conversion gain) HDR even though HDR features are embedded for mass production.

TABLE I. Specification

Parameter	Value
Process technology	Pixel: 65nm 1P5M Logic: 28nm 1P8M
Number of effective pixels	16,384 (H) x 12,288 (V)
Pixel size	0.64µm
Maximum frame rate	8fps for 200MP 30fps for 50MP 60fps for 12.5MP
Supply voltage	Pixel/Analog circuit: 2.2V (PD GND -0.6V) PLL/CPHY/IO 1.8V Logic: 1.0V
Full well capacity	6,000e- @ 200MP 24,000e- @50MP 96,000e- @12.5MP
Random noise	3.4e- w/o multiple sampling @ analog gain x16 2.2e- w/ multiple sampling @ analog gain x16

There were several design challenges that we faced during the implementation of 0.64 µm 200 MP sensor.

- First of all, the power consumption is crucial. To reduce the power consumption, 200 MP tetra square remosaic is implemented by S/W in Application Processor (AP) instead of embedded H/W in the sensor. Therefore, the image processing speed is limited by channel lag. Note that the remosaic algorithm complexity has increased due to the image quality enhancement technique.

- Secondly, the pixel and analog circuit co-simulation is hardly performed. For example, dark shading simulation takes longer time even though the full resolution is not included. Thus, the proper results with 200 MP cannot be obtained because of nodal complexity of current simulation environment. In coming days, the model hardware correlation will be improved by trying different methods.

- Last, the designed columned comparator layout is very narrow inside 0.64 µm column pitch. Therefore, the comparator is more sensitive not only to avoid crosstalk by shielding metals but also to balance parasitic capacitance in each comparator by routing freedom limit.

In day light, resolution of 200 MP provides the more detailed image. Fig. 4 presents the results of zoom mode between 200 MP and 50 MP. The pixel can maintain the same image quality when the region of interest is changed when in zoom mode at 200 MP. Fig. 5 shows the experimental result of the implemented 200 MP chip with evaluation board and SLR lens. The printed image size is 28m x 22m and it maintains the proper image quality. Therefore, it provides a clear and proper image.

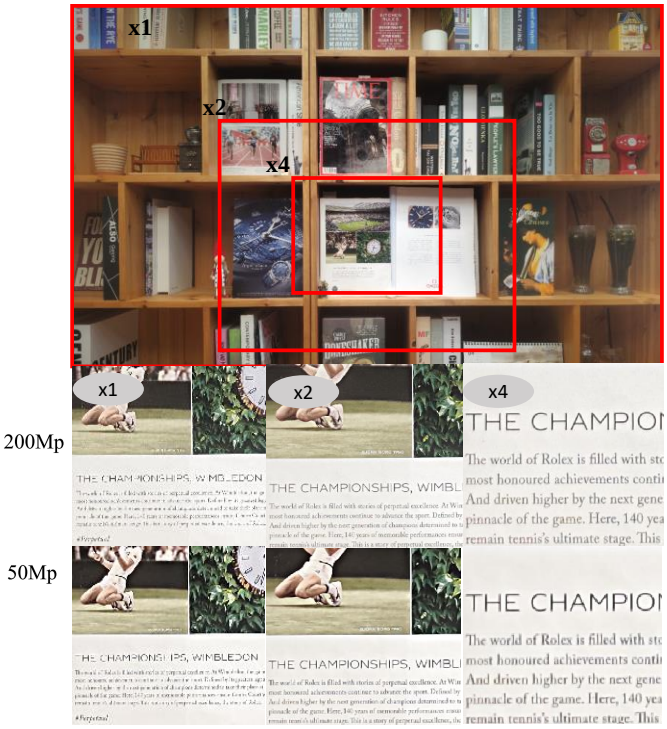


Fig. 4. Comparison between 200 MP and 50 MP with zoom x1, x2, and x4

Fig. 5. Detailed Captured Image with 200 MP (Deimensions of 28m x 22m)

Fig. 6 illustrates a chip microphotography of the implemented 200 MP stack sensor. The chip size is 11,799 µm x 10,758 µm. The top chip consists of pixels and the bottom chip consists of the columned ADC (comparator array, counter array, and a DAC), two row drivers, two PMUs, logics, and a CPHY.

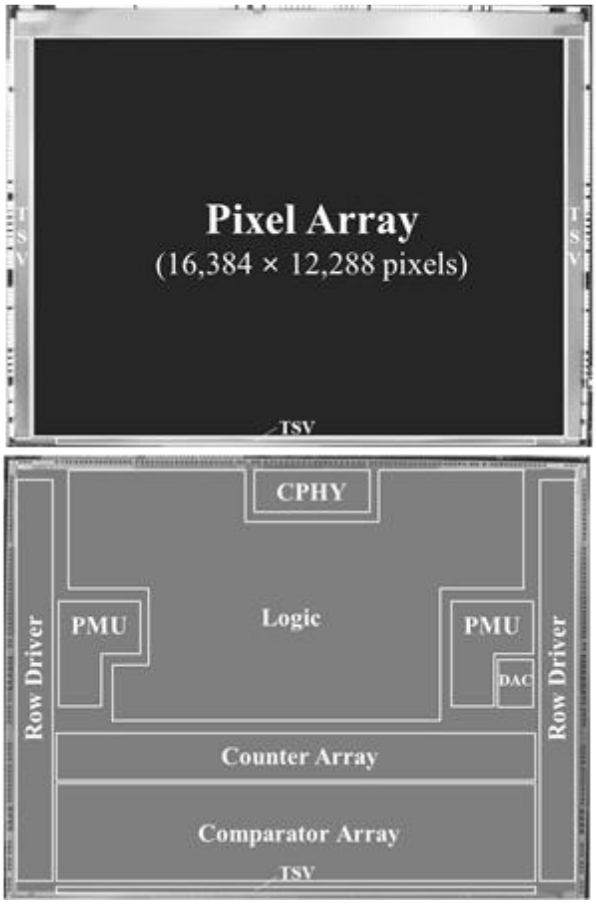


Fig. 6. Chip Microphotograph

Table II describes the comparison with other works [3]-[4]. This work is the first mass production 200 MP sensor for mobile applications. As of now, mass production of 200 MP sensor has been produced by 0.56 µm.

TABLE II. COMPARISON

Parameter	This work	[3]	[4]
Stack process	Top: 65nm Bottom: 28nm	Top: 40nm Bottom: 22nm	Top: 65nm Bottom: 28nm
Number of pixels	200MP	200MP	200MP
Pixel pitch	0.64μm	0.61μm	0.60μm
Full well capacity	6,000e-	5,000e-	10,000e-
Pixel shared type	4-shared	8-shared	8-shared
Trench type	Frontside deep trench isolation	Backside deep trench isolation	Frontside deep trench isolation
Transfer gate type	Single VTG	Single VTG	Dual VTG

IV. CONCLUSIONS

This paper presents the first mass production implementation of 200 MP stacked CIS with 0.64 μm-pitch pixels. The super resolution sensor over 200 MP is suitable to take pictures of objects on earth from satellites or adapt user experiences with various machine learning algorithms for the next generation sensors.

ACKNOWLEDGEMENT

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