Image sensor family with 1.40 µm pixel, 10ke- LFW, NIR-enhanced QE, extended dynamic range, and low power consumption

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Abstract*— *We are reporting on an image sensor family with 1.40 µm pixel size, multiple resolutions (5 MP, 8 MP, 20 MP), stacked backside illuminated, fabricated in 65 nm technology, with 6 µm silicon epitaxial thickness. The 1.40 µm pixel is the smallest pixel for low light surveillance imaging performance, combining low noise, increased near-infrared quantum efficiency, enhanced dynamic range and low power consumption for integration in energy-efficient battery-operated camera systems.

I. Introduction

We have developed a rolling shutter low power consumption image sensor family with 1.40 µm pixel size and array resolutions of 5 MP, 8 MP, and 20 Mp. Sensor design combined advanced technology features to address demanding requirements for surveillance, consumer and industrial imaging application. It demonstrates good low light performance, high responsivity in near infrared (NIR), and enhanced dynamic range. To the best of our knowledge this is the smallest pixel size to date to meet performance requirements for low light surveillance applications [1].

II. Pixel design and Operation

The pixel was designed in stacked backside illuminated (BSI) CMOS 65 nm technology, with 6 µm silicon epi and partial backside deep trench isolation (BDTI). To further increase the pixel quantum efficiency (QE) in the NIR spectrum for surveillance imaging, the backside process included a variant with inverted pyramids to extend the optical path of NIR photons [2]. The 1.40 µm pixel size was chosen for optimized trade-off between spatial resolution, signal-to-noise ratio (SNR) in low light conditions, and dynamic range.

Photodiode (PD) implants, potential profile, and layout were optimized through Technology Computer-Aided Design (TCAD) simulations and through silicon design-of-experiment (DOE) work to achieve 10 ke- linear full well (LFW) capacity while: (a) Maintaining a limited signal swing at the floating diffusion (FD) for reduced power consumption [3] and (b) Avoiding charge lag. Figure 1 presents vertical cross-section and top view of the PD in TCAD. The optimal PD pinning voltage allowed sufficient FD signal swing at a pixel supply voltage (Vaapix) not higher than 2.8V, which was essential in order to maintain low power consumption. Figure 2 presents LFW vs Vaapix curves in low conversion-gain (LCG) and high conversion-gain (HCG) modes. DOE analysis was also focused on ensuring pixel isolation, passivation of Si/SiO2 interface with the BDTI, and for preventing bright pixels - in order to minimize dark signal non-uniformity (DSNU) at elevated temperature conditions.

Figure 3 presents simplified schematics of the pixel circuit. The architecture is 1×2 shared row-wise with a dual conversion gain (DCG) transistor, TX1 and TX2 are the transfer gates, SF is the source follower transistor, RS is the row-select line, Pixout is the output pixel voltage, and SHR and SHS are the sample-and-hold reset and signal lines, respectively. Linear mode output is in 10-bit data format. Dual gain readout [4]- [5] is used for the enhanced dynamic range (eDR) mode. In eDR mode, the intra-scene dynamic range, which is defined as the ratio between the effective LFW and the total noise in the dark with 16.7 ms integration time, is up to 72.5 dB, and the data format is 12-bit.

Figure 4 presents the timing diagram of the circuit in eDR mode. In this mode, after charge integration, each pixel is read twice in two consecutive reads with high and low conversion gain, respectively. The HCG readout is correlated double sampling to cancel *kTC* noise on FD. The LCG readout is double sampling, which doesn't cancel the *kTC* noise component. Since *kTC* noise is lower than photon shot noise when the photo-signal is high, its unwanted contribution to the drop in signal-to-noise ratio (SNR) at the transition point between the HCG and the LCG reads is very small.

III. Pixel performance Characterization

Pixel characterization was conducted by methodologies that are used to evaluate signal and noise properties [6]. Figure 5 presents dark signal histogram at junction temperature, Tj, of 80C and 33 ms integration time. The standard deviation of the measurement, after conversion to charge units using the corresponding system gain, is the dark signal non-uniformity (DSNU) which equals 1.5 e-. Figure 6 shows read noise histogram at 25C with maximum gain, where the root mean square (RMS) of the distribution is 1.3 e-. Figure 7 presents photon-transfer curve (PTC) measurement at gain that is sufficiently low to extract the PD LFW. To highlight eDR mode dynamic range, Figure 8 is showing the eDR SNR curve and compares it to the SNR curve in linear mode with low conversion gain.

Three color filter array (CFA) variants were implemented to address specific image quality requirements in targeted markets: Bayer ('RGGB'), RGB-IR with 4x4 unit cell, and monochrome ('Mono'). The quantum efficiency (QE) curves of

the three variants are shown in Figure 9. The RGB-IR variant was developed with a backside process skipping the inverted pyramids for ensuring maximum dynamic range in the R, G, B channels. NIR QE enhancement was not required as NIR absorption in the silicon epi was sufficiently high to fulfill the requirements of the specific RGB-IR applications [2].

Figure 10 presents images that were captured in low light conditions under (a) visible and (b) NIR illumination. Both images were captured when the sensors were activated with maximum gain and integration time of 16.7 ms, where illumination conditions at the scene were (a) 5500K, 0.66 lux, and (b) 940 nm, 26.3 nW/cm2. Images are presented in signal range of 0 – 330 DN. The F#2 lens that was used during image capture had a VIS/940 nm dual-band filter with transmission greater than 95% in the visible band and at 940 nm. Figure 11 shows photos of the packaged image sensor products, where the 5 MP and 8 MP products are in a chip-scale package (CSP) and the 20 MP product is in a mixed-pitch ball grid array (MPBGA) package.

The SNR1s metric was introduced by Sony Semiconductor Solutions Corporation for quantitative evaluation of SNR of security cameras at low illumination [1]. SNR1s is defined as the illuminance on a gray target with 18% reflectance under 3,200K illumination for which SNR of the green channel equals 1, or 0 dB, when the camera is activated at room temperature with 1/60 sec exposure time and a F#1.4 lens that has 95% transmission and a CM500 infrared-cut filter. Figure 12 presents SNR1s values versus pixel size for various Sony STARVIS sensors – with smallest pixel size of 1.45 µm [1], and for the sensor family developed in this work. The SNR1s values are distributed along a curve decreasing with pixel size - as expected from the contribution of responsivity, i.e., the smaller the pixel the more challenging the low light performance and hence the more elevated values of SNR1s. The SNR1s performance of the 1.40 µm pixel developed in this work is improved versus the model described by the pixel area fit line.

The main performance parameters of the pixel array, applicable to the three array resolutions, are summarized in Table 1. The table presents SNR1 values as calculated for different conditions, such as at 80C and under 940 nm illumination.

IV. Conclusion

In summary, we are reporting on the development of a rolling shutter, low power consumption image sensor family with 1.40 µm pixel size, multiple resolution variants (5 Mp, 8 Mp, 20 Mp), BSI stacked, 65 nm technology, with 6 µm epi silicon, partial BDTI, and backside process option for enhancement of NIR QE. Sensor performance has demonstrated meeting the most demanding requirements for imaging in low light conditions in surveillance, consumer and industrial applications.

Acknowledgment

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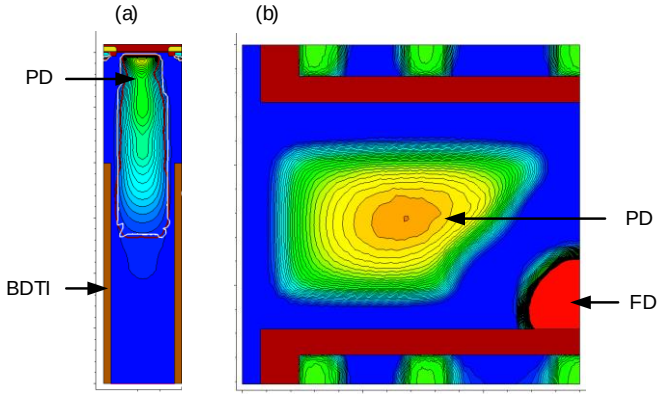

Figure 1. TCAD simulation: (a) Vertical cross-section in the middle of the PD;(b) Top view of the PD in the shallow region. As it can be seen, the PD is completely isolated from neighboring pixel.

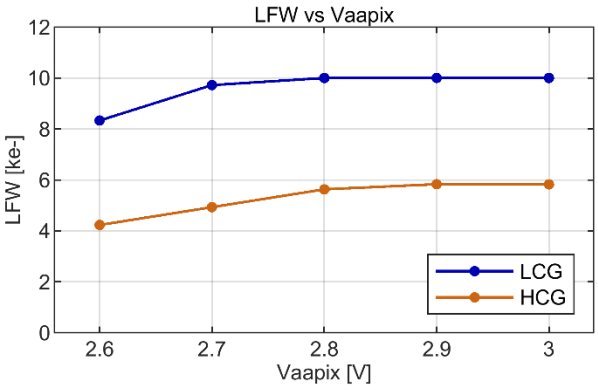

Figure 2. LFW vs Vaapix in LCG and HCG modes.

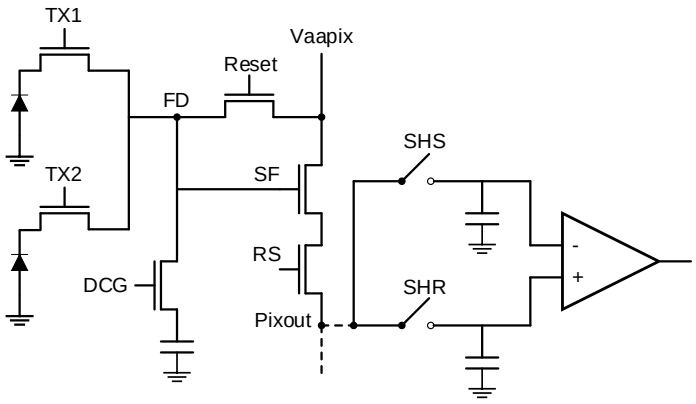

Figure 3. Simplified schematics of the pixel architecture, which is a 1x2 shared with a DCG transistor.

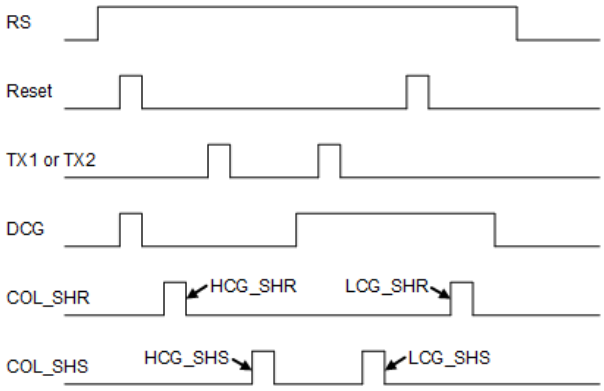

Figure 4. Timing diagram in eDR mode.

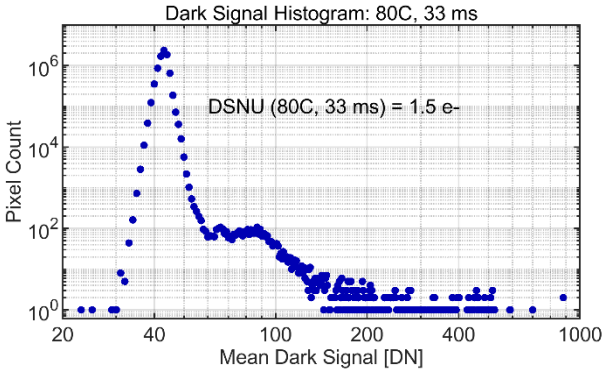

Figure 5. Dark-signal distribution at 80C, high gain, and 33 ms integration time. DSNU equals 1.5 e-.

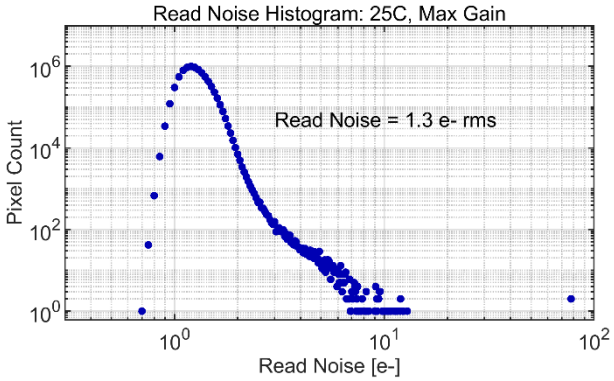

Figure 6. Read noise distribution at 25C.

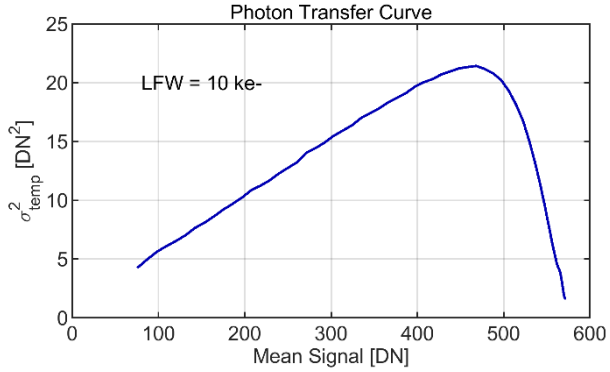

Figure 7. Photon transfer curve at low gain.

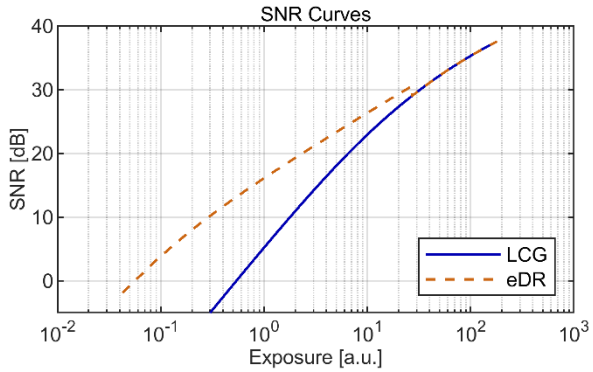

Figure 8. SNR curves in LCG and eDR modes.

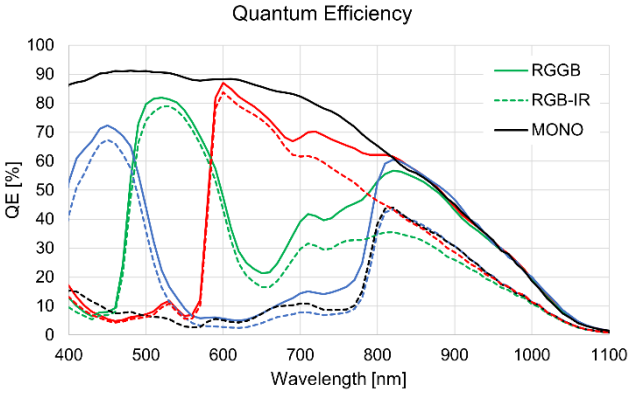

Figure 9. QE curves of the RGGB, RGB-IR, and mono CFA variants of the product.

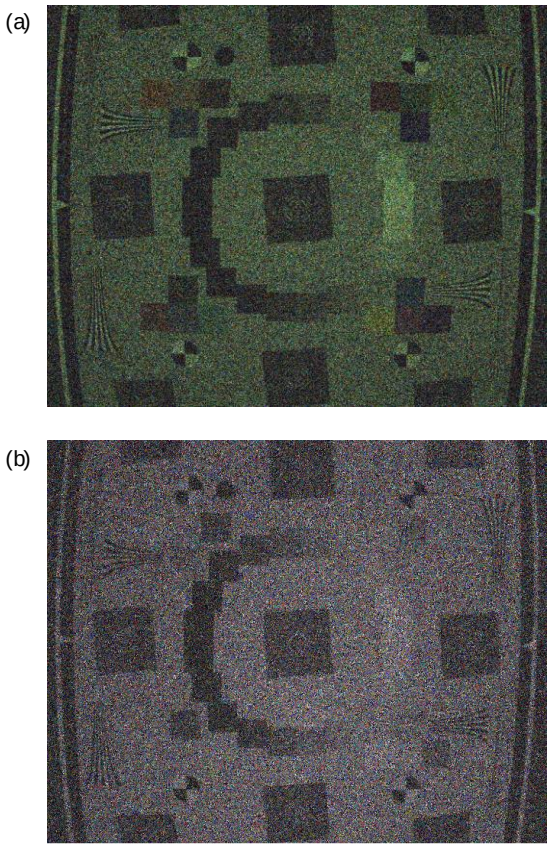

Figure 10. Color and NIR images in low illumination conditions: (a) 5,500K, 0.66 lux, and (b) 940 nm, 26.3 nW/cm^2

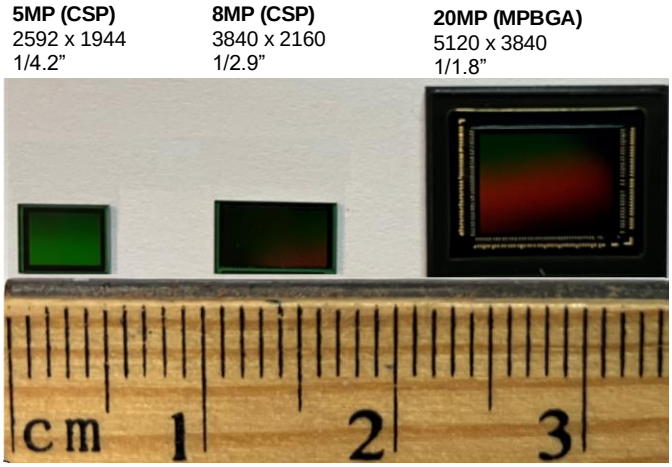

Figure 11. Photos of the 5, 8, and 20 MP image sensor products.

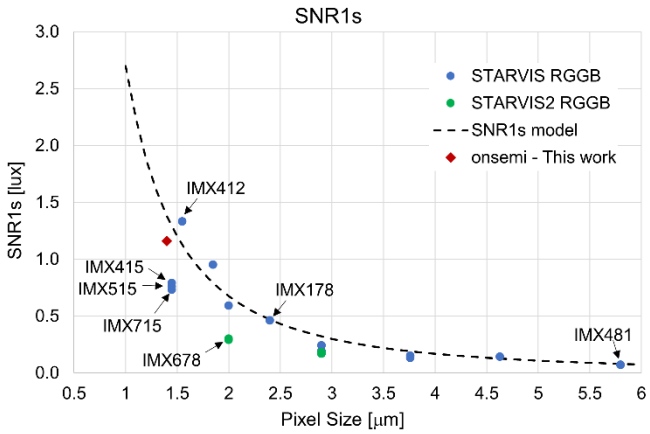

Figure 12. SNR1s of various security image sensor products versus pixel size.

Table 1. Sensor performance parameters

Parameter	Units	Typical values
LFW	ke-	10.0
DSNU, 33 ms, 80C	e-	1.5
Dark current, 80C	e-/s/pixel	66.0
Read noise, max gain, 25C	e- rms	1.3
eDR mode intra-scene dynamic range	dB	72.5
SNR1s at scene, 25C, 3200K, CM500, 16.7 ms, max gain	lux	1.2
SNR1 at image plane, 25C, 16.7 ms, max gain	e-/pixel	2.1
SNR1 at image plane, 80C, 940 nm, 16.7 ms, max gain	µW/cm^2	4.5
SNR1 at image plane, 80C, 16.7 ms, max gain	e-/pixel	2.3
Power consumption, 10-bit, 30fps, full resolution	mW	5 Mp: 100 8 Mp: <180 20 Mp: <280