Hot Carrier Injection Induced Random Telegraph Noise Degradation in a 0.8um-pitch 8.3Mpixel Stacked CMOS Image Sensor

Calvin Yi-Ping Chao, Meng-Hsiu Wu, Shang-Fu Yeh, Chih-Lin Lee, Chin Yin, and Honyih Tu
Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, ROC
Tel: (886) 3-5636688 ext 703-8243, email: calvin_chao@tsmc.com

***Abstract*—In this work we investigate the degradation of the random telegraph noise (RTN) and the threshold voltage ($\boldsymbol{V_t}$) shift of an 8.3Mpixel stacked CMOS image sensor (CIS) under hot carrier injection (HCI) stress. We report for the first time the significant statistical differences between these two aging behaviors. The $\boldsymbol{V_t}$ shift is relatively uniform among the whole population and gradually evolves over stress time. By contrast, the RTN degradation is evidently discrete and random in nature. The generation of new RTN traps during the time of stress is demonstrated both statistically and on the individual device level.**

I. Introduction

The hot carrier injection (HCI), the time dependent dielectric breakdown (TDDB), the bias temperature instability (BTI), and the electron migration (EM) are the most important aging and reliability issues for advanced CMOS devices [1]. In this study, we focus on the HCI induced aging effects. Although the threshold voltage (V_t) shift and the mobility degradation caused by HCI stress are well-known for over 40 years, the impacts on random telegraph noises (RTN) are less studied or reported [2–5], especially the statistical behavior of large sample sizes.

In state-of-the-art CMOS image sensors (CIS), the pixel pitch is comparable to the visible light wavelength and the full well capacity (FWC) of the photodiode is reduced to the range of 5000 to 6000 electrons [6]. Although the median readout noise of 1 e-rms or less can be achieved by design, the RTN on the noise distribution tail could be more than 10 times higher than the median noise. Therefore, RTN becomes a performance limiting factor to achieve high dynamic range and good image quality.

II. Test Chip Design

The test chip is a stacked backside-illuminated CIS with a sensor array on the top layer, fabricated by a 28 nm 1P4M process, and a readout circuit layer on the bottom by a 22 nm 1P7M process, stacked by a wafer-level hybrid bond (HB) technology. The array consists of 2512×3296 (8.3M) pixels with a 0.8 um pitch and a 4×2-shared structure, read out by a bank of 1648 column-parallel 12-bit ADCs with front-end amplifiers supporting 1X to 8X analog gains. A simplified signal-chain schematic is shown in Fig. 1. The 3 pixel-devices, the reset (RST), the row select (RSL), and the source follower (SF), support 3.3 V operation. The device under study is the SF NMOS with W = 0.16 um, L = 0.87 um, and 5.7 nm dielectric thickness, biased by a constant column current source of 7.2 uA in normal operations. The conversion factor from the ADC output to the SF output is 292 uV/DN at 1X gain and 36.5 uV DN at 8X gain. The median read noise is about 190 uV-rms operated at 60 MHz clock and 1.48 fps frame rate.

III. HCI Stress Experiments

In normal imaging mode, the SF output (V_O) is read out by a correlated double sampling (CDS), before and after the charge transfer from the photodiode to the sense node (SN). The voltage difference is amplified and digitized. In this work, we are only concerned with the SF. The charge transfer is disabled, and the SF gate voltage (V_G) is fixed by RSV with RST turned on. The readout random noise (RN) is measured by the CDS. But V_O is obtained in a test mode by measuring the difference between V_O and a fixed reference voltage.

The SF drain voltage (V_D), or the V_{PIX} in Fig. 1, is 3.1 V for normal operation. When V_D is increased, the channel conduction electrons are accelerated by the high electric field. The energetic and hot electrons can in turn generate more electron-hole pairs by the process of impact ionization. This is characterized by the rapid increase of the substrate current (I_B) due to the holes as V_D increases. Fig. 2 shows the measured I_B of a SF device vs. V_D under various current biases in separate test keys on the same wafer as the CIS chip.

In typical reliability testing, the supply voltage is raised to 20%-50% higher than its normal value to speed up the device aging. In our experiments, the SF is biased by a 7.2 uA source current (I_S), and we choose to raise the V_{PIX} in Fig. 1 up to 6.6 V where the I_B becomes comparable to I_S according to Fig. 2. Several devices under test (DUTs) were selected and stressed for 10, 20, 50, and 100 min at room temperate. Between 2 consecutive stressing, the DUT is measured under normal operation conditions. Negligible relaxation effects were observed for several days after stressing.

Because of the row-by-row rolling readout and there are 628 rows of SFs in the pixel array, the stress imposed on the DUT is different when it is active (RSL turned on, I_S = 7.2 uA, about 1/628 of the stress time) and when it is inactive (RSL turned off, I_S ~ 0 uA, about 627/628 of the stress time). It requires further study in the future to distinguish these two stress effects and their dependencies on stress voltages.

IV. HCI Induced Vt Shift and RN Degration

Two well-known device aging effects caused by HCI are threshold voltage shift and mobility degradation [1]. In our SF configuration, either the increase of V_t or the decrease of mobility lead to the similar decrease of the SF output voltage. Since the V_G and I_S of the SF are fixed in our experiments, the change of SF output is considered as an effective V_t shift (ΔV_t) in the rest of this paper. Fig. 3 shows the measured

distribution of V_{GS} after a series of HCI stress up to 100 min. The change of V_{GS} (effective ΔV_t) is small and not much noticeable in Fig. 3. But the ΔV_t becomes very clear in Fig. 4 histograms by subtracting the unstressed V_{GS} from the stressed V_{GS} for each stress time t, $\Delta V_t(t) \stackrel{\text{def}}{=} V_{GS}(t) - V_{GS}(0)$. The corresponding inverse cumulative distribution function (ICDF) family of curves are plotted in Fig. 5. The systematic increasing trend of ΔV_t of various constant ICDF contours are shown in Fig. 6.

The random noises (RN) are calculated as the standard deviation of 100 consecutive frames of data, device by device. The change of RN before and after HCI stress is calculated as $\Delta RN(t) \stackrel{\text{def}}{=} \sqrt{\left(RN(t)\right)^2 - \left(RN(0)\right)^2}$.

The histograms and ICDF curves of ΔRN are shown in Fig. 7–8 and the dependence on stress time is plotted in Fig. 9. Apparently, there are similarities between Figs. 4–6 and Figs. 7–9. However, close examination in the next section shows there are significant differences as well.

V. KEY FINDINGS

The differences in the degradation of V_t and RN become clear when we look at how the individual devices change progressively throughout the stress time. Fig. 10(a)–(c) show the correlation scatter plots of the ΔV_t after 20-, 50-, and 100-min stress vs. that after 10-min stress. Regardless of the device-to-device variation, we observe that all the 1M devices are degraded uniformly. All the data points concentrate in the neighborhood along a straight line in each plot. The x/y ratios 1.78, 2.56, and 3.35 of the lines are roughly proportional to the ratios of the logarithm of the stress time.

By contrast, the correlation of the ΔRN after 20-, 50-, and 100-min stress vs. that after 10-min stress plotted in Figs. 11(a)–(c) show very different features. The scatter plots have two obvious branches. In each figure, one group of data points are centered along the x=y diagonal line, representing the devices whose RNs remain unchanged after different stress times. The other group of data points on the lower right branch correspond to the devices with RN significantly increased after longer stress time. It is also clear that the number of the points in the lower right branch continues to increase as the stress time is increased.

As previously reported [7–8], the RN distribution tails are dominated by the RTN devices showing charge emission and capture activities. The interpretation of Figs. 11(a)–(c) is that many new RTN traps are generated discretely during the stress time, while some existing RTN traps remain unchanged. Such a separation of two distinct groups does not exist in the ΔV_t scatter plots Figs. 10(a)–(c).

VI. RTN GENERATION AND DEGENERATION

The RTN devices are characterized by the multiple discrete signal levels in their time domain waveforms. We sort the 5000-frame waveforms of the entire 1M devices after each stress time according to the number of histogram peaks identified. Because of the CDS, a single trap in theory should generate a symmetric 3-peak histogram. In real data, 2-peak histograms are often observed [7]. For simplicity, we consider both the 3-peak and 2-peak cases as single-trap RTNs and plot them separately on top of the total population histograms in Figs. 12(a)–(c) for 3 stress times. Clearly the tail portion of the RN histograms are dominated by the RTN devices. And the number of RTN devices increases as the stress time increases.

Moreover, we could monitor the individual devices to see how they evolve over time. Figs. 13(a)–(c) show the snapshots of the signal waveforms and their corresponding histograms of 3 selected devices after 0-, 20-, and 100-min stress. The device in Fig. 13(a) shows a single RTN trap before the stress and remains unchanged after 20- and 100-min stress. The device in Fig. 13(b) shows no trap before stress, but one single trap defect is generated after 20 min stress and stayed the same up to 100 min stress. Fig. 13(c) shows an example device with no RTN trap after 20 min stress and one RTN trap is generated after 100 min stress. These are concrete evidence of trap generation during the HCI stress.

A defect-related RTN trap may be caused by process-induced damage (PID) or by HCI stress. Once a defect is generated, it is not expected to disappear through further stress. However, Fig. 14(a)–(b) show two examples where the 3 discrete RTN peaks might degenerate to 1 peak due to the broadening the peak width. We speculate that it is caused by the increase of non-RTN noises such as the flicker noises due to the degradation of interface states. A careful separation of the flicker noise and RTN degradation requires further study. Finally, the number of devices with identified RTN traps is plotted against stress time in Fig. 15.

VII. CONCLUSION

The RTN degradation caused by HCI stress in a CIS chip is studied both statistically and on the level of individual devices. The results highlighted the characteristic differences between the effective V_t shift and the RTN degradation, although their physical mechanisms might be similarly related to the generation of interface states and traps inside the gate dielectric by energetic electrons and holes. Monitoring the RTN degradation could be a useful tool to study the long-term reliability of MOSFET devices. More systematic experiments on a wider range of voltages and the time dependence of the HCI stress effects are in progress.

REFERENCES

[1] T. Grasser, Editor, *Hot Carrier Degradation in Semiconductor Devices*. Cham, Switzerland: Springer International Publishing AG, 2015.

[2] T. Ahmed, *et al.*, “Identification of channel hot carrier stress-induced oxide traps leading to random telegraph signals in pMOSFETs,” IEEE T-ED, vol. 68, no. 2, pp. 713–719, Feb. 2021.

[3] H.-S. Song, *et al.*, “Investigation of random telegraph noise characteristics with intentional hot carrier aging”, IEEE IRPS Digest, pp. P61.1–P61.4, Apr. 2020.

[4] A. B. Manut, *et al.*, “Impact of hot carrier aging on random telegraph noise and within a device fluctuation,” IEEE J-EDS, vol. 1, pp. 15–21, Jan. 2016.

[5] C. Liu, *et al.*, “New observations on hot carrier induced dynamic variation in nano-scaled SiON/poly, HK/MG and FinFET devices based on on-the-fly HCI technique: the role of single trap induced degradation,” IEEE IEDM Digest, pp. 34.6.1–34.6.4, Dec. 2014.

[6] S. Park, *et al.*, “A 64Mpixel CMOS image sensor with 0.56µm unit pixels separated by front deep-trench isolation,” IEEE ISSCC Digest, pp. 108–109, Feb. 2022.

[7] C.Y.-P. Chao, *et al.*, “CMOS image sensor random telegraph noise time constant extraction from correlated to uncorrelated double sampling,” IEEE J-EDS, vol. 5, pp. 79–89, Jan. 2017.

[8] C.Y.-P. Chao, *et al.*, “Statistical analysis of random telegraph noises of MOSFET subthreshold currents using a 1M array test chip in a 40 nm process,” IEEE J-EDS, vol. 9, pp. 972–984, Oct. 2021.

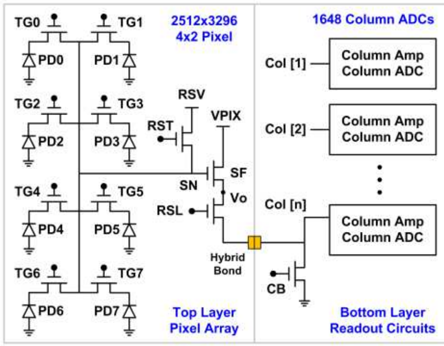


Fig. 1. Simplified test chip architecture. The device under stress is the source follower (SF) NMOS in the 4x2-shared pixel on the top layer. The total number of SF is 628x1648 ~1M.

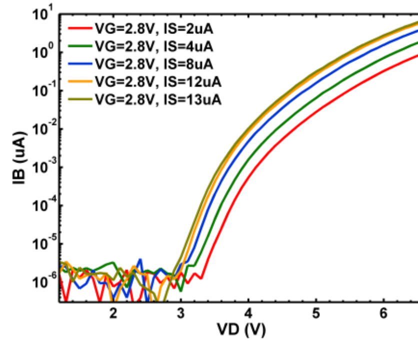


Fig. 2. The substrate current I_B of a stand-alone SF in a separate test key as a function of the drain volage V_D indexed by a family of source currents I_S while the gate voltage V_G is fixed.

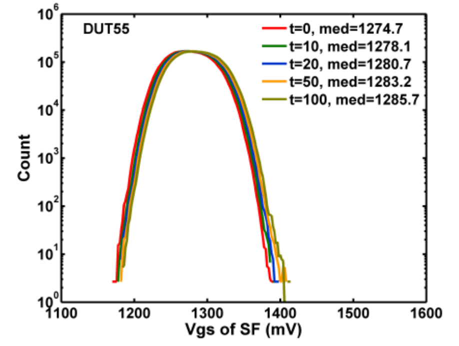


Fig. 3. The histogram of the gate-to-source voltage V_{GS} of the SF biased at a constant source current of 7.2 uA (default operation) after the HCI stress time (t) from 0 to 100 min.

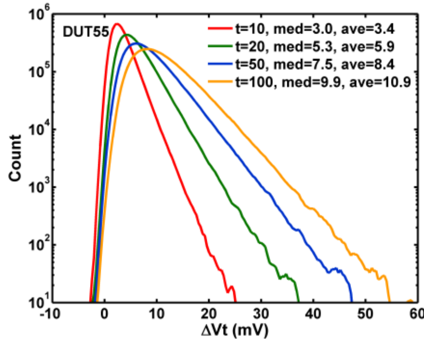


Fig. 4. The histogram of the SF threshold voltage shift (ΔV_t) after the HCI stress time (t) from 10 min to 100 min.

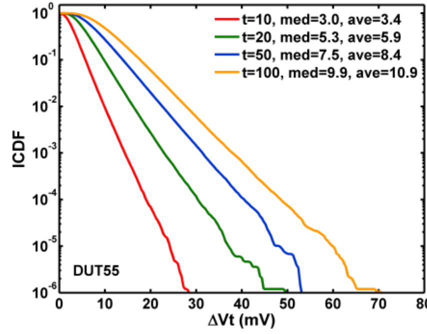


Fig. 5. The ICDF of the SF threshold voltage shift (ΔV_t) after the HCI stress time (t) from 10 to 100 min.

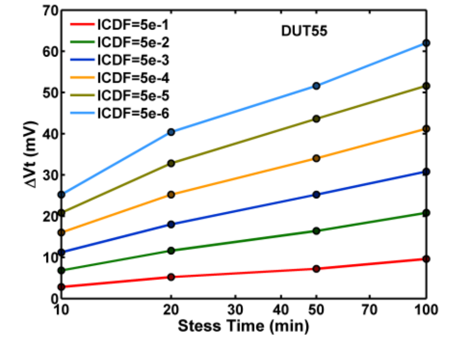


Fig. 6. The SF threshold voltage shift (ΔV_t) vs. the HCI stress time of various constant ICDF contours from 5e-1 to 5e-6.

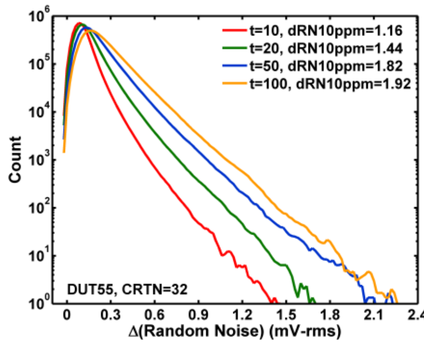


Fig. 7. The histogram of the increase of random noise (ΔRN) after the HCI stress time (t) from 10 min to 100 min.

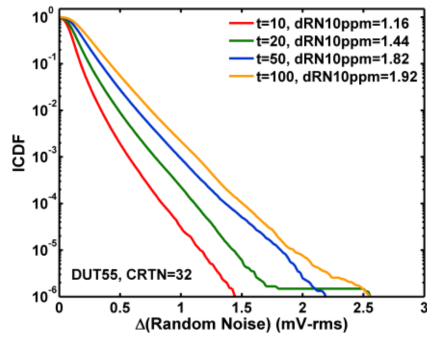


Fig. 8. The ICDF of the random noise increase (ΔRN) after the HCI stress time (t) from 10 min to 100 min.

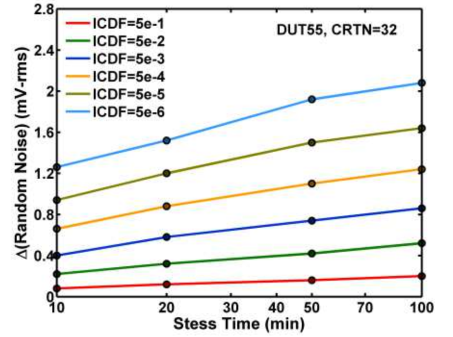
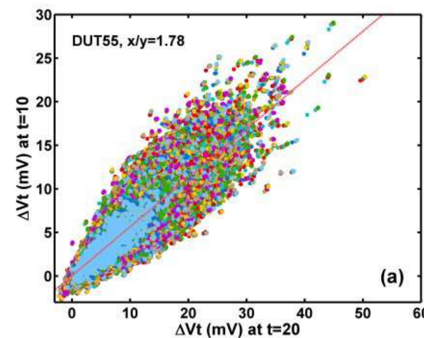
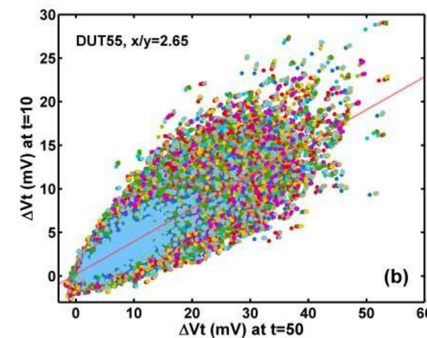


Fig.9. The increase of random noise (ΔRN) vs. the HCI stress time at various constant ICDF levels from 5e-1 to 5e-6.





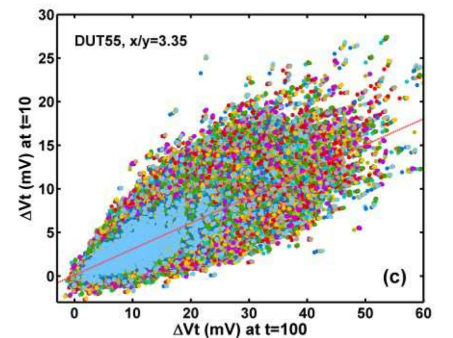


Fig. 10. The correlation of the SF threshold voltage shift (ΔV_t) after 10 min HCI stress vs. after (a) 20 min, (b) 50 min, and (c) 100 min stress, respectively. The linear least-square fit of the x/y ratio (red dash line) shows the continuous increase of the ΔV_t as the stress time increases. The ΔV_t increases are relatively uniform among all 1M devices, which are different from the random noise increases shown in Fig. 11 below.

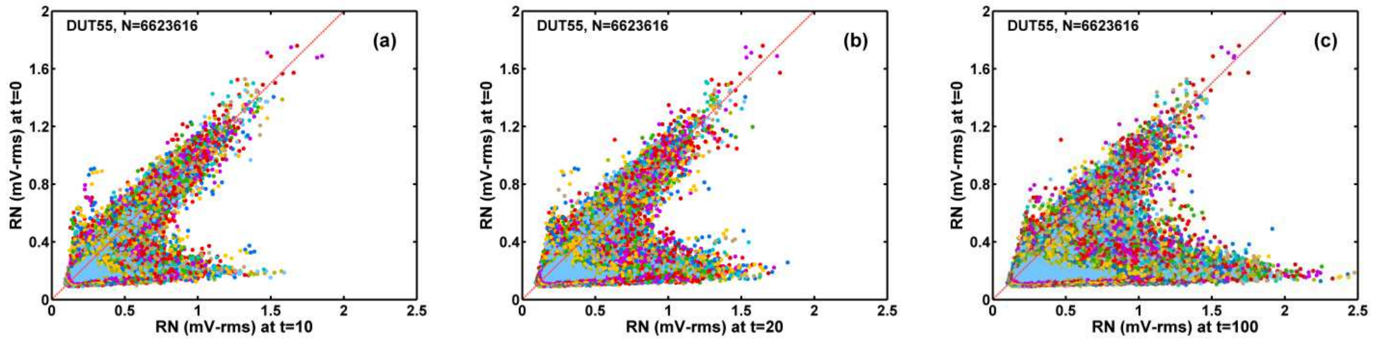


Fig. 11. The correlation of the random noises (RN) before HCI stress (t = 0) vs. after (a) 10 min, (b) 20 min, and (c) 100 min stress, respectively. The RN increases are noticeably nonuniform. The RN along the x=y red dash line remains relatively unchanged. The devices on the lower-right branches show significant increase of RN. The population of the lower branch (estimated as the number M) increases as the stress time increases.

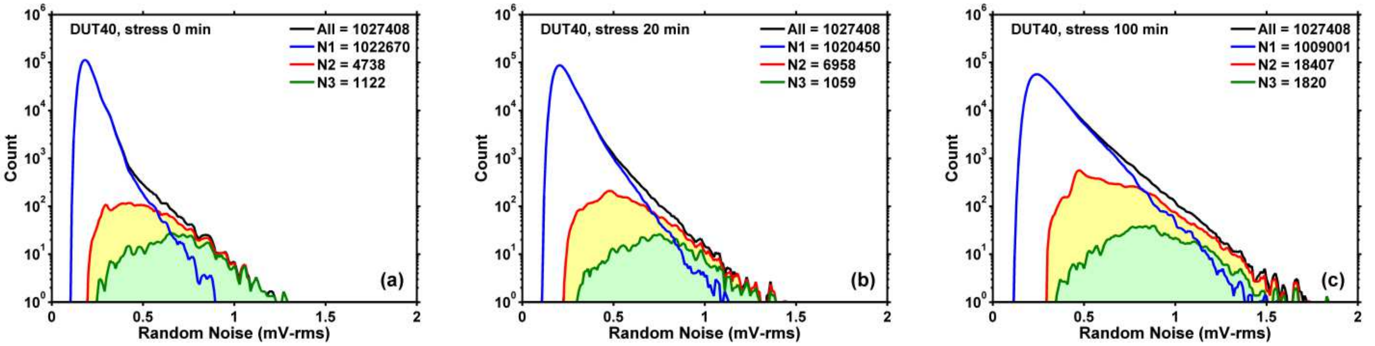


Fig. 12. The RN distribution of the RTN devices, identified by the discrete levels of their 5000-frame waveforms, (a) before HCI stress, (b) after 20 min stress, and (c) after 100 min stress. The RTN devices clearly contribute and dominate the long tails of the RN histograms. The number of RTN devices increases systematically as the stress time increases.

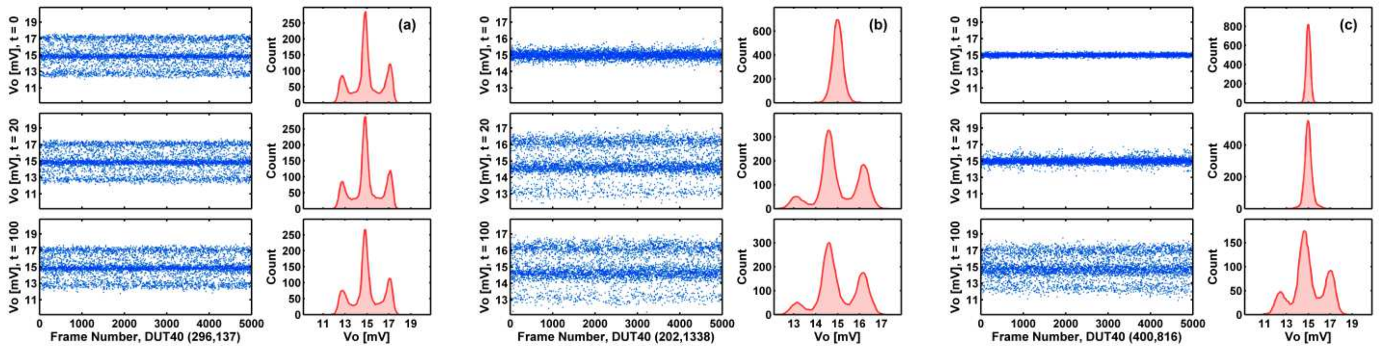


Fig. 13. Generation of RTN traps during HCI stress. The 5000-frame waveforms before (t = 0) and after the HCI stress (t = 20, 100 min) with the corresponding histograms are shown for 3 selected examples. (a) Device (296, 137) shows 1 trap before stress and remains unchanged after stress. (b) Device (202, 1338) shows no trap before stress, and 1 trap generated after 20 min stress. (c) Device (400, 816) shows no trap before stress, but 1 trap generated after 100 min stress.

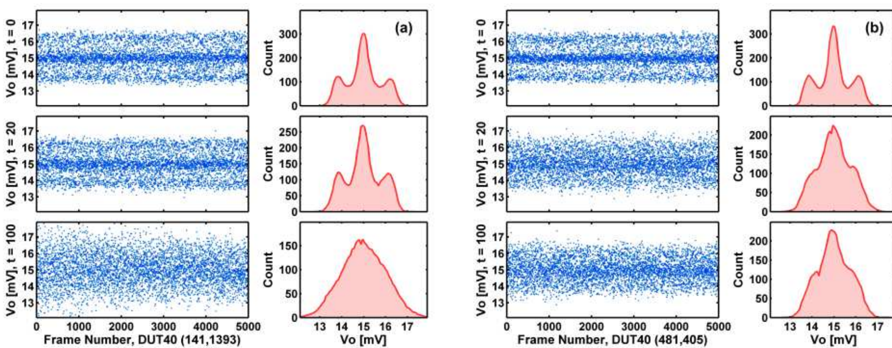


Fig. 14. Degeneration of the RTN discrete levels. During the HCI stress, the non-RTN noises may be increased significantly such that the discrete RTN levels become indistinguishable. (a) Device (141, 1393) shows such degeneration after 100 min stress. (b) Device (481, 405) shows degeneration after 20 min.

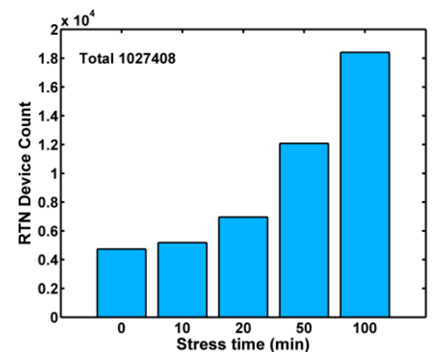


Fig. 15. Estimated number of RTN devices before and after the HCI stress based on the time-domain signal waveforms.

Gate Oxide Benchmarking For Low Frequency Noise Improvement On 3D Stacked CMOS Image Sensors

Maria Gouveia Da Cunha [1,2], Sebastien Place [1], Olivier Gourhant [1], Sebastien Haendler [1], Pierre Magnan [2], Philippe Martin-Gonthier [2], and Vincent Goiffon [2]

[1]STMicroelectronics, 850 Rue Jean Monnet, 38920 Crolles, France
Telephone: 04 76 92 60 00
[2]ISAE-SUPAERO, 10 Av. Edouard Belin, 31400 Toulouse, France

Email: maria.gouveiadacunha01@st.com

I. INTRODUCTION

Low Frequency Noise (LFN) and especially Random Telegram Signal (RTS) can limit the performance of CMOS Image Sensors (CIS) in low light level applications. This is especially true for demanding small-pixel-pitch-CIS-generations optimized for mobile applications [HAS19]-[NAK21].

RTS impacts mainly two specific devices in CIS: the Source Follower (SF) of the pixel located in the top-tier part and the Analog-to-Digital Converter (ADC) circuit deported in the bottom-tier part [CHA21]. 3D-stacked CIS technology gives the opportunity to treat independently top and bottom sources of RTS, as shown in Fig 1. The decreasing number of devices to integrate in the top-tier part provides more process flexibility and margin to optimize at the same time the photodetection performances (driven by the photodiode) and the low noise charge-to-voltage conversion (influenced by the SF) without impacting the rest of the circuit. This aspect is developed in the following sections by proposing a dedicated gate oxide benchmarking for the top-tier and the corresponding impact on noise is studied. On the contrary, the optimization of bottom-tier ADC devices has a direct influence on the performance of the whole circuit. Hence, the RTS reduction in ADC devices by process optimization is not addressed in this study.

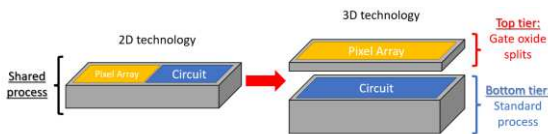


Fig 1: 3D stacked Image Sensor. Gate Oxide (GO) process splits under investigation on the pixel array part.

II. GATE OXIDE PROCESS PLAN DESCRIPTION

As exposed, a wide variety of top-tier gate oxide processes have been explored throughout this noise study. Among them, furnace oxidation, rapid thermal oxidation or nitridation processes will be further commented.

Furnace gate oxidations (FUR A and B) are slow and low temperature processes (slow increasing and decreasing temperature ramp). FUR A and B have different oxidation capabilities.

Rapid Thermal Oxidation (RTO) processes (Process Of Reference (POR)/RTO A, RTO B and RTO C) were developed to enable short time, high temperature oxidation. POR/RTO A and B have fixed oxidizing atmospheres, but temperature A is lower than B. RTO B and C have different oxidizing atmospheres but with fixed temperature.

Gate oxide nitridation processes (NIT A, B and C) are used as a barrier to prevent poly gate dopant diffusion inside the channel. POR and NIT A have the same process with different nitrogen doses (NIT A has a lower N dose than the POR). NIT A, B and C have different nitridation conditions leading to different N diffusion profiles in gate oxide bulk. NO NIT corresponds to a no nitridation condition.

Table 1 summarizes the various process trials and acronyms which are covered in this study.

TABLE I. GATE OXIDE SPLITS DESCRIPTION

<table>
<tr><th colspan="6">Gate oxide splits</th></tr>
<tr><td colspan="6">Furnace</td></tr>
<tr><td colspan="3">FUR A</td><td colspan="3">FUR B</td></tr>
<tr><td colspan="6">Different oxidation capacity</td></tr>
<tr><td colspan="6">Rapid thermal oxidation</td></tr>
<tr><td colspan="2">POR/RTO A</td><td colspan="2">RTO B</td><td colspan="2">RTO C</td></tr>
<tr><td colspan="3">RTO A & RTO B: Fixed atmosphere and $T_A<T_B$</td><td colspan="3">RTO B & RTO C: Different atmospheres & $T_C=T_B$</td></tr>
<tr><td colspan="6">Nitridation</td></tr>
<tr><td>NIT A</td><td colspan="2">NIT B</td><td colspan="2">NIT C</td><td>NO NIT</td></tr>
<tr><td>POR & NIT A: Same process N dose: NIT A< POR</td><td colspan="4">NIT A & NIT B & NIT C: Different nitridation condition leading to different N diffusion profile</td><td>No nitridation</td></tr>
</table>

III. CHIP DESIGN SPECIFITIES AND INDIVIDUAL TEST STRUCTURES

The tested image sensor is constituted of 0.7 Mpix based on a classical 4T pixel architecture depicted in Fig 2. It is composed of NMOS pixel transistors with fixed narrow geometries: SF, Reset (RST) and Read (RD). A pinned photodiode allowing charge collection is coupled to a Transfer Gate (TG) for charge transfer to the SF + RD readout chain. Additional individual test structures are also available and used for device material characterization: large geometry NMOST and PMOST (Specific standard V_{th} MOSFETs). In this work, it is proposed to focus on the SF contribution (Low V_{th} pixel MOSFETs) as it causes most of noise performance. RST and RD are considered as standard V_{th} pixel MOSFETs.

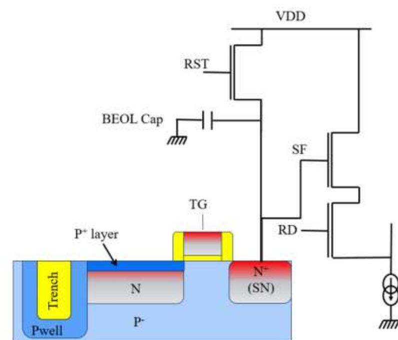


Fig 2: 4T electrical pixel architecture studied

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Gate oxide characterization

Before comparing electrical measurements, a full set of in-line oxide thickness measurements has been done (see Fig 3).

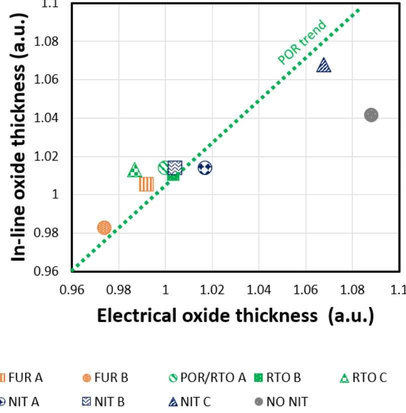


Fig 3: Relative in-line oxide thickness variation as a function of the extracted electrical oxide thickness

These ellipsometric measurements have been compared to Electrical Oxide Thickness (EOT) measured on large capacitance structures biased in accumulation at Parametric Test (PT). A good alignment between both measurements is seen except for NO NIT. For this process split, EOT is attributed to a significant change in relative dielectric permittivity of the gate oxide (ε_{ox}), as depicted in equation (1):

$$EOT = \frac{\varepsilon_{ox}\varepsilon_0}{C_{ox}} \qquad (1)$$

EOT and the oxide capacitance C_{ox} per surface unit are inversely proportional. ε_0 is the vacuum permittivity.

In addition, C_{ox} is directly related to the RTS amplitude $\frac{\Delta I_{DS}}{I_{DS}}$ as illustrated by [KIR89]-[SIM92]:

$$\frac{\Delta I_{DS}}{I_{DS}} = \left(\frac{gm}{I_{DS}}\right)\frac{1}{WL}\frac{q}{C_{ox}} \qquad (2)$$

Where I_{DS} is the MOSFET drain current, g_m is the MOSFET transconductance, W and L are the MOSFET dimensions. The lower the C_{ox}, the higher the RTS amplitude. As a consequence, it is expected to have a higher RTS amplitude for NO NIT.

Finally, it is observed that NIT C split is significantly marginal in terms of EOT. Compared to POR, NIT C is a nitridation process using an oxidizing step resulting in a higher oxide thickness, as shown in Fig 3.

To go deeper in material characterization, the process comparison has been extended on large MOS structures to avoid edge MOS effects. By comparing threshold voltage (V_{th}) maps for each of them as a function of EOT and with respect to gate oxide splits, it is possible to highlight material properties variations.

Detailed ΔV_{th} vs EOT maps are plotted for NMOST in Fig 4 and for PMOS in Fig 5.

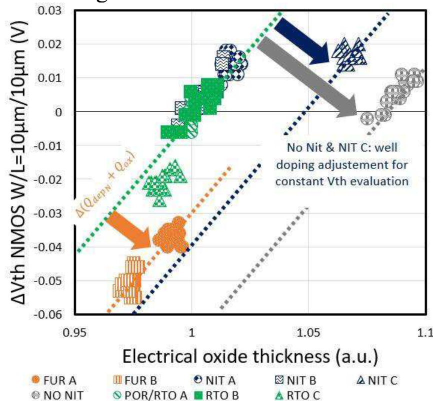


Fig 4: Large NMOST threshold voltage variation V_{th} as a function of the electrical oxide thickness for each GO process.

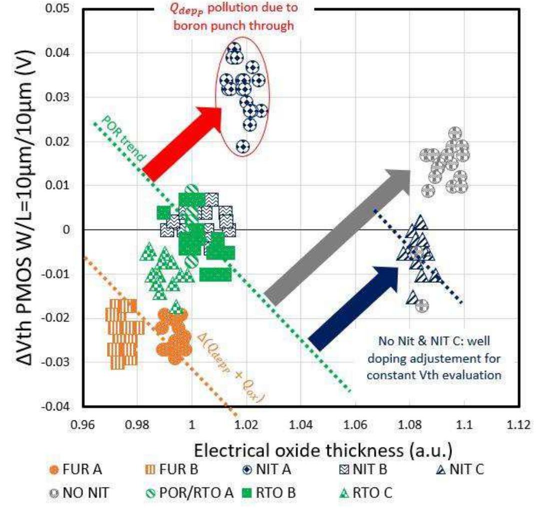


Fig 5: Large PMOST threshold voltage variation V_{th} as a function of the electrical oxide thickness for each GO process.

Equations (3), (4) and (5) help to understand the relationship between the V_{th} and EOT plots:

$$V_{th} = V_{FB} + \Phi_d + \frac{Q_{dep}}{C_{ox}} \qquad (3)$$

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} \qquad (4)$$

$$C_{ox} = \frac{\varepsilon_{ox}.\varepsilon_0}{EOT} \qquad (5)$$

Where V_{FB} is the flatband voltage, Φ_d is the potential voltage drop at the depleted region and Φ_{ms} is the work function difference between Φ_m of the gate material and Φ_s of the substrate.

Most of the process splits follow the POR trend represented by the green dashed lines. For both NMOST and PMOST V_{th} decreases for furnace anneals processes, as shown in orange. It is consistent with thermal budget change (or channel depletion layer Q_{dep} modification) and/or fixed charges (Q_{ox}) modification (consistent with more positive charges), as depicted in (3) and (4). RTO C is impacted the same way but less significantly. More significant changes are observed with nitridation related process splits. For PMOST, V_{th} is shifted for NIT A. Since NIT A has a lower N dose compared to POR process, it is believed that $Q_{dep,p}$ is polluted due to poly gate dopants punch through. NIT B does not highlight any change compared to POR. Taking into account the positive charge influence on NIT C and NO NIT process splits, Q_{dep} has been treated specifically to match V_{th} value with POR. As a consequence, in NIT C, Q_{dep} is respectively decreased by 10% for PMOST and increased of same proportion for NMOST, highlighting positive fix charge contribution changes and especially much important nitrogen diffusion in the oxide. For NO NIT, Q_{dep} is respectively increased by 50% for PMOST and decreased by 30% for NMOST illustrating here positive fixed charge reduction.

In this study, noise measurements are performed on the test chips composed of small area SF MOST. In order to characterize the studied devices, V_{th} variation of SF and RD MOSTs as a function of the gate oxide process is plotted in Fig 6. SF and RD are both narrow channel transistors with respectively dedicated pixel Low and Standard V_{th}.

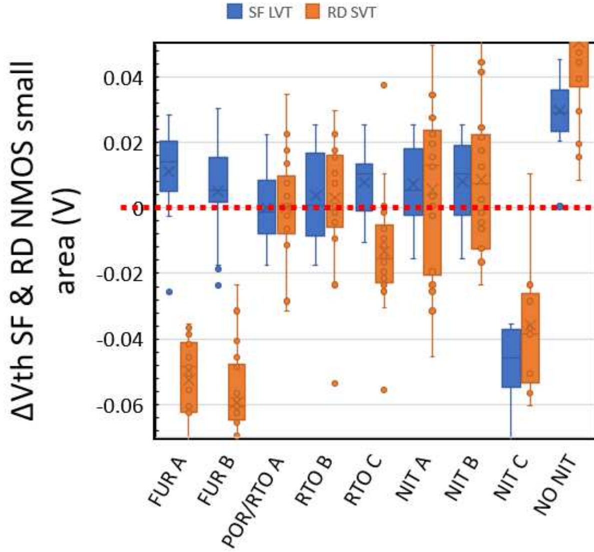


Fig 6: Source Follower threshold voltage variation versus Readout threshold voltage variation for each GO process split compared to the POR value.

It is observed on SF that V_{th} are relatively less impacted by the studied process splits, except by NIT C and NO NIT due to uncompensated positive fixed charge effect. Since SF has a narrow channel, it is assumed that V_{th} variation's contributions are not the same as in large width NMOS transistors. Lateral edge MOST contribution is added to the central MOST one.

In addition, it is observed for RD that V_{th} follows comparatively the same variation as SF Low V_{th}, except for furnace splits FUR A and B. This highlights that Standard V_{th} are more sensitive to diffusion due to thermal budget, consistently with large NMOSTs observations.

B. *Noise extraction and discussion*

Based on 4T pixel architecture, temporal noise from each individual structure was acquired for the 700 thousand SF + RD. Fig 8 shows the relative cumulated temporal noise (TN) population at two thresholds as depicted in Fig 7: T1 and T2=2xT1. In this study, a RTS pixel is defined as a pixel with a higher TN value than the threshold T1 or T2 [WAN06], [KIT22].

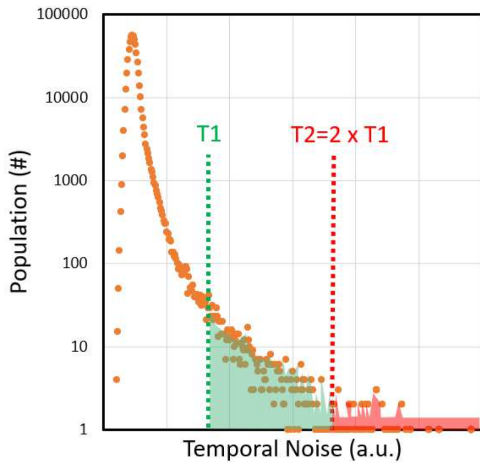


Fig 7: Temporal noise (TN) population distribution for 1 die (700000 pixels).

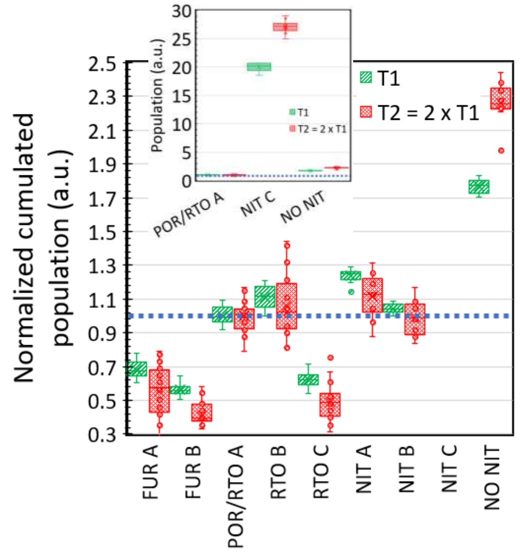


Fig 8: Relative cumulated temporal noise population for T1 (green) and for T2 (red).

FUR A, FUR B and RTO C conditions have the lower TN population compared to POR. On the other hand, NIT C and NO NIT show the higher TN population, consistent partly with [HA17]. Another important parameter representative of interface state evolution is photodiode dark current variation related to POR, as shown in Fig 9. Dark current depicts slight degradation for NIT C due to interface state degradation caused by significantly higher N diffusion, impacting electrons current generated underneath TG, in accumulation biased mode. It suggests that this process shared on TG and SF gate oxide is responsible of a significant degradation of near interface traps for both dark current and RTS. NO NIT degradation could be linked to significant EOT increase (due to ε_{ox}change) being responsible of RTS amplitude degradation as developed earlier.

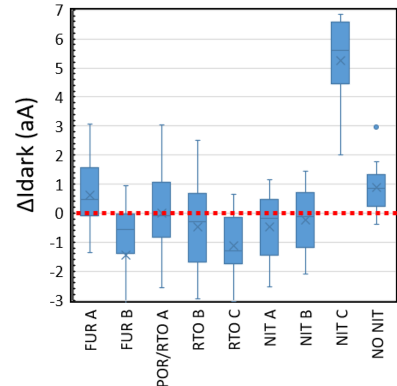


Fig 9: Dark current shift versus process splits

From the normalized current spectral density S_{I_d}/I_{d^2} of SF (at f=10Hz) [HUN90]-[LOP11], the trap density N_{it} has been extracted ($cm^{-3}.eV^{-1}$) and is plotted in Fig 10:

$$\frac{S_{Id}}{I_d^2} = S_{VGfb}\left(\frac{g_m}{I_d}\right)^2\left(1+\Omega\ \frac{I_d}{g_m}\right)^2 \qquad (6)$$

Where S_{VGfb} and Ω are fitting parameters obtained from the experimental curve $\frac{S_{Id}}{I_d^2}$ versus I_d, S_{VGfb} is the normalized flat-band voltage noise spectral density, $\Omega = \alpha_{sc}\mu_{eff}C_{ox}$, α_{sc} the Coulomb scattering coefficient, μ_{eff} is the effective mobility and,

$$S_{VGfb} = \frac{q^2\lambda\, kT\, \boldsymbol{N_{it}}}{WL\, C_{ox}^2 f} \qquad (7)$$

Where λ is the tunnel attenuation distance (=0.1 nm in SiO_2).

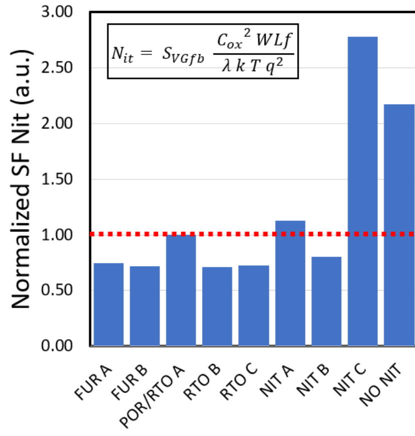


Fig 10: Normalized trap number density N_{it} evolution at 10Hz according to the process split for Source Follower

It is observed that NIT C and NO NIT have higher N_{it} than POR, since they are significantly affected either by interface density degradation or EOT increase. For the others process trials, limited variations are observed compared to POR.

A map is plotted in Fig 11 between T1 threshold population and N_{it}, to evaluate if a correlation exists.

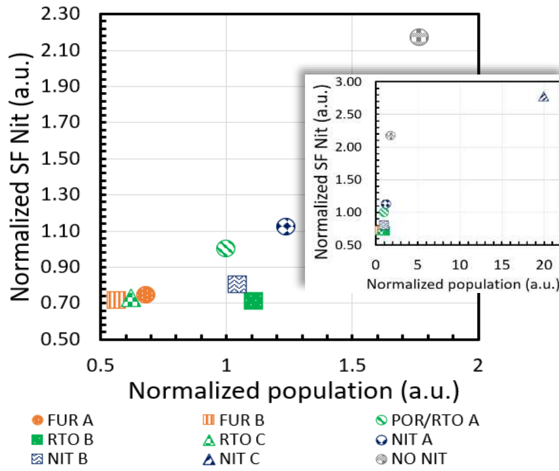


Fig 11: Plot map N_{it} versus RTS pixel population at T1

FUR A, FUR B and RTO C conditions show an improvement for both metrics. However, some GO processes highlight an improvement on N_{it} metrics without improving TN population, such as NIT B and RTO B. N_{it} sampling rate extraction is assumed to be much more limited than TN sampling. It could be part of the discrepancy observed.

Moreover, it can be assumed that some process trials are more uniform or have a better quality, leading to less extrinsic variabilities and N_{it} improvement observed at the same time.

Regarding defect localization, since central MOS size is reduced in SF, it is assumed here that shallow trench isolation (STI) defects could have a more important contribution in N_{it} values but also on RTS population. The effects of the STI edge on low frequency noise characteristics of SF transistors have been studied in some publications [KWO16]. It has been shown that SF transistors with STI edge in contact with the channel show greater RTS amplitudes due to the enhanced trap density induced by STI-induced damage. An additional study is needed to confirm the contributors between edge and central MOS.

V. Conclusion

Throughout this study, it was demonstrated that 3D-stacking technologies open new opportunities to improve RTS pixel in top-tier wafer without influencing the performance of the bottom-tier devices. It is highlighted that oxidizing process tuning is fully part of temporal noise optimization techniques in 3D CIS. Three conditions were clearly identified as best candidate (FUR A, FUR B and RTO C) on RTS point of view for narrow channel SF device, likely sensitive to planar oxide or top sidewall trench interface quality. This optimization could be freely cumulated to other known processes [YEN21]-[KWO13]-[KIM13], design [HAS19] or device approach [KIT22] to limit overall noise of the pixel.

Based on this noise analysis, it is observed that intrinsic defect density value N_{it} and RTS extrinsic temporal noise [WAN06] are not always correlated throughout the different GO processes investigated. Although, for the three best candidates both metrics are likely improved.

In this study, no wafer-to-wafer variability problem is observed between best candidates as not enough wafers/lots have been measured, not allowing us to come out with a better candidate among the three processes mentioned above. However, from a production point of view, RTO processes are often preferred for thin gate oxide growth compared to Furnace ones especially for temperature and oxide uniformity control.

References:

[CHA21] CHAO, Calvin, *et al.* Characterization of Random Telegraph Noises of MOSFET Subthreshold Currents for a 40 nm Process, IISW 2021.
[HA17] HA, Man-Lyun, *et al.* Temporal Noise Improvement Using the Selective Application of the Fluorine Implantation in the CMOS Image Sensor. In: Proceedings of the International Image Sensors Workshop (IISW), Hiroshima, Japan. 2017. p. 32-35.
[HAS19] HASEGAWA, Takuma, *et al.* A new 0.8 µm CMOS image sensor with low RTS noise and high full well capacity. IISW Dig. Tech. Pap, 2019, 1: 24-27.
[HOL07] HOLLAUER, Christian, Modeling of thermal oxidation and stress effects [Dissertation, Technische Universität Wien], 2007.
[HUN90] HUNG, K.K., et al, A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors. IEEE Transactions on Electron Devices, vol. 37, no. 3, p. 654-665, 1990.
[KIM13] KIM, Joo Hyung, *et al.* Fluorine Improvement of MOSFET interface as revealed by RTS measurements and HRTEM. IEEE, 2013
[KIR89] KIRTON, M.J. *et al.* Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/*f*) noise, Advances in Physics, Vol. 35, No. 4, p.367-468, 1989
[KIT22] KITAMURA, Shota, *et al.* Low-Noise Multi-Gate Pixel Transistor for Sub-Micron Pixel CMOS Image Sensors. In: 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits). IEEE, 2022. p. 347-348.
[KWO13] KWON, Hyuk-Min, *et al.* Effects of high-pressure annealing on random telegraph signal noise characteristic of source follower block in CMOS image sensor. IEEE electron device letters, 2013, 34.2: 190-192.
[KWO16] KWON, Sung-Kyu, et al. Effects of shallow trench isolation on low frequency noise characteristics of source-follower transistors in CMOS image sensors, Solid-State Electronics, 2016
[LOP11] LOPEZ, Diana, *et al.* Low-frequency noise investigation and noise variability analysis in high-k/metal gate 32-nm CMOS transistors. IEEE Transactions on electron devices, 2011, 58.8: 2310-2316.
[MAR10] MARTIN-GONTHIER, Philippe, MAGNAN, Pierre. RTS Noise Impact in CMOS Image Sensors Readout Circuit, IEEE International Conference on Electronics, Circuits and Systems, 2009
[NAK21] NAKAZAWA, Keiichi, *et al.* 3D sequential process integration for CMOS image sensor. In: 2021 IEEE International Electron Devices Meeting (IEDM). IEEE, 2021. p. 30.4. 1-30.4. 4.
[SIM92] SIMOEN, E. et al. Explaining the amplitude of RTS noise in submicrometer MOSFETs, IEEE Transactions on Electron Devices, 1992, 39, 422-429.
[TRA93] TRAPP, O. D., *et al.* Semiconductor technology handbook. Technology Associates, 1993.
[WAN06] WANG, Xinyang, *et al.* Random telegraph signal in CMOS image sensor pixels. In: 2006 International Electron Devices Meeting. IEEE, 2006. p. 1-4.
[YEN21] YEN, Wen-Cheng, *et al.* Improvement of Fluorine to Photo Response Non-Uniformity and Random Telegraph Signal of Pinned Photodiode

Exploring Space-Radiation Induced Dark Signal and Random-Telegraph-Signal in a Sony IMX219 CMOS Image-Sensor

Aubin Antonsanti[1,4,5], Jean-Marie Lauenstein[2], Alexandre Le Roch[3], Landen Ryder[2],
Cédric Virmontois[4], Vincent Goiffon[5]
[1] Southeastern Universities Research Association at NASA Goddard Space Flight Center (GSFC), USA
[2] NASA Goddard Space Flight Center, USA/ [3]NASA Postdoctoral Program at NASA GSFC, USA
[4] Centre National d'Etudes Spatiales, Toulouse, France/ [5] ISAE-Supaero, Toulouse, France
Email: aubin.antonsanti@isae-supaero.fr

I. Introduction

Beyond high-performance image sensors embedded in telescopes or scientific instruments, additional cameras are required for satellite orientation, Entry Descent Landing (EDL) sequence, and rover navigation. Star trackers, proximity cameras, and engineering cameras are examples of non-scientific imaging systems where the development cost is far smaller than the critical scientific payload and where the use of Commercial-Off-The-Shelf (COTS) CMOS Image Sensors (CISs) is of great interest. Over the past decade, space applications have seen an increasing number of engineering cameras that have not been specifically developed for space applications at first [1]. New needs have arisen to assist missions with high frame rates and fast data transmission where COST CIS camera modules are preferred candidates.

Therefore, implementing COTS CIS in space missions is a trend that is more likely to keep growing as the number of missions increases. All those new applications will drastically increase the need for long-lifetime cameras, making Radiation Hardness Assurance (RHA) way more critical contrary to previous missions. To meet future mission requirements, the radiation-induced performance degradation of COTS CIS is currently being explored on several CIS technologies.

Both Total Ionizing Dose and Displacement Damage Dose lead to a dark current increase altering the dynamic range as well as creating hot pixels altering the image quality. Some pixels also exhibit a dark current Random Telegraph Signal (DC-RTS), seen as blinking pixels with a time constant in the range of a few seconds, minutes, hours [2], [3]. Such pixels see their dark current randomly and instantaneously switch between two or more discrete dark current levels preventing in-flight calibration and perturbing the normal operation.

This work aims at exploring radiation-induced dark signal and Dark Current Random-Telegraph-Signal in a COTS, micro-meter pitch, backside-illuminated (BSI) CMOS Image Sensor (CIS).

II. Device Information

The device under test (DUT) is a Sony IMX219. The IMX219 is a backside illuminated CIS with 3280 × 2464 pixels and 1.12 μm pitch. The detection layer of the sensor is stacked on another silicon die containing the sensor's ROIC and logic electronics. A Scanning Electron Microscopy (SEM) cross-section is shown in Fig. 1 with the different layers of the optical stack identified. Pixels are arranged in a clover leaf patter [4] where a subgroup of four pinned-photodiodes (PPDs) are connected through Transfer Gates (TG) to a shared Sense-Node (SN). Two subgroups are sharing the same reset (RST) and row select (SEL) transistors. This pattern is commonly employed and allows to use 11 transistors for 8 pixels (1.375 transistors per pixel) as seen in Fig. 2.

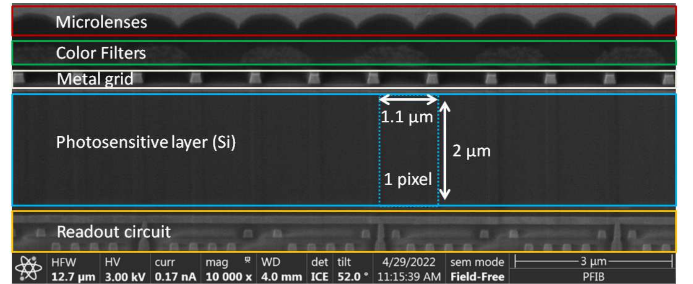


Fig. 1. SEM image of the IMX219 optical stack's cross-section

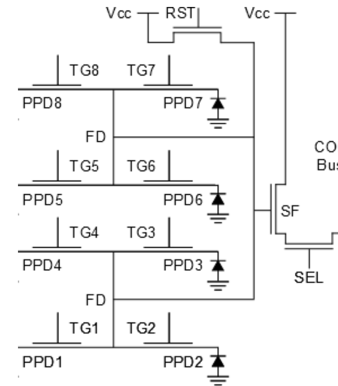


Fig. 2. IMX219 pixels electrical layout

Fig. 3. Images taken with an integration time of 400ms and unitary gain with a 1) pristine; 2) 235 TeV/g(Si) proton irradiated; 3) 1 Mrad(SiO2) gamma irradiated; 4) 2160TeV/g(Si) irradiated IMX219.

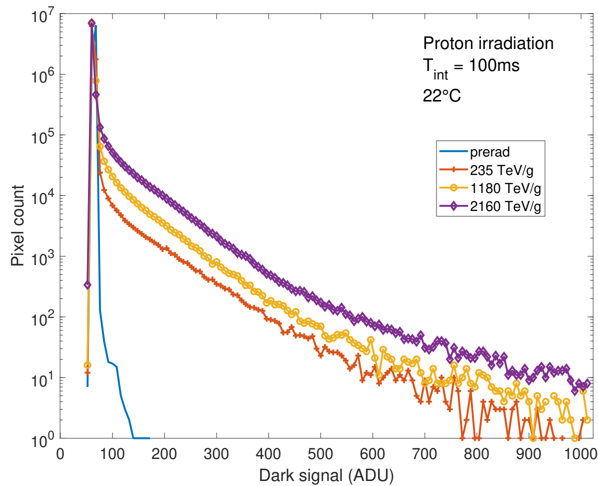


Fig. 4. Histograms of dark signal of proton irradiated IMX219. Proton induced Displacement Damage is responsible for the creation of a tail of hot pixels whose occurrence increases with the total dose.

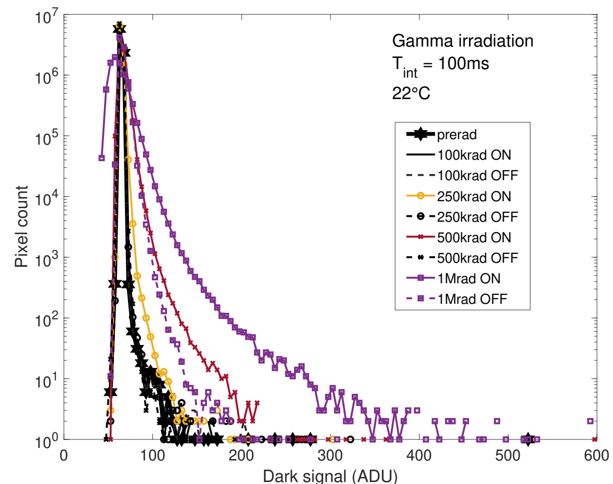


Fig. 5. Histograms of the dark signal of gamma irradiated IMX219. Ionizing radiations are responsible for the widening of the dark signal distributions. The fact that the main occurrence peak isn't shifting towards the high ADU values shows the effect of the on-chip black clamping circuit.

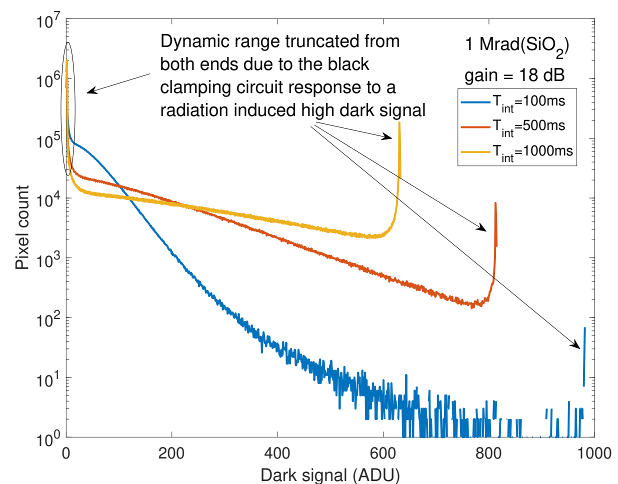


Fig. 6. Effects of the black-clamping circuit on the dynamic range at high TID. The signal histogram is shifted towards low ADU values to compensate for the radiation induced dark signal which significantly increases with the integration time. The correction forces pixels' value to 0 ADU and the saturation level is also reduced, thus diminishing the 10-bit ADC initial dynamic range.

III. Irradiation Details

Two irradiation campaigns have been made. The first used a 62 MeV proton beam at the Light Ion Facility (LIF) located in Université Catholique de Louvain, Belgium. All DUTs were grounded during irradiation at room temperature. The deposited Displacement Damage Dose (DDD) ranged from 235 to 2160 TeV/g (Si). The second used gamma rays at the Radiation-Effect-Facility of the NASA Goddard Space Flight Center. Both grounded and biased DUTs were used and irradiated at room temperature. A thermocouple was used to monitor the temperature of the biased DUT during irradiation. Devices were heating up to 32°C when biased but irradiation didn't cause extra heating. The deposited Total Ionizing Dose (TID) ranges from 10 $\mathrm{krad(SiO_2)}$ to 1 $\mathrm{krad(SiO_2)}$.

All measurements were performed in a climatic chamber whose temperature was set so that the temperature of the DUTs was 22°C when biased.

IV. Results

A. Dark current degradation

Proton-induced displacement damages are responsible for the creation of an exponential dark current tail of hot pixels as seen in Fig. 4 and reported multiple times in previous studies on CIS radiation hardness [5]–[9]. In [5], it was shown that the displacement damage induced dark current degradation on the DUT was following the typical trend with the dose for CIS.

TABLE I
IMX219 DSNU AND READOUT NOISE

Particle	Bias	Dose krad(SiO_2)	DSNU %	Readout noise ADU RMS
ref	-	-	0.66	2.03
γ	gnd	100	0.64	2.03
γ	gnd	250	0.92	2.08
γ	gnd	500	1.39	2.04
γ	gnd	1000	6.23	2.08
γ	on	100	0.78	2.08
γ	on	250	2.06	1.59
γ	on	500	5.72	1.82
γ	on	1000	14.8	2.2
		TeV/g(Si)		
ref	-	-	0.59	1.87
p^+	gnd	235(10 krad)	18.0	2.1
p^+	gnd	1180(50 krad)	37.7	2.27
p^+	gnd	2160(90 krad)	43.3	3.27

However, the study concluded that no TID induced degradation was observed although devices were irradiated up to a TID of $90\,\mathrm{krad(SiO_2)}$.

Fig. 5, displays histograms of dark signal for gamma irradiated devices. It can be seen that there are no obvious changes in the histogram shape bellow $250\,\mathrm{krad(SiO_2)}$ for the biased devices versus bellow $1\,\mathrm{Mrad(SiO_2)}$ for the grounded devices. Above these values, histograms widen with dose, reflecting an increase in the dark current shot-noise. The increase in dark current mean value should be visible in the form of a shift of the peak of maximum occurrence towards high dark signal values. Such a shift isn't visible here due to the sensor's black clamping circuit that shifts the output histogram so that the mean dark signal is coded 64 ADUs. This mean dark signal is evaluated using 16 rows of optically black pixels.

Table I sums up the measured Dark Signal Non Uniformity (DSNU) and readout noise for both the proton and gamma irradiations. The DSNU was evaluated as the standard-deviation of the pixels' dark signal over the array divided by the mean dark signal using an integration time of 100 ms. The readout noise was evaluated as the average standard deviation of individual pixel's dark signal values over 100 frames using an integration time of 100 ms. It can be seen that the DSNU is much lower for the gamma irradiated devices than for the proton irradiated device. This is an expected result since the TID induces an homogeneous degradation of the dark current over the array while DDD will create individual hot pixels [7]. This effect can also be seen on the pictures in Fig. 3.

Although the black clamping can mitigate part of the dark current degradation, the dynamic range of the sensor is still reduced by the increase of the dark current level and shot-noise. As seen in Fig. 6, at high dose and in some specific use cases (low luminosity, high integration time, high gain), the radiation induced dark signal increase will cause the black clamping circuit to shift a lot of the histogram values to 0 ADU and will also reduce the saturation level bellow the maximum value that the 10 bit ADC can code, 1023.

B. Dark current Random Telegraph Signal

Fig. 7 displays an example of the temporal response of an RTS pixel. An edge-detection algorithm [10] allows to extract

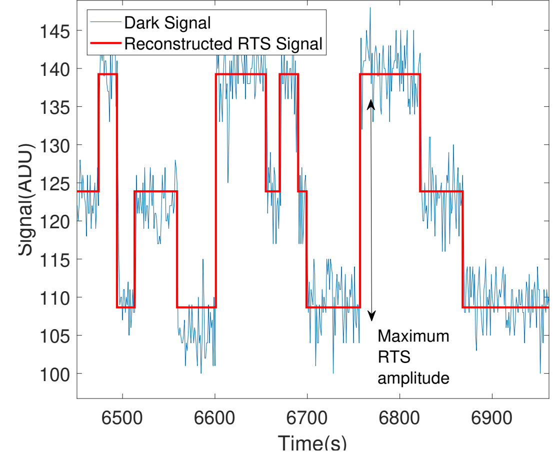


Fig. 7. Temporal evolution of the dark signal of a pixel exhibiting 3 RTS levels. The maximum RTS amplitude is the highest jump between two consecutive discrete levels. All RTS measurements were carried out using an integration time of 100ms and an inter-sample time of 1s. RTS traces are extracted using a sharp edge detection algorithm [10].

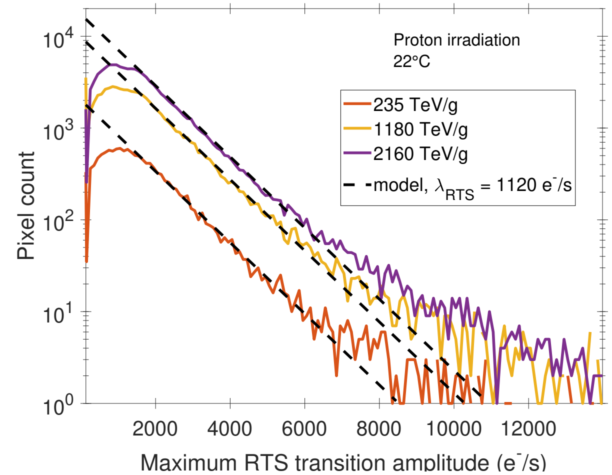


Fig. 8. RTS Maximum transition amplitude histograms of proton irradiated IMX219. The number of pixel exhibiting an RTS behavior increases with the dose. The slope of these exponential distributions is the mean maximum RTS transition amplitude. A slope of 1120 e-/s is found, close to the 1200 e-/s reported in the literature [7] [11].

TABLE II
IMX219 RTS DETECTION

Particle	Bias	Dose krad(SiO_2)	RTS Fraction %	%Multi-level %
γ	gnd	100	0	-
γ	gnd	250	0	-
γ	gnd	500	0.16	0
γ	gnd	1000	2.93	0.94
γ	on	100	0.01	0
γ	on	250	0.99	1.0
γ	on	500	16.2	3.8
γ	on	1000	32.8	9.5
		TeV/g(Si)		
p^+	gnd	235(10 krad)	0.64	23.6
p^+	gnd	1180(50 krad)	3.18	27.1
p^+	gnd	2160(90 krad)	5.14	25

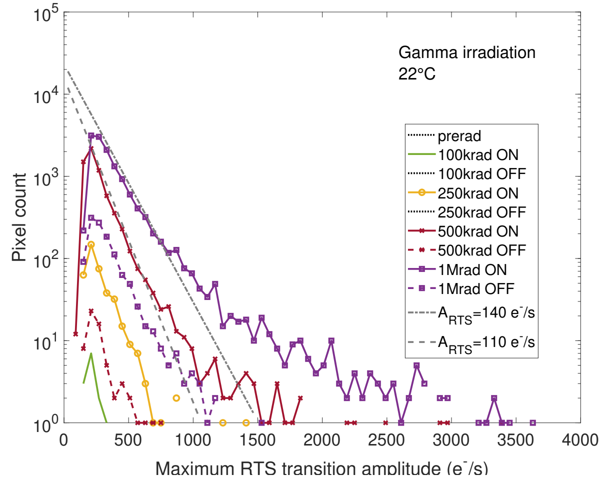


Fig. 9. RTS Maximum transition amplitude histograms of gamma irradiated IMX219. Black dots in the legend indicate dose steps where no RTS pixels where detected. Biasing the device during irradiation strongly increases the number of RTS pixels created.

the highest transition between two levels, the number of RTS level as well as the number of transitions. Black-clamping is not an issue when extracting RTS amplitudes as it can be seen as an offset that should not vary from frame to frame. Prerad RTS detection revealed less than 4 RTS pixels per milion pixel.

Proton-induced RTS maximum transition amplitudes are exponentially distributed (Fig. 8). The experimental RTS maximum transition amplitude distributions' associated exponential slopes values are well in line with the values found in the literature ($A_{\mathrm{RTS}} \approx 1200$ e-/s at $\approx 22\,°\mathrm{C}$) for a wide range of image sensor technology nodes, designs, or pixel size [5], [10], [11]. This result strengthens the idea of a universal behavior of displacement damage-induced RTS in silicon.

Table II shows the fraction of RTS pixels detected and the fraction of RTS pixels exhibiting more than two RTS levels after the different irradiations. For the proton irradiations, it has been shown in [5] that both quantities were significantly smaller in the DUT than in CIS with a larger pitch. This reduction of the fraction of RTS and of multilevel RTS has been directly linked to the reduction of the pixels' sensitive volume.

For the TID induced RTS pixels after gamma irradiation, it can be seen in Fig 9 that the maximum RTS amplitudes are mostly exponentially distributed and of a much lower than the displacement damage induced RTS pixels. The exponential slope of ≈ 110e-/s matches the literature [7].

Both proton and gamma induced maximum RTS amplitudes histograms deviate from the exponential behavior at high dose. This is not a commonly reported result and local Electric-Field-Enhancement was proposed in [5] as a phenomenon that could explain this deviation.

Table II also shows that the fraction of RTS pixel increases faster when the device is biased during gamma irradiation. For the biased devices, the creation of RTS pixels accelerates significantly after $250\mathrm{krad}(\mathrm{SiO_2})$. It can be seen that, comparatively to displacement damage induced RTS pixels, TID induced RTS pixels are mostly exhibiting two RTS levels.

V. Conclusions

Proton irradiations showed that the DUT was following the typical trend for dark-current and RTS degradation for CIS. The reduced pixel pitch induced a decrease of the fraction of pixels disclosing an RTS behavior when comparing to larger pitch CIS.

Gamma irradiations revealed that the DUT has a very good tolerance to TID up to 250 krad. Biasing the DUT during irradiation has a strong negative impact on the TID induced degradation of both the dark signal and RTS behavior.

A deviation of the maximum RTS transition amplitude distributions from a purely exponential behavior is observed in both the proton and gamma irradiations. Local Electric-Field-Enhancement was proposed as a first hypothesis on the origin of this behavior in [5], due to an observed shift of the RTS amplitudes activation energies from the mid-gap. The increase in dopants gradient profiles resulting from the submicrometer pixel pitch reduction trend imposed by the smartphone camera market is also supporting this hypothesis [12].

The response to cumulative dose of the IMX219 is very promising for a use as an engineering/proximity camera in space applications, where the dose rarely exceed the 100 krad range. Cumulative dose might however not been the most challenging aspect in assessing the radiation hardness of such 3D-stacked CIS. The device susceptibility to Single-Event-Effects; such as transistor latchup or functional interrupt; might be the real bottleneck because of the presence of the ROIC and logical die stacked under the detection layer.

References

[1] J. Maki *et al.*, "The Mars 2020 Engineering Cameras and microphone on the perseverance rover: A next-generation imaging system for Mars exploration," *Space Sci. Rev.*, vol. 216, pp. 1–48, Nov. 2020.

[2] I. H. Hopkins and G. R. Hopkinson, "Random telegraph signals from proton-irradiated CCDs," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1567–1574, Dec. 1993.

[3] I. Hopkins and G. Hopkinson, "Further measurements of random telegraph signals in proton irradiated CCDs," *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6, pp. 2074–2081, Dec. 1995.

[4] E. R. Fossum and D. B. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 3, pp. 33–43, May 2014.

[5] A. Antonsanti *et al.*, "Probing dark current random telegraph signal in a small pitch vertically pinned photodiode cmos image sensor after proton irradiation," *IEEE Transactions on Nuclear Science*, vol. 69, no. 7, pp. 1506–1514, 2022.

[6] J.-M. Belloir *et al.*, "Pixel pitch and particle energy influence on the dark current distribution of neutron irradiated CMOS image sensors," *Opt. Express*, vol. 24, no. 4, pp. 4299–4315, Feb. 2016.

[7] V. Goiffon, "Radiation effects on CMOS active pixel image sensors," in *Ionizing Radiation Effects in Electronics: From Memories to Imagers.* Boca Raton, FL, USA: CRC Press, 2015, pp. 295–332.

[8] C. Virmontois, V. Goiffon *et al.*, "Similarities between proton and neutron induced dark current distribution in CMOS image sensors," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 927–936, Aug. 2012.

[9] C. Virmontois *et al.*, "Dark current random telegraph signals in solid-state image sensors," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4323–4331, 2013.

[10] V. Goiffon, G. R. Hopkinson *et al.*, "Multilevel RTS in proton irradiated CMOS image sensors manufactured in a deep submicron technology," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2132–2141, Aug. 2009.

[11] C. Virmontois *et al.*, "Dark Current Random Telegraph Signals in Solid-State Image Sensors," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4323–4331, Dec. 2013.

[12] M. Uchiyama *et al.*, "A 40/22nm 200mp Stacked CMOS Image Sensor with 0.61um Pixel," in *2021 International Image Sensor Workshop (IISW)*, Online Conference, 20-23 Sept 2021, Art. no. R02.

Low Temperature Lag-induced FPN of Dual Transfer Global Shutter Pixels under Low Illumination Condition

Xiaoliang Ge[1], Yangyu Guo[2], Yang Liu[2], Ning Cui[2], Tadashi Imoriya[3],
Masafumi Tsutsui[3], Masakatsu Suzuki[3], Assaf Lahav[1]
[1]Gpixel Inc, Hangzhou, China; [2]Gpixel Inc, Changchun, China;
[3]Tower Partners Semiconductor Co. Ltd., Uozu, Japan
Email address: xiaoliang.ge@gpixel.com

***Abstract* — This paper presents the lag-induced Fixed Pattern Noise (FPN) of dual transfer global shutter pixels. Instead of focusing on analyzing the inter-frame charge smear between bright and dark frames, we investigate the black dots pattern artifact arising from the lag along the charge transfer path of the pixel. The presence of this image artifact in a CMOS image sensor (CIS) result in a poorer FPN for still images application. We explore the behavior of this FPN under low illumination and low temperature conditions, explain the mechanism of these lag artifacts, and further discuss the experiments that have been undertaken to enhance the charge transfer efficiency of the pixel.**

I. INTRODUCTION

In recent times, global shutter pixels [1] have gained significant popularity and are being employed in various applications. Among them, the Intelligent Traffic Systems (ITS) are particularly intrigued by this global shutter pixel technology for its capability to track fast-moving vehicles without any motion distortion. This feature facilitates the CMOS image sensors (CIS) to provide accurate and reliable data for traffic analysis and evaluation, thus, allowing the ITS to gain insight into traffic trends and help improve the traffic flow in their perspective area. Nonetheless, this ITS application necessitates an image sensor that is able to perform well in a wide range of circumstances. For instance, the camera must be able to offer clear images and ensure a high-level performance in low light conditions and extremely cold temperatures, such as -40°C. In this paper, we evaluate the performance of a 3.8um pixel pitch charge domain global shutter pixel in this kind of challenging conditions, with a focus on assessing the lag-induced FPN, and discuss the improvement trials that have been attempted.

II. MECHANISM AND CHALLENGE

The charge domain dual transfer global shutter pixel schematic and operating timing are shown in Fig. 1. In this pixel, TX1 functions as a transfer gate from the Pinned-Photodiode (PPD) to Memory Node (MN), as well as acts as a storage-gate over MN. TX2 is served as a transfer gate from the MN to the Floating Diffusion (FD) node. Therefore, the incomplete charge transfer may not only take place on the typical path from PPD to the MN, but also from the MN to the FD.

Fig.2 (a)-(b) shows the captured contrast-enhanced images when the die temperature is at -40°C and 0°C. We could observe that the black dots appear in the region where the median signal level is below or around 100e-. It can be considered that the pixels with lag lost electrons during the charge transfer, resulting in darker signals and showing as black dots pattern. These black dots are camouflaged by the photon shot noise under strong light conditions, yet they become more visible when the illumination is faint, leading to a higher FPN spec. Therefore, under weak illumination conditions, the number of black dots and their associated FPN value can be leveraged to study the impact of lag on image quality.

Fig. 3 shows the signal histogram across three different temperatures, -40°C, -20°C, and 0°C. It can be observed that when the temperature decreases, the number of tail pixels over the lower signal side increases, leading to a higher FPN. This phenomenon is in line with the findings between temperature and thermionic emission charges that jump across the charge transfer potential barrier [5-6], which is expressed as:

$$Q = AT^2 exp(-X_0/kT) t_{TX\text{-}on}, \qquad [1]$$

where A is the Richardson constant, T is the temperature, X_0 is the barrier height, k is the Boltzmann constant, and $t_{TX\text{-}on}$ is the TX1/TX2 transfer time. When the internal

potential of the PPD is close to the potential barrier of charge transfer, the thermionic emission takes over the transfer process, and the amount of charge that can cross the barrier is contingent upon the environment temperature. As the temperature decreases, fewer of the charges can pass through the barrier, causing a more pronounced black dots pattern on the image. This mechanism poses a challenge in terms of achieving full charge transfer under low temperature conditions when operating this global shutter pixel.

What's more, it is noteworthy that the TX2 of this pixel works in a row-by-row manner. When a high frame-rate request is made, the TX2 switch-on period can be as short as a few hundred nanoseconds, due to the limitation of the row time. This tight transfer time presents a difficulty for complete charge transfer between MN, TX2, and FD in the design of this charge domain global shutter pixel [4].

To address these challenges, several characterizations have been done to analyze the impact of lag-induced FPN, and various design strategies have been proposed and applied in the development of this charge domain global shutter pixel.

III. CHARACTERIZATION RESULTS

We evaluated the lag-induced FPN artifact by setting up the sensor in a way that the image plane could be uniformly illuminated with a light source. The illumination level and the exposure time were adjusted to ensure that the median signal reaches 100 e-. The sensor was operated at the frame rate of 65fps and 8 frame images from the pixel-array active region were obtained consecutively for statistical analysis.

Fig. 3 shows signal histograms of the die temperature under -25°C with different TX1/TX2 high voltage and charge transfer time. It can be observed that a shorter TX1 transfer time (Fig.3 (a)) and a lower TX1 switch-on voltage (Fig.3 (b)) result in more lag-induced black dots. This indicates that there is a potential hump might be present in the PPD-TX1 overlap region (Fig.4 (a)) and an edge barrier appearing on TX1 (Fig.4(b)).

Besides, the number of black dots drops as the TX2 transfer time becomes longer (Fig.3 (c)), while the number remains the same for different TX2 switch-on voltages (Fig.3 (d)). This implies that the charge transfer speed in MN is not high enough (Fig.4(c)) and a surface potential dip appears under TX2 (Fig.4(d)).

IV. IMPROVEMENT AND MEASUREMENT RESULTS

Based on the study of the measurement results and TCAD simulation, optimized process splits have been proposed to improve the charge transfer performance. This optimization involves the Vpin adjustment on the PPD, electric field enhancement in the MN, and the surface potential dip flattening under TX2.

Fig. 5 (a) and (b) show the TCAD simulation results of the electrostatic potential and electric field in the MN with different additional implants. It can be observed that the electric field is enhanced with this additional n implant. Apart from that, as demonstrated in Fig.5 (c) and Fig.5 (d), the utilization of an extra implant beneath TX2 is successful in eliminating the surface potential dip and enhancing the electric field.

Fig. 6 shows the results of the experiment both at the bench-level and the wafer-level of the new DOE lot. These measurements are done with the same settings. The DOE#4 has the best results which can be explained that two times higher electric field is applied on MN combined with the optimized conditions on this split process.

V. CONCLUSIONS

This paper describes the lag-induced FPN of dual transfer global shutter pixels under low temperature and low illumination level. We investigate the behavior of this type of FPN, the causes of these lag effects, and further analyze the simulation and experiments that have been done to increase the charge transfer efficiency of the pixel.

Reference

[1] W. Gao, et al., "Photodiode Barrier Induced Lag Characterization Using a New Lag versus Idle Time Methodology", *IISW*, June 2017.

[2] L. Anzagira, et al., "Lag-Induced Image Artifacts in Still Imaging with CIS", *Electronic Imaging*, 2018.

[3] E. Fossum, et al., "Charge Transfer Noise and Lag in CMOS Active Pixel Sensors", *IISW*, June 2003.

[4] M. Tsutsui, et al., "Development of Low Noise Memory Node in a 2.8um Global Shutter Pixel with Dual Transfer", *IISW*, June 2017.

[5] E. A. Irene, et al., "Thermionic emission model for the initial regime of silicon oxidation", *Appl. Phys. Letter*, 51:767, 1987.

[6] L. Bonjour, et al., "Experimental Analysis of Lag Sources in Pinned Photodiodes", *IEEE Electron Device Letters*, vol.33, no.12, pp.1735-1737, 2012

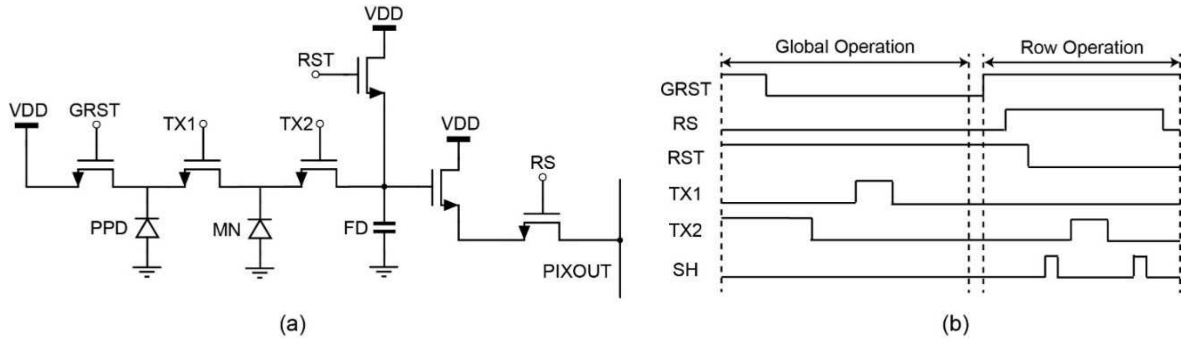


Fig. 1 Dual transfer charge domain global shutter pixel structure (a) Pixel circuit schematic; (b) Timing diagram.

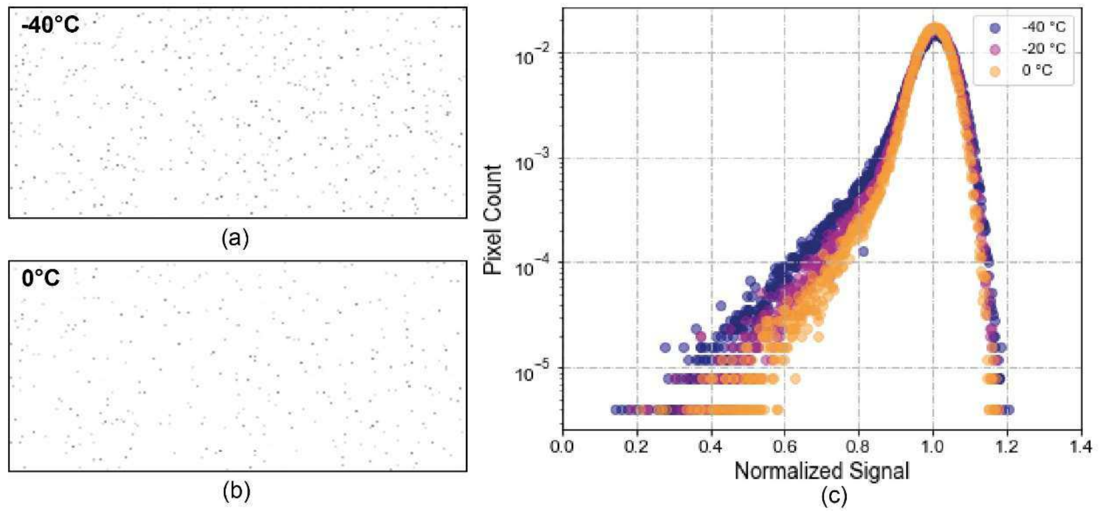


Fig. 2 Contrast-enhanced images under (a) -40°C; (b) 0°C; and (c) the normalized histogram across different temperatures.

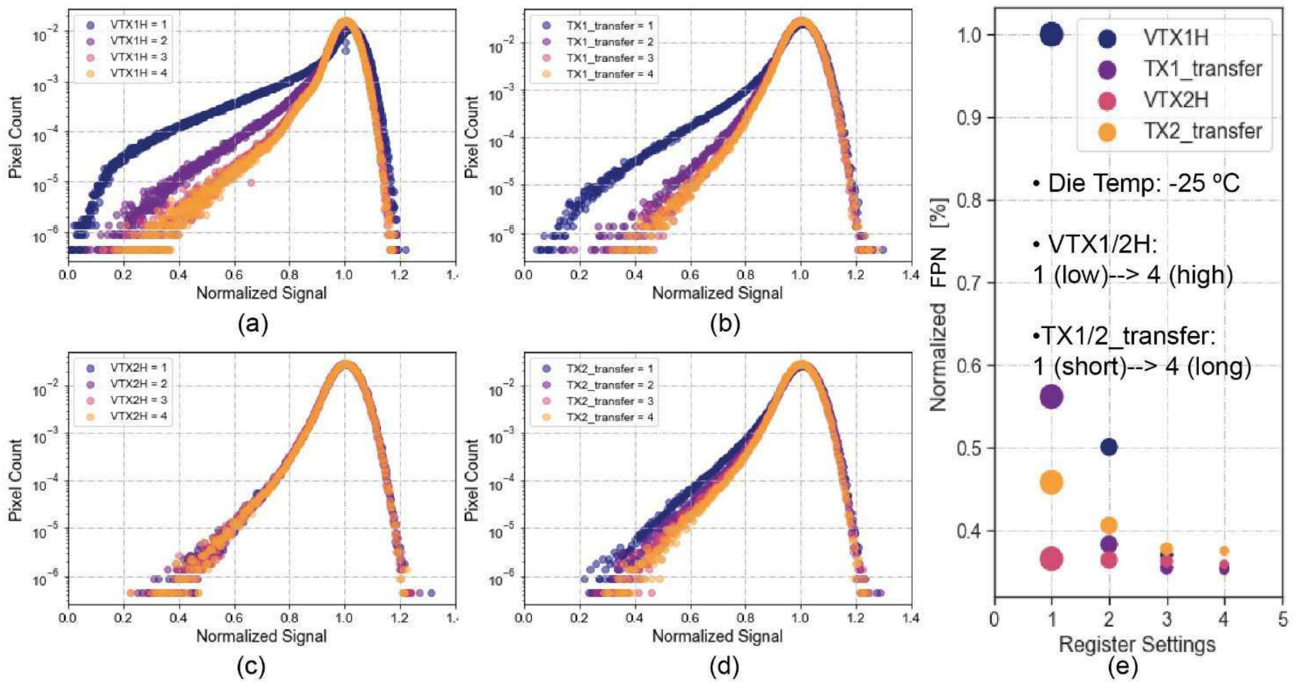


Fig. 3 Signal histograms at -25°C with TX1/ TX2 high voltage and charge transfer time @ mean signal = 100e-

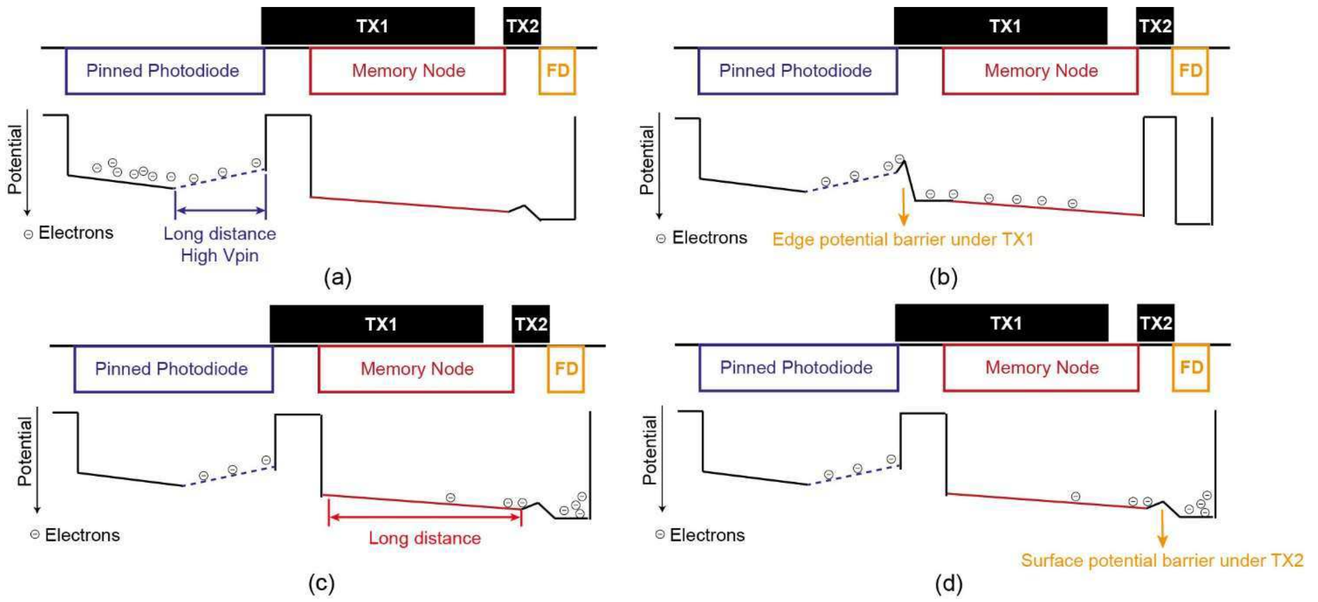


Fig. 4 Barrier locations (a) PPD; (b) TX1; (c) MN; (d) TX2.

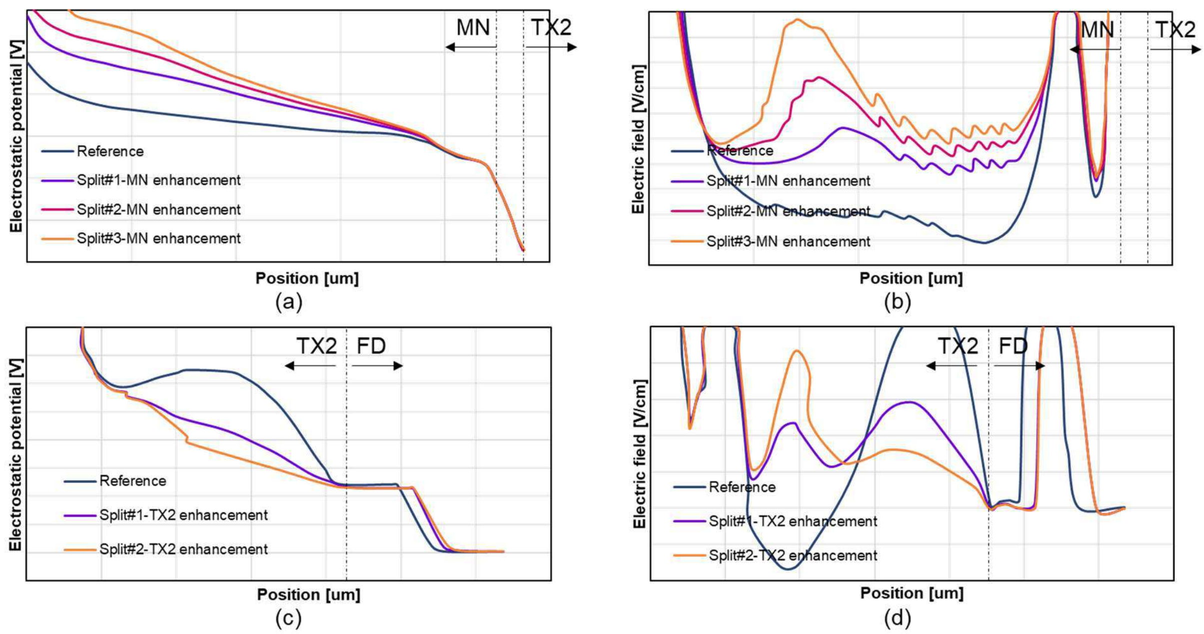


Fig. 5 MN enhancement split (a) Electrostatic potential; (b) Electric field; and TX2 enhancement split (a) Electrostatic potential; (b) Electric field;

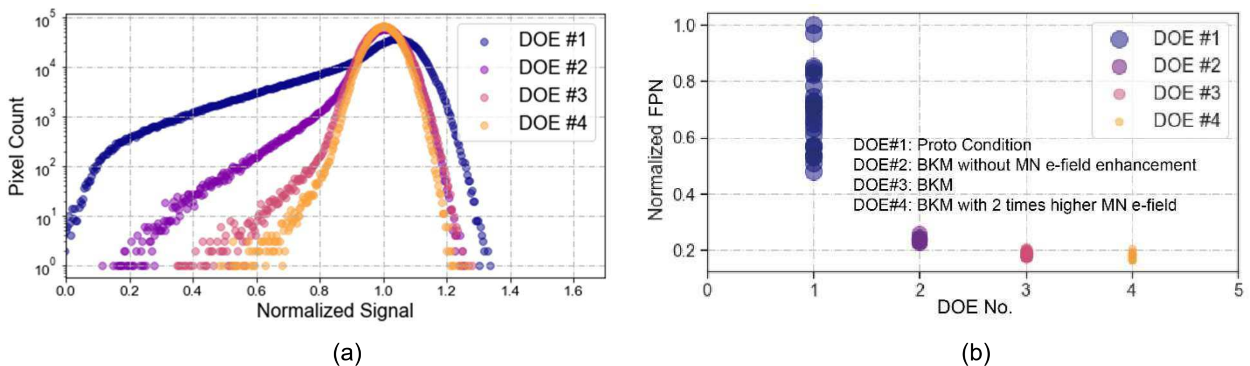


Fig. 6 (a) Signal histogram (measured at bench level); (b) Normalized PRNU (measured at wafer level)

Reduction of RTS noise by optimizing fluorine implantation in CMOS image sensor

Sungyong You, Juhee Lee, Dongmo Im, Sungsoo Choi*, Taeheon Lee, Sanghoon Lee, JuEun Kim, Kyumin Lee, Soojin Hong, Jihee Yang, Sumin Jung, Hyeji Choi, Hyunchul Kim and Chang-Rok Moon

Semiconductor R&D Center, Samsung Electronics Co. Hwasung-City, Gyunggi-do, 18848, Republic of Korea.
*Corresponding Author: sungsoo.choi@samsung.com

Abstract— In-pixel source follower transistors in CMOS image sensors play an important role in their noise characteristics. As the pixel shrink continues due to the demand for high resolution in the mobile market, the SF transistors must also become smaller. Despite the limited size of SF gates, one of the ways to prevent the degradation of noise performance is to improve the interface traps between Si and SiO_2 in the gate oxide. Additionally, RTS noise caused by these traps dominates the overall noise performance in small-pitch, high resolution CISs. In this study, we present a method to improve the RTS noise by optimizing fluorine implantation process for the SF gate. To determine the effect of the fluorine implantation on the noise performance, we fist present the experiments with various implant doses. We also presented an evaluation of the side effect of too high implantation dose and the potential for additional noise reduction by preventing the diffusion of fluorine atoms out of the gate oxide, which can occur through subsequent thermal processes.

Keywords—CMOS Image Sensors, Fluorine implantation, Source follower amplifiers, Random Telegraph Signal Noise, RTS,

I. INTRODUCTION

In CMOS image sensors (CISs), random telegraph signal (RTS) represents a noise source that causes random variations in output voltage over time [1]. The RTS noise is caused by the random trapping and de-trapping of charge carriers in the gate oxide layer resulting in threshold voltage fluctuations [1]. The RTS noise can degrade the image quality of CISs by causing image artifacts and have a significant impact on the performance of CISs in low light conditions [1].

As pixel pitch decreases, recent studies have demonstrated that RTS noise introduced by traps located at the Si-SiO2 interface of the source follower (SF) amplifiers dominates the noise performance of CISs [1,2]. On the other hand, the SF gate area has been the bottleneck of pixel shrinkage while the demand of smaller CISs with more resolutions kept on growing with the expansion of the mobile market [3]. As a result, the interface trap density has become a primary source of noise performance in small-pitch, high resolution CISs.

Fluorine implantation is commonly applied to improve the RTS noise by reducing the interface trap density [4]. Fluorine ions can passivate the traps in the gate oxide layer, which reduces the number of traps available to capture charge carriers and improves the electrical properties of SF transistors [4]. However, the use of fluorine ions must be carefully controlled to maximize RTS noise reduction and avoid side effects for the following reasons.

First of all, high-dose fluorine implantation can increase the gate oxide thickness by introducing excess fluorine atoms into the oxide layer [2]. When the fluorine atoms are introduced into the oxide layer, they can bond with the silicon atoms in the oxide layer to form silicon-fluorine bonds. Once the interface is saturated with the silicon-fluorine bonds, the Si-O bonds in the bulk oxide layer are broken by fluorine and the oxygen diffuses towards the interface to oxidize additional silicon as illustrated in Figure 1 [2]. Also, it is known that increased gate oxide thickness can lead to deterioration of RTS noise characteristics [5]

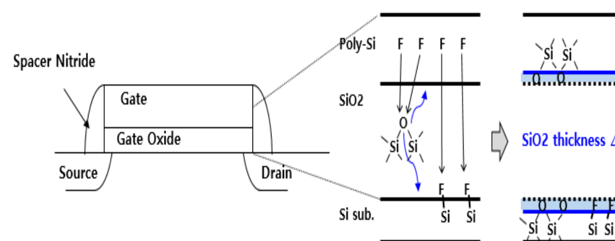


Fig 1. Schematic diagram of a SF transistor (left) and fluorine effects on SiO_2 (right)

Second, the net fluorine concentration in the gate oxide layer, which is responsible for the passivation of interface traps, may decrease due to out-diffusion by the post-thermal processes [6]. As the gate size decreases, fluorine diffusion to the gate edge is the main cause of the decrease in net fluorine concentration [6].

The paper is organized as follows. We first present a typical gate fabrication process and experiments using different fluorine doses and process sequences. We also describe how to measure interface trap density, electrical gate oxide thickness, and RTS noise. Finally, we propose optimized fluorine implantation conditions that result in the most RTS noise reduction without adverse effects.

II. METHODS

The fabrication of the SF amplifier used in the experiments is a general polysilicon gate fabrication process. Gate and field oxide films are grown, polysilicon is deposited on the surface of the oxide films, and then patterned. The polysilicon gate is oxidized, then nitride sidewall spacers are formed and source-drain regions are ion-implanted.

Fluorine implantation is processed prior to formation of the nitride sidewall spacers with different implant doses, and interfacial trap density, gate oxide thickness and RTS noise are quantified. In addition, the fluorine implantation is performed twice to confirm the side-effects of excessive fluorine dose. Finally, in order to investigate the degree of RTS noise reduction according to the presence or absence of the diffusion barrier., an additional experiment is conducted on the fluorine implantation after forming the nitride sidewall spacers.

We use a charge pumping method to quantify the interface state density of the gate oxide layer. The charge pumping method is based on the idea that interface traps can capture and release charges by applying a periodic voltage to the gate of the transistor. The charges trapped in the interface traps result in a shift in the threshold voltage of the transistor, which can be measured as a change in the drain current (Icp). By measuring the change in the drain current as a function of the gate voltage, it is possible to calculate the density of the interface traps in the gate oxide layer.

We use a high-frequency capacitance-voltage (HF-CV) measurement method to obtain the electrical gate oxide thickness (Tinv). The HF-CV method is a technique used to measure the capacitance of a transistor as a function of the voltage applied to its gate at high frequencies. Measurements can provide information about interface density of states, oxide thickness, and other key parameters that can affect a transistor's performance.

For RTS noise measurements, we take two consecutive image frames under dark conditions with high analog gain. Then we plot the pixel-by-pixel output difference on a histogram. In addition, the RTS noise is obtained by counting the number of pixels that differ by more than a certain standard in parts-per-million (ppm) units.

III. RESULTS AND DISCUSSION

During the fabrication process, fluorine atoms are first introduced via ion implantation into the polysilicon and diffused into the gate oxide after annealing, as shown by the SIMS measurements in Figure 2(a). Also, Figure 2(b) shows that 1.6 times more fluorine atoms exist in the gate oxide film when the fluorine implantation process is performed twice than the standard condition. This result indicates that the more fluorine atoms implanted into the polysilicon, the more fluorine atoms can be located in the oxide layer after annealing to passivate more traps on the interface surface.

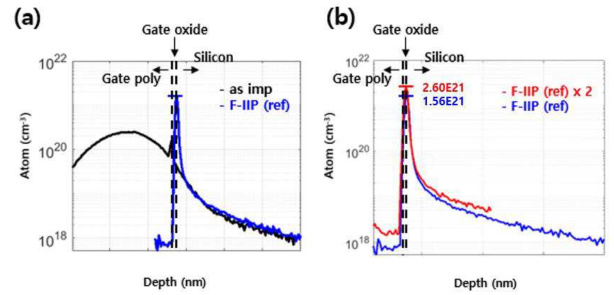


Fig 2. SIMS fluorine profiles. (a) Fluorine dose profile before (black line) and after anneal (blue line) (b) Comparison of fluorine profiles for once (blue line) and twice implantations (red line).

To confirm the above result, we performed CP measurements with different fluorine doses as describe in Methods section. Figure 3(b) shows that Icp decreases with increasing the dose of fluorine implantation. It indicates that interfacial properties appear to improve with higher dose of fluorine implantation. The HF-CV measurements show that the gate oxide capacitance decreases with increasing fluorine implantation doses, as shown in Figure 3(a). This result represents the actual increase in gate oxide thickness as mentioned in the introduction section.

Interfacial properties and gate oxide thickness are one of the key parameters for RTS noise characteristics as described in the equation in Figure 3. Therefore, RTS noise measurements were performed with different implant dose and we found that the improvement of interfacial properties (i.e. Nit) has a more dominant effect on the RTS noise than the increase in gate oxide thickness (Tinv) caused by fluorine implantation. As results, we were able to reduce RTS noise about 20% by increasing fluorine implantation dose, as shown in Figure 4.

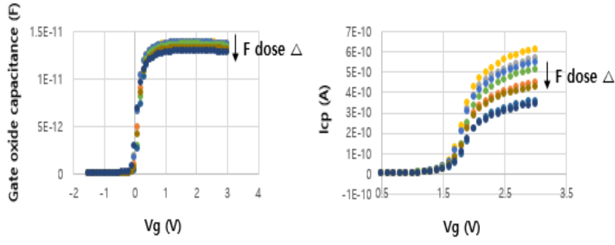
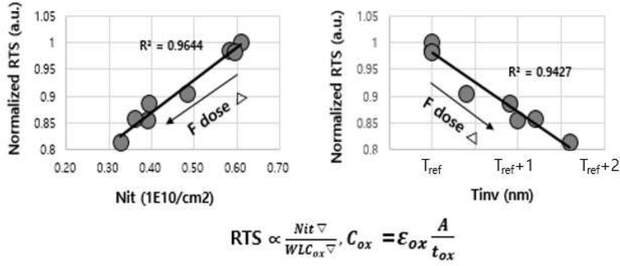


Fig 3. Results of charge pumping (left) and high-frequency capacitance-voltage measurements (right) as a function of fluorine implantation doses.



$$RTS \propto \frac{Nit\triangledown}{WLC_{ox}\triangledown}, C_{ox} = \varepsilon_{ox}\frac{A}{t_{ox}}$$

Fig 4. Correlation between RTS noise and gate oxide properties according to different fluorine implantation. In the right figure, T_{ref} represents thickness of inversion layer at the interface between the silicon and silicon oxide (T_{inv}) when F-IIP is not applied. Ref+1, Ref+2 indicate T_{inv} that is 1 and 2 greater than the T_{ref}, respectively.

To determine the side effects of high-dose fluorine implantation, we also performed fluorine implantation twice after gate poly-silicon deposition as described in Methods section. Then, we found that high-dose fluorine implantation caused a large number of gaseous bubble defects in silicon oxide.

This is because fluorine ions can react with the silicon atoms in the oxide to form SiF4 gas, which can create gaseous voids or bubbles as shown in Figure 5. The process typically begins with implantation of fluorine ions into the silicon oxide, which can damage the lattice structure of the oxide layer. During the post annealing steps, the fluorine ions can react with the silicon atoms in the oxide to form SiF4 gas. The SiF4 gas can then accumulate in the oxide, forming gaseous bubbles. As a results, it was shown that the fluorine implantation dose could not be continuously increased due to the side effects mentioned above.

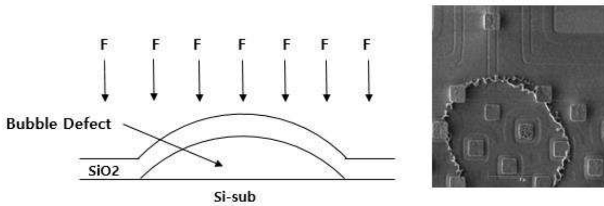


Fig 5. Bubble defects inside the surface oxide under the high dose fluorine implantation condition.

Due to the above bubble defects, there is a limit to increasing the fluorine implantation dose, so another method to improve RTS reduction with a limited fluorine implantation dose is needed. Therefore, we move the fluorine implantation process step after the nitride sidewalls spacers to use the nitride spacer as diffusion barrier. As a result, we expected to increase the net fluorine concentration in the gate oxide layer by minimizing the out-diffusion of fluorine atoms at the gate edge, as described in Methods section. The results show an additional 4% improvement in RTS noise reduction when nitride spacer formation is followed by fluorine implantation. This indicates that retained fluorine concentration increased as illustrated in Figure 6. Finally, we were able to reduce the RTS noise in our device by approximately 14% by optimizing the fluorine implantation process, without side effects on the gate oxide layer, as illustrated in Figure 6.

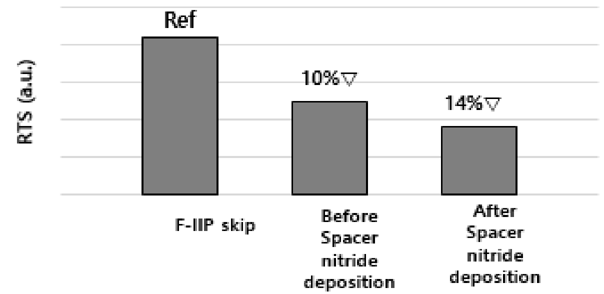


Fig 6. RTS noise results according to the different fluorine implantation process sequence.

IV. Conclusion

We conducted a study on the mechanism of fluorine implantation in order to improve RTS noise by reducing interface traps in the gate oxide layer of SF transistors. We found that RTS noise improved with increasing the dose of fluoride implantation. However, we confirmed that the dose could not be continuously increased due to the bubble defect, and RTS noise could be improved by about 10% compared to the case where fluorine implantation was not applied. We also found that in a limited dose of fluorine implantation, RTS noise could be further improved by 4% by using the nitride spacers used as diffusion barriers to reduce the diffusion of the fluorine atoms to the gate edge. This achievement can allow further pixel shrink for the high-resolution CISs without the inevitable noise degradation at a limited SF sizes.

REFERENCES

[1] Wang, Xinyang, et al. "Random telegraph signal in CMOS image sensor pixels." 2006 International Electron Devices Meeting. IEEE, 2006.

[2] Kim, Joo Hyung, et al. "Fluorine improvement of MOSFET interface as revealed by RTS measurements and HRTEM." 2013 IEEE Radio and Wireless Symposium. IEEE, 2013.

[3] Park, Sungbong, et al. "A 64Mpixel CMOS Image Sensor with 0.50um Unit Pixels Separated by Front Deep-Trench Isolation." 2022 IEEE International Solid-State Circuits Conference (ISSCC). Vol. 65. IEEE, 2022.

[4] Wright, Peter J., and Krishna C. Saraswat. "The effect of fluorine in silicon dioxide gate dielectrics." IEEE Transactions on Electron Devices 36.5 (1989): 879-889.

[5] Wong, S. P., et al. "Effects of high dose fluorine implantation into silicon." Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms 67.1-4 (1992): 481-485.

[6] Fujii, Shuntaro, et al. "Impacts of Depth and Lateral Profiles of Fluorine Atoms in Gate Oxide Films on Reliability." 2021 IEEE International Reliability Physics Symposium (IRPS). IEEE, 2021.

[7] Xiao, Yujie, et al. "Optimizing Photoresist Strip to reduce fluorine outgassing causing bubble defect." 2022 33rd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC). IEEE, 2022.

Dark Current Compensation of a CMOS Image Sensor by Using In-Pixel Temperature Sensors

Accel Abarca[1,2], Albert Theuwissen[1,3]
[1]Delft University of Technology, Electronic Instrumentation Lab., Mekelweg 4, 2628CD, Delft, The Netherlands.
[2]now with INL – International Iberian Nanotechnology Lab., Avenida Mestre José Veiga s/n, 4715-330, Braga, Portugal; accel.abarca@inl.int
[3] Harvest Imaging, Witte Torenwal 8E, app. 2.1, 3960 Bree, Belgium; albert@harvestimaging.com

***Abstract*—In this paper a novel technique to compensate for dark current of a CMOS image sensor (CIS) by using in-pixel temperature sensors (IPTSs) is presented. The IPTSs are integrated in the same layer as the image pixels and use the same readout circuit as the pixels. Therefore, the real temperature variations in the pixel array can be measured as well as the thermal distribution across the array. The dark current compensation can be carried out locally by creating a dark reference frame from the in-pixel temperature measurements and the temperature behavior of the dark current. The artificial dark reference frame is subtracted from the actual images to reduce/cancel the dark signal level of the generated images.**

Keywords—CIS, in-pixel temperature sensors, dark current compensation

I. Introduction

Over the last few decades the growing market for portable devices has pushed the CMOS active pixel sensor (APS) industry to rapidly improve CMOS technology performance. The wide use of the APS is related to its high integrability, low cost, and low power consumption [1], [2]. CMOS APS image sensors are widely used in a variety of applications, ranging from medical to military. The dark current is one of the key parameters which characterizes the performance of the APS, where a low dark current is preferred. However, the continuous downscaling of CMOS technology to sub-micron sizes while keeping dark current levels low is a challenge [3], [4]. The dark current is one of the major components of fixed pattern noise (FPN) in CIS as well as an important contributor to temporal random noise [5]. Large dark current in a CIS leads to high noise, non-uniformity, and a reduced dynamic range [6]. The dark current exhibits a linear behavior over exposure time, and an exponential behavior over temperature. In fact, the dark current doubles every ~5-10 °C [7], [8], [9]. A conventional technique for dark current compensation is to take a dark reference frame during the picture acquisition at a certain exposure time with closed mechanical shutter, and subtract this dark frame from the images. However, the temperature must be kept constant during the acquisition to avoid any dark current variation. Also, some cameras (such as mobile phones) do not have a shutter, therefore obtaining the dark reference frame is not possible. A technique to compensate for dark current has been proposed by [10]. In [10] the compensation involves using a Miller differential amplifier with the non-inverting input connected to a dummy shielded photodiode and the inverting input connected to an active photodiode. The offset (dark current level) provided by the dummy shielded photodiode is sampled and subtracted from the video signal (including the dark current from the active photodiode) compensating for the dark current of the active pixel. However, the mismatch between the active photodiode and the dummy shielded photodiode is not addressed in [10]. Another technique has been proposed by [11], where the dark current of hundreds of hot pixels is used as a temperature indicator across the pixel array. The dark current of the hot pixels has been calibrated in a temperature range of -40 °C and 8 °C, and it is used to predict the dark current level of the rest of the pixels. However, the compensation is limited to the temperature range of -40 °C and 8 °C and no information about the accuracy of the hot pixels acting as temperature sensors is provided.

We propose using the absolute temperature information provided by the in-pixel temperature sensors (IPTSs) to create a dark reference frame at a particular exposure time to compensate for dark current across the pixel array without the need of a mechanical shutter and without the request for constant temperature. The in-pixel temperature sensors have been proposed in our previous works, where the use of parasitic substrate bipolar temperature sensor pixel (Tixel) [12], and the use of the imaging pixel itself as a temperature sensor [13], [14] have been shown and proved. In this paper, the CIS and the IPTSs are characterized in a temperature range of -40 °C and 90 °C. The dark current exhibits the typical exponential behaviour, increasing with the temperature, while the IPTSs show good accuracy in the above-mentioned temperature range. The dark current can be compensated by 82% of its median value and the non-uniformity is reduced by 63% when using the IPTSs, which proves the quality of the generated artificial dark frame.

II. Dark Current Compensation

A. *CMOS Image Sensor*

The test CIS is composed of a 60 × 70 pixel array, row and column decoders, a programmable gain amplifier (PGA), a sample and hold circuit (S/H), an output buffer, and an external 16 bits ADC, as shown in Figure 1. The IPTS is based on the nMOS source follower (nSFTS) of the 4T pixel itself. Thus, the 4T pixel can be used either as a pixel or as a temperature sensor.

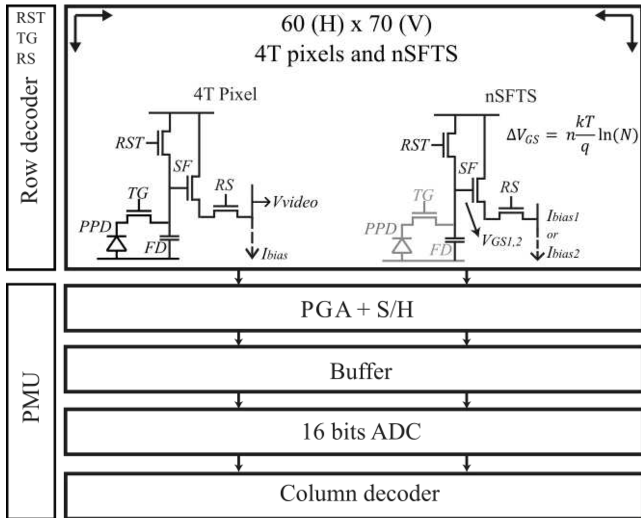


Figure 1: Block diagram of the CIS.

When the nSFTS is biased by sequential ratiometric currents in a ratio N ($N = Ibias2/Ibias1$), then the differential gate-source voltage (ΔV_{GS}) is proportional to the absolute temperature (PTAT), as shown in (1) (the TG of the pixel must be switched off):

$$\Delta V_{GS} = n\frac{kT}{q}\ln(N) \rightarrow T = \frac{q\Delta V_{GS}}{nkT\ln(N)} \quad (1)$$

where n is a process parameter, k is the Boltzmann constant, T is the absolute temperature, and q is the single electro-charge. As the pixel's readout offers the opportunity to use correlated double sampling (CDS) performed by the PGA and S/H, it becomes natural to use the same readout system for the nSFTSs in order to obtain the differential gate-source voltage.

The sensor was designed and fabricated in a standard CIS 0.18 µm TowerJazz technology.

B. Dark Current Compensation Technique

The CMOS imager pixel can be used as a standard pixel or as a temperature sensor, but not simultaneously. Nevertheless, it is possible to take a temperature frame (TF) in between the video frames, as shown in Figure 2.

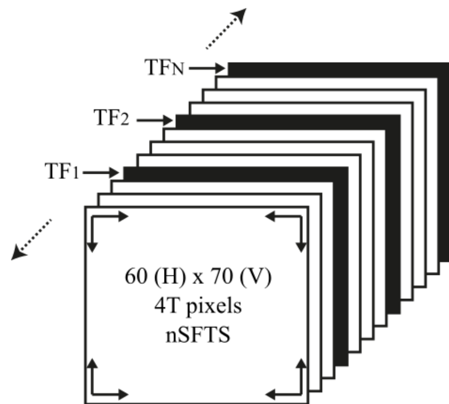


Figure 2: Temperature frames that are taken in between image frames.

As the dark current depends on temperature, it can be compensated by using the knowledge of the absolute temperature and thermal distribution provided by the TF. Thus, the dark current compensation is done locally at pixel level. It is well known that the dark current exhibits an exponential behavior over temperature, as shown in equation (2).

$$I_{dark} = A \cdot e^{B \cdot T} \quad (2)$$

Where A and B are constants defined during measurements.

Then, the nSFTSs provide absolute temperature based on ΔV_{GS} across the pixel array in the form of (3):

$$\Delta V_{GS} = C \cdot T + D \quad (3)$$

where C and D are constants.

Combining equations (2) and (3), the temperature value is replaced in the exponential fit and the absolute dark current level is obtained.

$$I_{dark} = A \cdot e^{F \cdot \Delta V_{GS}} \quad (4)$$

Where constant F combines B, C, and D.

As the dark signal (S_{dark}) linearly depends on the exposure time (t_{exp}), the absolute dark signal can be calculated from the dark current value at a certain exposure time.

$$\begin{aligned} S_{dark} &= I_{dark} \cdot t_{exp} \\ S_{dark} &= A \cdot e^{F \cdot \Delta V_{GS}} \cdot t_{exp} \end{aligned} \quad (5)$$

Thus, by applying this algorithm to each pixel across the pixel array, an artificial dark frame can be generated from the absolute temperature information provided by the nSFTSs without the need of a mechanical shutter and the request for constant temperature. Constants (A, B, C, D, and F) are obtained from measurements.

III. Measurement Results and Discussion

The measurement setup consists of a PCB, FPGA, a PC with Quartus and LabView, and a temperature-controlled oven. The test chip is mounted on the PCB that provides all the power supplied to the chip and contains the 16-bit ADC. The FPGA generates all the control signals for the chip and for the ADC. The FPGA is configured by using Quartus, and the data of the chip is collected by utilizing LabView. Measurements have been performed over a temperature range of -40 °C and 90 °C. As a temperature reference, a calibrated Pt-100 thermistor was used. After averaging 100 frames and all pixels, the average dark current exhibits two types of temperature behavior depending on the temperature range, as shown in Figure 3. At low temperatures, the average dark current increases 1.08 times every 5 °C and it is mainly due to depletion I_{dark}. While at high temperatures it increases 1.8 times every 5 °C, and diffusion I_{dark} dominates. Therefore, the dark current becomes more relevant at temperatures above 35 °C. The dark current for temperatures above 35 °C is shown in Figure 4.

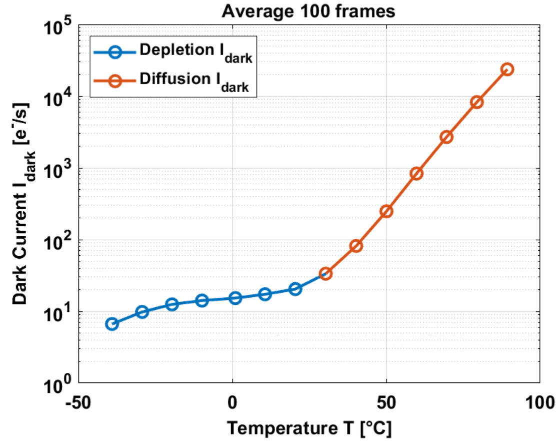


Figure 3: Dark current over temperature.

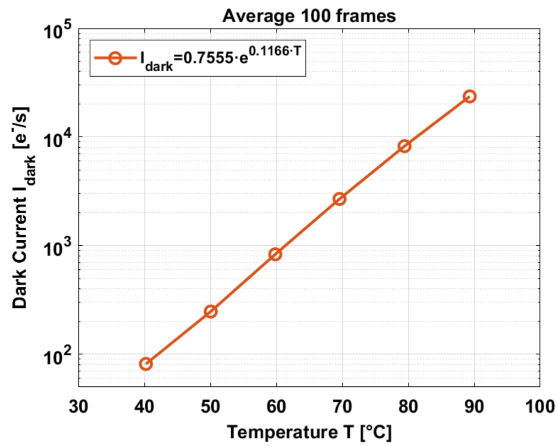


Figure 4: Dark current at high temperatures.

The average dark current at high temperatures is fit by an exponential curve providing the relation between I_{dark} and T.

On the other hand, the nSFTSs exhibit good linearity and accuracy in the temperature range of -40 °C and 90 °C. The average output voltage ΔV_{GS} has a curvature of 0.15 % with and average temperature coefficient (TC) of 1.15 mV/°C, as shown in Figure 5.

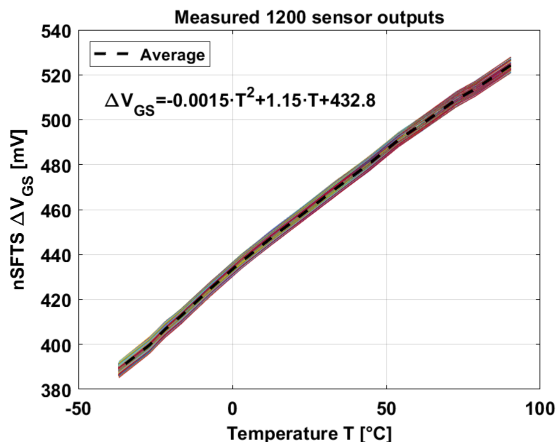


Figure 5: ΔV_{GS} over a temperature range of -40 °C and 90 °C.

After systematic non-linearity removal (by applying a 1st order polynomial), the 3σ inaccuracy was calculated by applying a 2nd order polynomial and it is ±0.55 °C, as shown in Figure 6.

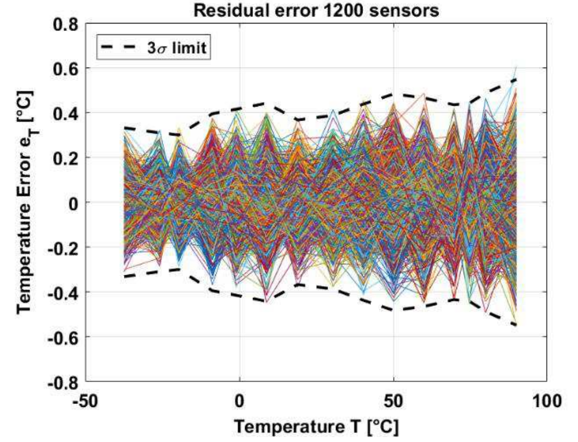


Figure 6: 3σ inaccuracy after systematic removal. 3σ = ±0.55 °C.

An artificial dark reference frame can be generated from the temperature information of each nSFTS and the average dark current, as it was stated in Section II. In this case, an artificial dark reference frame is calculated at 50 °C and at 1 s exposure time. The artificial dark frame is compared to a pre-recorded dark reference frame obtained by using an external closed mechanical shutter on the test CIS device. Figure 7 shows the comparison between frames with closed mechanical shutter and the artificially generated. For simplicity, a smaller piece of the pixel array has been considered.

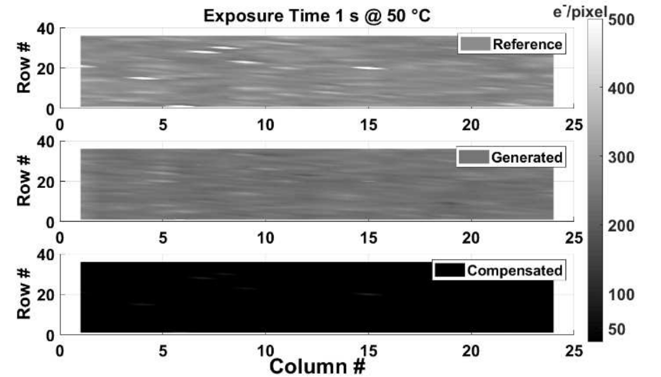


Figure 7: (Top) pre-recorded dark reference frame; (Middle) artificial dark frame ($\Delta V_{GS} \rightarrow T \rightarrow I_{dark} \rightarrow S_{dark}$); (Bottom) subtraction between the dark reference frame (top) and the generated dark frame (middle)).

After subtracting the pre-recorded dark reference frame and the artificial dark frame, the dark signal level is reduced from ~300 e⁻/pixel to ~50 e⁻/pixel, and the non-uniformity is reduced from 40 e⁻ to 15 e⁻. The compensation is done off-chip. The reduction of the median value and the non-uniformity can be clearly observed when the pre-recorded dark reference frame is compensated at histogram level. The artificial dark frame compensates the pre-recorded frame in its median value (μ) by 82 %

and it compensates in its non-uniformity (σ) by 63 %, as shown in Figure 8.

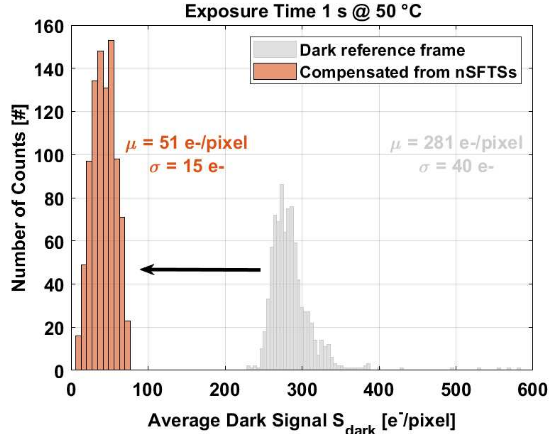


Figure 8: Compensation of the pre-recorded dark reference frame with close mechanical shutter.

The main characteristics of the CIS and the nSFTS are shown in Table 1.

Table 1: Summary of the CIS and nSFTS performance.

CIS		nSFTS	
Characteristic	Value	Characteristic	Value
Type	4T	Type	nMOS
Process [μm]	0.18	Process [μm]	0.18
Array	60 × 70	Range [°C]	−40 to 90
Pixel Area [μm^2]	11 × 11	Area [μm^2]	11 × 11
CG [μV/e$^-$]	78	Resolution [°C]	0.1
I_{dark} @ 30 °C [e$^-$/pixel]	50	3σ inaccuracy [°C]	±0.55
		Power [μW]	120

IV. CONCLUSION

A novel technique for dark current compensation of a CIS has been presented. The compensation can be performed in a CIS without the need of a mechanical shutter and the demand for constant temperature of the device. This technique makes used of accurate in-pixel temperature sensors that assist in creating an artificial dark reference frame at a certain exposure time by using the temperature information of the IPTSs and the dark current level of the CIS. The IPTS consists of the nMOS source follower of the pixel itself. When the nSFTS is biased by sequential ratiometric currents, then the ΔV_{GS} is PTAT. The artificial dark frame has been compared to a pre-recorded dark reference frame with closed mechanical shutter, proving to be highly efficient when compensation is performed. At 50 °C and at 1 s exposure time, the artificial dark frame compensates by 82 % in its median value and by 63 % in the non-uniformity.

ACKNOWLEDGMENT

The authors acknowledge TowerJazz for their support in fabricating the prototypes CIS devices.

REFERENCES

[1] J. Janesick and G. Putman, “Developments and applications of high-performance CCD and CMOS imaging arrays,” *Annual Review of Nuclear and Particle Science*, vol. 53, no. 1, pp. 263-300, 2003.

[2] L.G. McIlrath, “A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 5, pp. 846-853, 2001.

[3] C. Hsiu-Yu and K. Ya-Chin, “An ultra-low dark current CMOS imager sensor cell using n+ ring reset,” *IEEE Electron Device Letters*, vol. 23, no. 9, pp. 538-540, 2002.

[4] H.I. Kwon, I.M. Kang, B.G. Park, J.D. Lee and S.S. Park, “The analysis of dark signals in the CMOS APS imagers from the characterization of test structures,” *IEEE Transactions on Electron Devices*, vol. 51, no. 2, pp. 178-184, 2004.

[5] J. Nakamura, “Image Sensors and Signal Processing for Digital Still Cameras,” Taylor & Francis Group, pp. 67-72.

[6] S. Yu-Chuan and W. Chung-Yu, "A new CMOS pixel structure for low-dark-current and large-array-size still imager applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 51, no. 11, pp. 2204-2214, 2004.

[7] X. Wang, "Noise in sub-micron CMOS image sensors," Ph.D. Dissertation, Delft University of Technology, pp. 46-68, 2008.

[8] P.S. Baranov, V. T. Litvin, D. A. Belous, and A. A. Mantsvetov, "Dark current of the solid-state imagers at high temperature," *IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus)*, 2017: IEEE, pp. 635-638.

[9] R. Widenhorn, M. Blouke, A. Weber, A. Rest, and E. Bodegom, "Temperature dependence of dark current in a CCD," *Electronic Imaging*, 2002, vol. 4669, pp. 193-201.

[10] P. M. Beaudoin, Y. Audet, and V. H. Ponce-Ponce, "Dark current compensation in CMOS image sensors using a differential pixel architecture," *2009 Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference*, 2009, pp. 1-4.

[11] R. Widenhorn, A. Rest, M. Blouke, R. Berry, and E. Bodegom, "Computation of dark frames in digital imagers," *Electronic Imaging 2007*, 2007, vol. 6501, pp. 650103-650111.

[12] A. Abarca, S. Xie, J. Markenhof, and A. Theuwissen, “Integration of 555 temperature sensors into a 64 × 192 CMOS image sensor,” *Sensors and Actuators A: Physical* 2018, vol. 282, pp. 243-250.

[13] S. Xie, A. Abarca, and A. Theuwissen, “A CMOS-imager-pixel-based temperature sensor for dark current compensation,” *IEEE TCAS II: Express briefs* 2020, vol. 67, no. 2, pp. 255-259.

[14] A. Abarca, and A. Theuwissen, “In-pixel temperature sensors with an accuracy of ±0.25 °C, a 3σ variation of ±0.7 °C in the spatial noise and a 3σ variation of ±1 °C in the temporal domain,” *Micromachines* 2020, vol. 11, no. 7, 665.