Hot Carrier Injection Induced Random Telegraph Noise Degradation in a 0.8um-pitch 8.3Mpixel Stacked CMOS Image Sensor

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***Abstract*—**In this work we investigate the degradation of the random telegraph noise (RTN) and the threshold voltage ($\boldsymbol{V_t}$) shift of an 8.3Mpixel stacked CMOS image sensor (CIS) under hot carrier injection (HCI) stress. We report for the first time the significant statistical differences between these two aging behaviors. The $\boldsymbol{V_t}$ shift is relatively uniform among the whole population and gradually evolves over stress time. By contrast, the RTN degradation is evidently discrete and random in nature. The generation of new RTN traps during the time of stress is demonstrated both statistically and on the individual device level.

I. INTRODUCTION

The hot carrier injection (HCI), the time dependent dielectric breakdown (TDDB), the bias temperature instability (BTI), and the electron migration (EM) are the most important aging and reliability issues for advanced CMOS devices [1]. In this study, we focus on the HCI induced aging effects. Although the threshold voltage (V_t) shift and the mobility degradation caused by HCI stress are well-known for over 40 years, the impacts on random telegraph noises (RTN) are less studied or reported [2–5], especially the statistical behavior of large sample sizes.

In state-of-the-art CMOS image sensors (CIS), the pixel pitch is comparable to the visible light wavelength and the full well capacity (FWC) of the photodiode is reduced to the range of 5000 to 6000 electrons [6]. Although the median readout noise of 1 e-rms or less can be achieved by design, the RTN on the noise distribution tail could be more than 10 times higher than the median noise. Therefore, RTN becomes a performance limiting factor to achieve high dynamic range and good image quality.

II. TEST CHIP DESIGN

The test chip is a stacked backside-illuminated CIS with a sensor array on the top layer, fabricated by a 28 nm 1P4M process, and a readout circuit layer on the bottom by a 22 nm 1P7M process, stacked by a wafer-level hybrid bond (HB) technology. The array consists of 2512×3296 (8.3M) pixels with a 0.8 um pitch and a 4×2-shared structure, read out by a bank of 1648 column-parallel 12-bit ADCs with front-end amplifiers supporting 1X to 8X analog gains. A simplified signal-chain schematic is shown in Fig. 1. The 3 pixel-devices, the reset (RST), the row select (RSL), and the source follower (SF), support 3.3 V operation. The device under study is the SF NMOS with W = 0.16 um, L = 0.87 um, and 5.7 nm dielectric thickness, biased by a constant column current source of 7.2 uA in normal operations. The conversion factor from the ADC output to the SF output is 292 uV/DN at 1X gain and 36.5 uV DN at 8X gain. The median read noise is about 190 uV-rms operated at 60 MHz clock and 1.48 fps frame rate.

III. HCI STRESS EXPERIMENTS

In normal imaging mode, the SF output (V_O) is read out by a correlated double sampling (CDS), before and after the charge transfer from the photodiode to the sense node (SN). The voltage difference is amplified and digitized. In this work, we are only concerned with the SF. The charge transfer is disabled, and the SF gate voltage (V_G) is fixed by RSV with RST turned on. The readout random noise (RN) is measured by the CDS. But V_O is obtained in a test mode by measuring the difference between V_O and a fixed reference voltage.

The SF drain voltage (V_D), or the V_{PIX} in Fig. 1, is 3.1 V for normal operation. When V_D is increased, the channel conduction electrons are accelerated by the high electric field. The energetic and hot electrons can in turn generate more electron-hole pairs by the process of impact ionization. This is characterized by the rapid increase of the substrate current (I_B) due to the holes as V_D increases. Fig. 2 shows the measured I_B of a SF device vs. V_D under various current biases in separate test keys on the same wafer as the CIS chip.

In typical reliability testing, the supply voltage is raised to 20%-50% higher than its normal value to speed up the device aging. In our experiments, the SF is biased by a 7.2 uA source current (I_S), and we choose to raise the V_{PIX} in Fig. 1 up to 6.6 V where the I_B becomes comparable to I_S according to Fig. 2. Several devices under test (DUTs) were selected and stressed for 10, 20, 50, and 100 min at room temperate. Between 2 consecutive stressing, the DUT is measured under normal operation conditions. Negligible relaxation effects were observed for several days after stressing.

Because of the row-by-row rolling readout and there are 628 rows of SFs in the pixel array, the stress imposed on the DUT is different when it is active (RSL turned on, I_S = 7.2 uA, about 1/628 of the stress time) and when it is inactive (RSL turned off, I_S ~ 0 uA, about 627/628 of the stress time). It requires further study in the future to distinguish these two stress effects and their dependencies on stress voltages.

IV. HCI INDUCED VT SHIFT AND RN DEGRATION

Two well-known device aging effects caused by HCI are threshold voltage shift and mobility degradation [1]. In our SF configuration, either the increase of V_t or the decrease of mobility lead to the similar decrease of the SF output voltage. Since the V_G and I_S of the SF are fixed in our experiments, the change of SF output is considered as an effective V_t shift (ΔV_t) in the rest of this paper. Fig. 3 shows the measured

distribution of V_{GS} after a series of HCI stress up to 100 min. The change of V_{GS} (effective ΔV_t) is small and not much noticeable in Fig. 3. But the ΔV_t becomes very clear in Fig. 4 histograms by subtracting the unstressed V_{GS} from the stressed V_{GS} for each stress time t, $\Delta V_t(t) \stackrel{\text{def}}{=} V_{GS}(t) - V_{GS}(0)$. The corresponding inverse cumulative distribution function (ICDF) family of curves are plotted in Fig. 5. The systematic increasing trend of ΔV_t of various constant ICDF contours are shown in Fig. 6.

The random noises (RN) are calculated as the standard deviation of 100 consecutive frames of data, device by device. The change of RN before and after HCI stress is calculated as $\Delta RN(t) \stackrel{\text{def}}{=} \sqrt{\big(RN(t)\big)^2 - \big(RN(0)\big)^2}$.

The histograms and ICDF curves of ΔRN are shown in Fig. 7–8 and the dependence on stress time is plotted in Fig. 9. Apparently, there are similarities between Figs. 4–6 and Figs. 7–9. However, close examination in the next section shows there are significant differences as well.

V. KEY FINDINGS

The differences in the degradation of V_t and RN become clear when we look at how the individual devices change progressively throughout the stress time. Fig. 10(a)–(c) show the correlation scatter plots of the ΔV_t after 20-, 50-, and 100-min stress vs. that after 10-min stress. Regardless of the device-to-device variation, we observe that all the 1M devices are degraded uniformly. All the data points concentrate in the neighborhood along a straight line in each plot. The x/y ratios 1.78, 2.56, and 3.35 of the lines are roughly proportional to the ratios of the logarithm of the stress time.

By contrast, the correlation of the ΔRN after 20-, 50-, and 100-min stress vs. that after 10-min stress plotted in Figs. 11(a)–(c) show very different features. The scatter plots have two obvious branches. In each figure, one group of data points are centered along the x=y diagonal line, representing the devices whose RNs remain unchanged after different stress times. The other group of data points on the lower right branch correspond to the devices with RN significantly increased after longer stress time. It is also clear that the number of the points in the lower right branch continues to increase as the stress time is increased.

As previously reported [7–8], the RN distribution tails are dominated by the RTN devices showing charge emission and capture activities. The interpretation of Figs. 11(a)–(c) is that many new RTN traps are generated discretely during the stress time, while some existing RTN traps remain unchanged. Such a separation of two distinct groups does not exist in the ΔV_t scatter plots Figs. 10(a)–(c).

VI. RTN GENERATION AND DEGENERATION

The RTN devices are characterized by the multiple discrete signal levels in their time domain waveforms. We sort the 5000-frame waveforms of the entire 1M devices after each stress time according to the number of histogram peaks identified. Because of the CDS, a single trap in theory should generate a symmetric 3-peak histogram. In real data, 2-peak histograms are often observed [7]. For simplicity, we consider both the 3-peak and 2-peak cases as single-trap RTNs and plot them separately on top of the total population histograms in Figs. 12(a)–(c) for 3 stress times. Clearly the tail portion of the RN histograms are dominated by the RTN devices. And the number of RTN devices increases as the stress time increases.

Moreover, we could monitor the individual devices to see how they evolve over time. Figs. 13(a)–(c) show the snapshots of the signal waveforms and their corresponding histograms of 3 selected devices after 0-, 20-, and 100-min stress. The device in Fig. 13(a) shows a single RTN trap before the stress and remains unchanged after 20- and 100-min stress. The device in Fig. 13(b) shows no trap before stress, but one single trap defect is generated after 20 min stress and stayed the same up to 100 min stress. Fig. 13(c) shows an example device with no RTN trap after 20 min stress and one RTN trap is generated after 100 min stress. These are concrete evidence of trap generation during the HCI stress.

A defect-related RTN trap may be caused by process-induced damage (PID) or by HCI stress. Once a defect is generated, it is not expected to disappear through further stress. However, Fig. 14(a)–(b) show two examples where the 3 discrete RTN peaks might degenerate to 1 peak due to the broadening the peak width. We speculate that it is caused by the increase of non-RTN noises such as the flicker noises due to the degradation of interface states. A careful separation of the flicker noise and RTN degradation requires further study. Finally, the number of devices with identified RTN traps is plotted against stress time in Fig. 15.

VII. CONCLUSION

The RTN degradation caused by HCI stress in a CIS chip is studied both statistically and on the level of individual devices. The results highlighted the characteristic differences between the effective V_t shift and the RTN degradation, although their physical mechanisms might be similarly related to the generation of interface states and traps inside the gate dielectric by energetic electrons and holes. Monitoring the RTN degradation could be a useful tool to study the long-term reliability of MOSFET devices. More systematic experiments on a wider range of voltages and the time dependence of the HCI stress effects are in progress.

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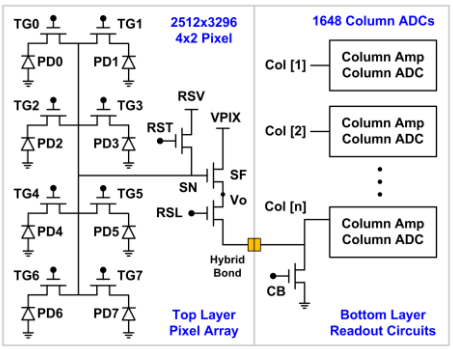


Fig. 1. Simplified test chip architecture. The device under stress is the source follower (SF) NMOS in the 4x2-shared pixel on the top layer. The total number of SF is 628x1648 ~1M.

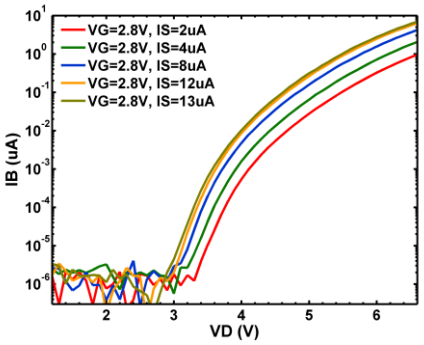


Fig. 2. The substrate current I_B of a stand-alone SF in a separate test key as a function of the drain volage V_D indexed by a family of source currents I_S while the gate voltage V_G is fixed.

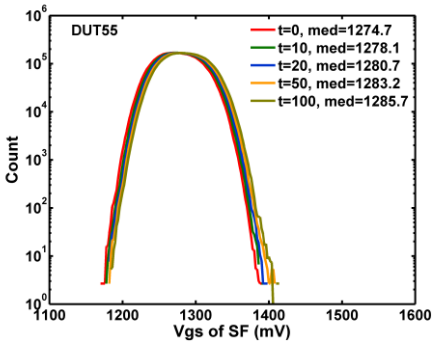


Fig. 3. The histogram of the gate-to-source voltage V_{GS} of the SF biased at a constant source current of 7.2 uA (default operation) after the HCI stress time (t) from 0 to 100 min.

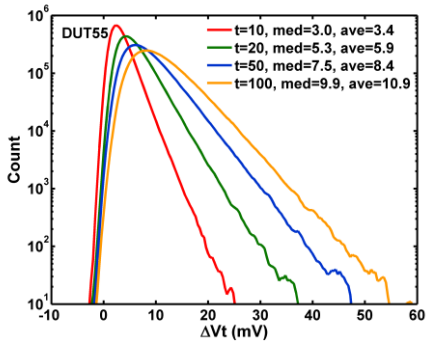


Fig. 4. The histogram of the SF threshold voltage shift (ΔV_t) after the HCI stress time (t) from 10 min to 100 min.

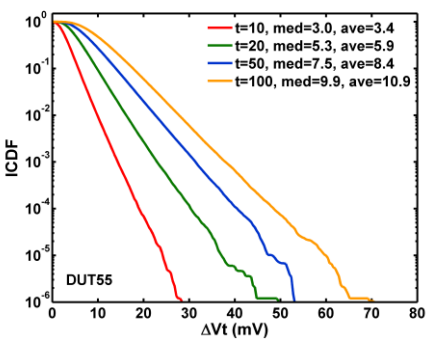


Fig. 5. The ICDF of the SF threshold voltage shift (ΔV_t) after the HCI stress time (t) from 10 to 100 min.

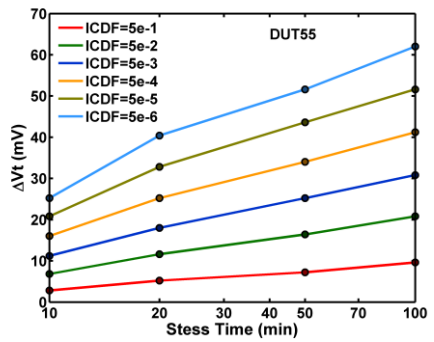


Fig. 6. The SF threshold voltage shift (ΔV_t) vs. the HCI stress time of various constant ICDF contours from 5e-1 to 5e-6.

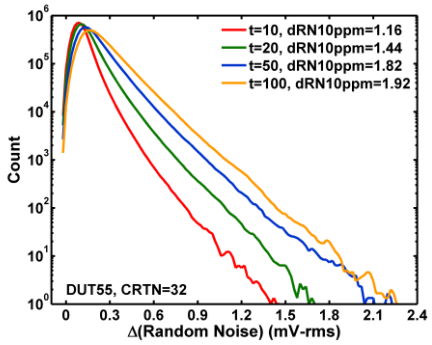


Fig. 7. The histogram of the increase of random noise (ΔRN) after the HCI stress time (t) from 10 min to 100 min.

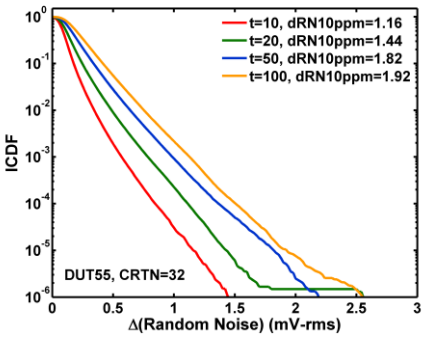


Fig. 8. The ICDF of the random noise increase (ΔRN) after the HCI stress time (t) from 10 min to 100 min.

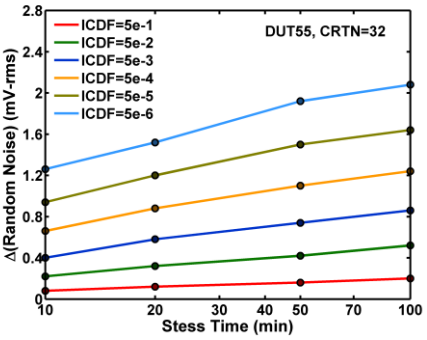
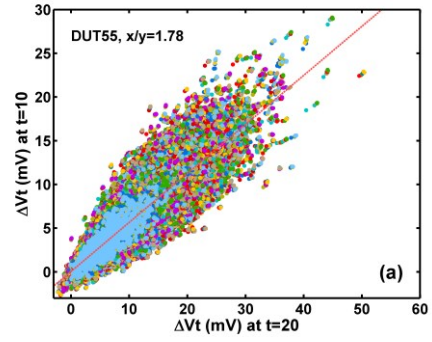
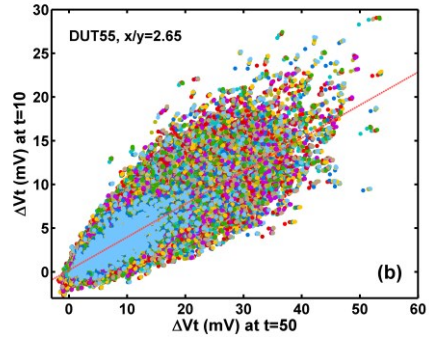


Fig.9. The increase of random noise (ΔRN) vs. the HCI stress time at various constant ICDF levels from 5e-1 to 5e-6.





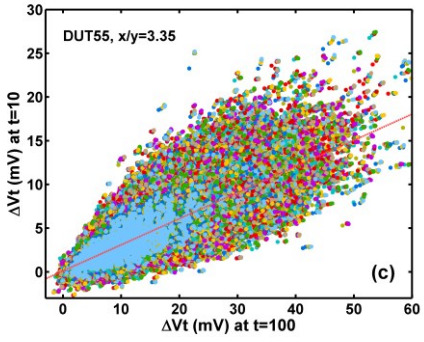


Fig. 10. The correlation of the SF threshold voltage shift (ΔV_t) after 10 min HCI stress vs. after (a) 20 min, (b) 50 min, and (c) 100 min stress, respectively. The linear least-square fit of the x/y ratio (red dash line) shows the continuous increase of the ΔV_t as the stress time increases. The ΔV_t increases are relatively uniform among all 1M devices, which are different from the random noise increases shown in Fig. 11 below.

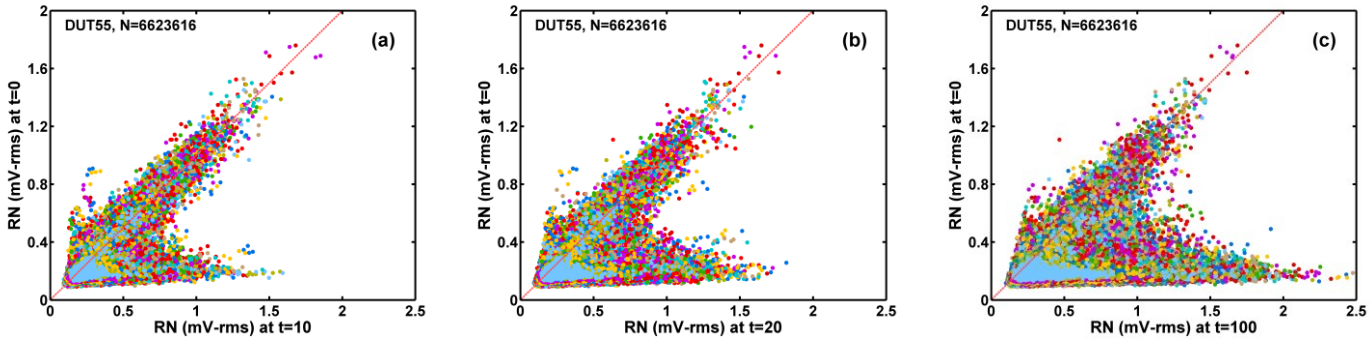


Fig. 11. The correlation of the random noises (RN) before HCI stress (t = 0) vs. after (a) 10 min, (b) 20 min, and (c) 100 min stress, respectively. The RN increases are noticeably nonuniform. The RN along the x=y red dash line remains relatively unchanged. The devices on the lower-right branches show significant increase of RN. The population of the lower branch (estimated as the number M) increases as the stress time increases.

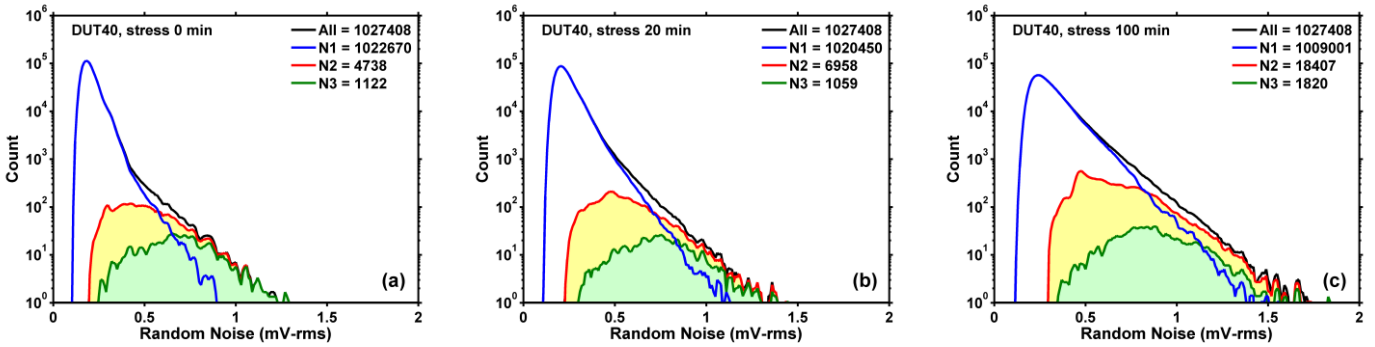


Fig. 12. The RN distribution of the RTN devices, identified by the discrete levels of their 5000-frame waveforms, (a) before HCI stress, (b) after 20 min stress, and (c) after 100 min stress. The RTN devices clearly contribute and dominate the long tails of the RN histograms. The number of RTN devices increases systematically as the stress time increases.

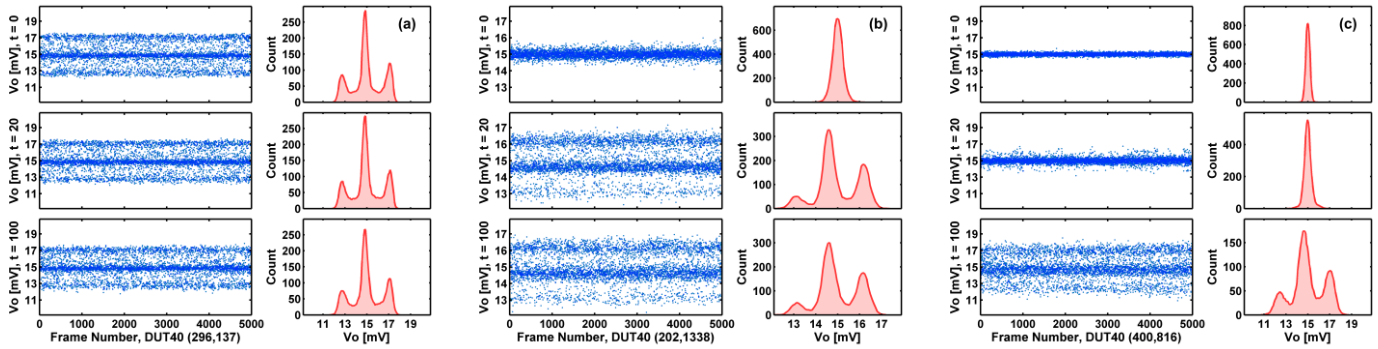


Fig. 13. Generation of RTN traps during HCI stress. The 5000-frame waveforms before (t = 0) and after the HCI stress (t = 20, 100 min) with the corresponding histograms are shown for 3 selected examples. (a) Device (296, 137) shows 1 trap before stress and remains unchanged after stress. (b) Device (202, 1338) shows no trap before stress, and 1 trap generated after 20 min stress. (c) Device (400, 816) shows no trap before stress, but 1 trap generated after 100 min stress.

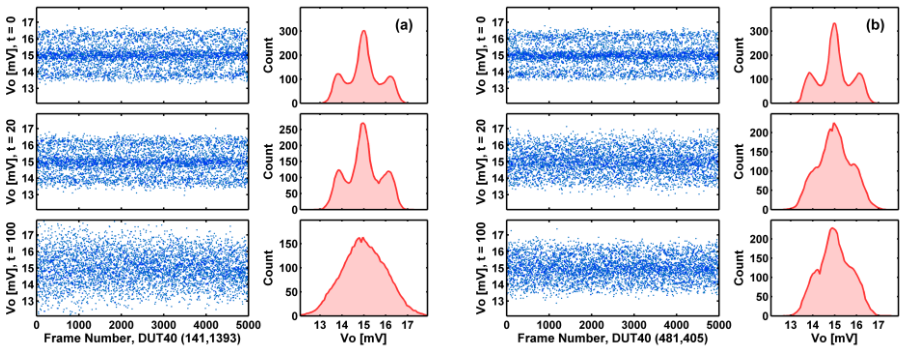


Fig. 14. Degeneration of the RTN discrete levels. During the HCI stress, the non-RTN noises may be increased significantly such that the discrete RTN levels become indistinguishable. (a) Device (141, 1393) shows such degeneration after 100 min stress. (b) Device (481, 405) shows degeneration after 20 min.

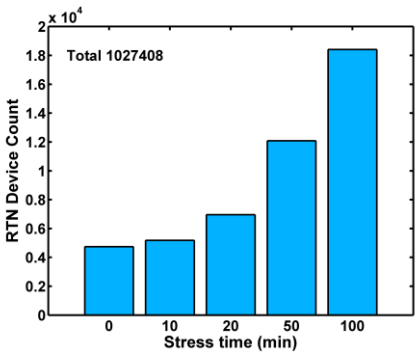


Fig. 15. Estimated number of RTN devices before and after the HCI stress based on the time-domain signal waveforms.