# *Gate Oxide Benchmarking For Low Frequency Noise Improvement On 3D Stacked CMOS Image Sensors*

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## I. Introduction

Low Frequency Noise (LFN) and especially Random Telegram Signal (RTS) can limit the performance of CMOS Image Sensors (CIS) in low light level applications. This is especially true for demanding small-pixel-pitch-CIS-generations optimized for mobile applications [HAS19]-[NAK21].

RTS impacts mainly two specific devices in CIS: the Source Follower (SF) of the pixel located in the top-tier part and the Analog-to-Digital Converter (ADC) circuit deported in the bottom-tier part [CHA21]. 3D-stacked CIS technology gives the opportunity to treat independently top and bottom sources of RTS, as shown in Fig 1. The decreasing number of devices to integrate in the top-tier part provides more process flexibility and margin to optimize at the same time the photodetection performances (driven by the photodiode) and the low noise charge-to-voltage conversion (influenced by the SF) without impacting the rest of the circuit. This aspect is developed in the following sections by proposing a dedicated gate oxide benchmarking for the top-tier and the corresponding impact on noise is studied. On the contrary, the optimization of bottom-tier ADC devices has a direct influence on the performance of the whole circuit. Hence, the RTS reduction in ADC devices by process optimization is not addressed in this study.

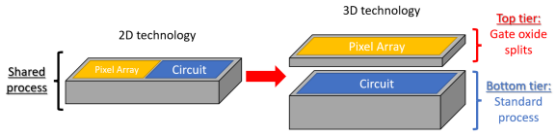


*Fig 1: 3D stacked Image Sensor. Gate Oxide (GO) process splits under investigation on the pixel array part.*

## II. Gate oxide process plan description

As exposed, a wide variety of top-tier gate oxide processes have been explored throughout this noise study. Among them, furnace oxidation, rapid thermal oxidation or nitridation processes will be further commented.

Furnace gate oxidations (FUR A and B) are slow and low temperature processes (slow increasing and decreasing temperature ramp). FUR A and B have different oxidation capabilities.

Rapid Thermal Oxidation (RTO) processes (Process Of Reference (POR)/RTO A, RTO B and RTO C) were developed to enable short time, high temperature oxidation. POR/RTO A and B have fixed oxidizing atmospheres, but temperature A is lower than B. RTO B and C have different oxidizing atmospheres but with fixed temperature.

Gate oxide nitridation processes (NIT A, B and C) are used as a barrier to prevent poly gate dopant diffusion inside the channel. POR and NIT A have the same process with different nitrogen doses (NIT A has a lower N dose than the POR). NIT A, B and C have different nitridation conditions leading to different N diffusion profiles in gate oxide bulk. NO NIT corresponds to a no nitridation condition.

Table 1 summarizes the various process trials and acronyms which are covered in this study.

TABLE I. Gate oxide splits description

| Gate oxide splits | | | |
|---|---|---|---|
| Furnace | | | |
| FUR A | | FUR B | |
| Different oxidation capacity | | | |
| Rapid thermal oxidation | | | |
| POR/RTO A | RTO B | RTO C | |
| RTO A & RTO B: Fixed atmosphere and $T_A<T_B$ | | RTO B & RTO C: Different atmospheres & $T_C=T_B$ | |
| Nitridation | | | |
| NIT A | NIT B | NIT C | NO NIT |
| POR & NIT A: Same process N dose: NIT A< POR | NIT A & NIT B & NIT C: Different nitridation condition leading to different N diffusion profile | | No nitridation |

## III. Chip design specifities and individual test structures

The tested image sensor is constituted of 0.7 Mpix based on a classical 4T pixel architecture depicted in Fig 2. It is composed of NMOS pixel transistors with fixed narrow geometries: SF, Reset (RST) and Read (RD). A pinned photodiode allowing charge collection is coupled to a Transfer Gate (TG) for charge transfer to the SF + RD readout chain. Additional individual test structures are also available and used for device material characterization: large geometry NMOST and PMOST (Specific standard $V_{th}$ MOSFETs). In this work, it is proposed to focus on the SF contribution (Low $V_{th}$ pixel MOSFETs) as it causes most of noise performance. RST and RD are considered as standard $V_{th}$ pixel MOSFETs.

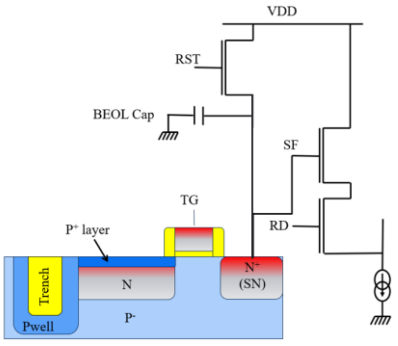


*Fig 2: 4T electrical pixel architecture studied*

## IV. Experimental results and discussion

### A. Gate oxide characterization

Before comparing electrical measurements, a full set of in-line oxide thickness measurements has been done (see Fig 3).

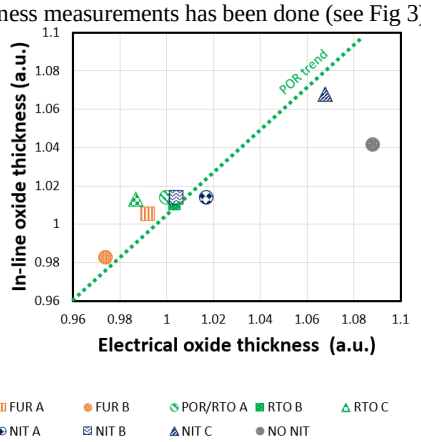


*Fig 3: Relative in-line oxide thickness variation as a function of the extracted electrical oxide thickness*

These ellipsometric measurements have been compared to Electrical Oxide Thickness (EOT) measured on large capacitance structures biased in accumulation at Parametric Test (PT). A good alignment between both measurements is seen except for NO NIT. For this process split, EOT is attributed to a significant change in relative dielectric permittivity of the gate oxide ($\varepsilon_{ox}$), as depicted in equation (1):

$$\mathrm{EOT} = \frac{\varepsilon_{ox}\varepsilon_0}{C_{ox}} \quad (1)$$

EOT and the oxide capacitance $C_{ox}$ per surface unit are inversely proportional. $\varepsilon_0$ is the vacuum permittivity.

In addition, $C_{ox}$ is directly related to the RTS amplitude $\frac{\Delta I_{DS}}{I_{DS}}$ as illustrated by [KIR89]-[SIM92]:

$$\frac{\Delta I_{DS}}{I_{DS}} = \left(\frac{gm}{I_{DS}}\right)\frac{1}{WL}\frac{q}{C_{ox}} \quad (2)$$

Where $I_{DS}$ is the MOSFET drain current, $g_m$ is the MOSFET transconductance, W and L are the MOSFET dimensions. The lower the $C_{ox}$, the higher the RTS amplitude. As a consequence, it is expected to have a higher RTS amplitude for NO NIT.

Finally, it is observed that NIT C split is significantly marginal in terms of EOT. Compared to POR, NIT C is a nitridation process using an oxidizing step resulting in a higher oxide thickness, as shown in Fig 3.

To go deeper in material characterization, the process comparison has been extended on large MOS structures to avoid edge MOS effects. By comparing threshold voltage ($V_{th}$) maps for each of them as a function of EOT and with respect to gate oxide splits, it is possible to highlight material properties variations.

Detailed $\Delta V_{th}$ vs EOT maps are plotted for NMOST in Fig 4 and for PMOS in Fig 5.

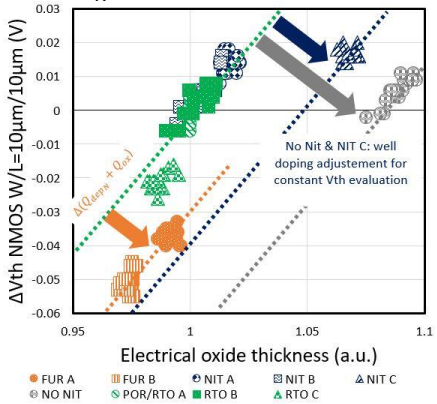


*Fig 4: Large NMOST threshold voltage variation $V_{th}$ as a function of the electrical oxide thickness for each GO process.*

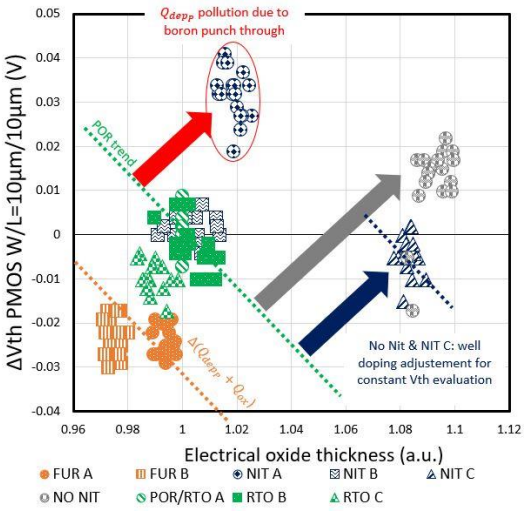


*Fig 5: Large PMOST threshold voltage variation $V_{th}$ as a function of the electrical oxide thickness for each GO process.*

Equations (3), (4) and (5) help to understand the relationship between the $V_{th}$ and EOT plots:

$$V_{th} = V_{FB} + \Phi_d + \frac{Q_{dep}}{C_{ox}} \quad (3)$$

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad (4)$$

$$C_{ox} = \frac{\varepsilon_{ox}\cdot\varepsilon_0}{EOT} \quad (5)$$

Where $V_{FB}$ is the flatband voltage, $\Phi_d$ is the potential voltage drop at the depleted region and $\Phi_{ms}$ is the work function difference between $\Phi_m$ of the gate material and $\Phi_s$ of the substrate.

Most of the process splits follow the POR trend represented by the green dashed lines. For both NMOST and PMOST $V_{th}$ decreases for furnace anneals processes, as shown in orange. It is consistent with thermal budget change (or channel depletion layer $Q_{dep}$ modification) and/or fixed charges ($Q_{ox}$) modification (consistent with more positive charges), as depicted in (3) and (4). RTO C is impacted the same way but less significantly. More significant changes are observed with nitridation related process splits. For PMOST, $V_{th}$ is shifted for NIT A. Since NIT A has a lower N dose compared to POR process, it is believed that $Q_{dep,p}$ is polluted due to poly gate dopants punch through. NIT B does not highlight any change compared to POR. Taking into account the positive charge influence on NIT C and NO NIT process splits, $Q_{dep}$ has been treated specifically to match $V_{th}$ value with POR. As a consequence, in NIT C, $Q_{dep}$ is respectively decreased by 10% for PMOST and increased of same proportion for NMOST, highlighting positive fix charge contribution changes and especially much important nitrogen diffusion in the oxide. For NO NIT, $Q_{dep}$ is respectively increased by 50% for PMOST and decreased by 30% for NMOST illustrating here positive fixed charge reduction.

In this study, noise measurements are performed on the test chips composed of small area SF MOST. In order to characterize the studied devices, $V_{th}$ variation of SF and RD MOSTs as a function of the gate oxide process is plotted in Fig 6. SF and RD are both narrow channel transistors with respectively dedicated pixel Low and Standard $V_{th}$.

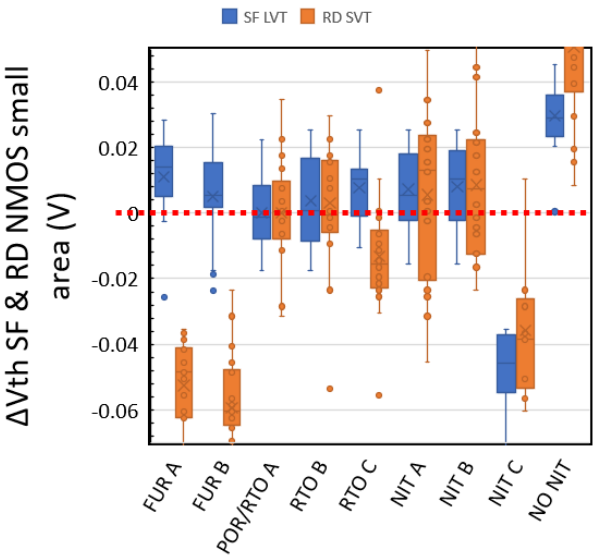


*Fig 6: Source Follower threshold voltage variation versus Readout threshold voltage variation for each GO process split compared to the POR value.*

It is observed on SF that $V_{th}$ are relatively less impacted by the studied process splits, except by NIT C and NO NIT due to uncompensated positive fixed charge effect. Since SF has a narrow channel, it is assumed that $V_{th}$ variation's contributions are not the same as in large width NMOS transistors. Lateral edge MOST contribution is added to the central MOST one.

In addition, it is observed for RD that $V_{th}$ follows comparatively the same variation as SF Low $V_{th}$, except for furnace splits FUR A and B. This highlights that Standard $V_{th}$ are more sensitive to diffusion due to thermal budget, consistently with large NMOSTs observations.

## B. *Noise extraction and discussion*

Based on 4T pixel architecture, temporal noise from each individual structure was acquired for the 700 thousand SF + RD. Fig 8 shows the relative cumulated temporal noise (TN) population at two thresholds as depicted in Fig 7: T1 and T2=2xT1. In this study, a RTS pixel is defined as a pixel with a higher TN value than the threshold T1 or T2 [WAN06], [KIT22].

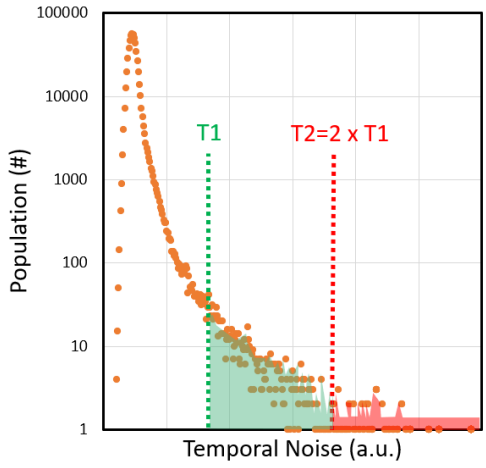


*Fig 7: Temporal noise (TN) population distribution for 1 die (700000 pixels).*

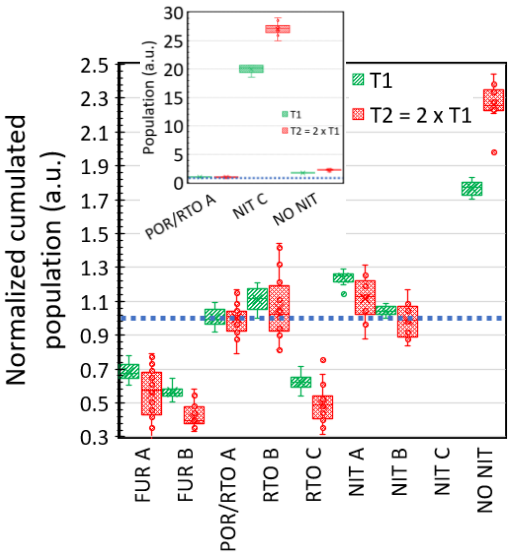


*Fig 8: Relative cumulated temporal noise population for T1 (green) and for T2 (red).*

FUR A, FUR B and RTO C conditions have the lower TN population compared to POR. On the other hand, NIT C and NO NIT show the higher TN population, consistent partly with [HA17]. Another important parameter representative of interface state evolution is photodiode dark current variation related to POR, as shown in Fig 9. Dark current depicts slight degradation for NIT C due to interface state degradation caused by significantly higher N diffusion, impacting electrons current generated underneath TG, in accumulation biased mode. It suggests that this process shared on TG and SF gate oxide is responsible of a significant degradation of near interface traps for both dark current and RTS. NO NIT degradation could be linked to significant EOT increase (due to $\varepsilon_{ox}$ change) being responsible of RTS amplitude degradation as developed earlier.

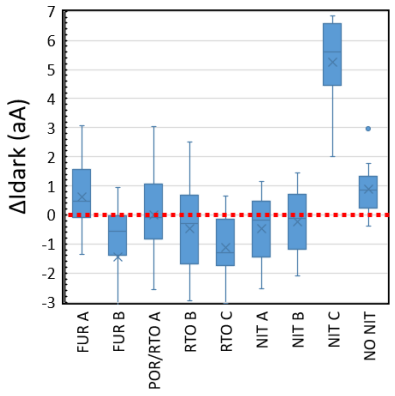


*Fig 9: Dark current shift versus process splits*

From the normalized current spectral density $S_{I_d}/I_{d^2}$ of SF (at f=10Hz) [HUN90]-[LOP11], the trap density $N_{it}$ has been extracted ($cm^{-3}.eV^{-1}$) and is plotted in Fig 10:

$$\frac{S_{Id}}{I_d^2} = S_{VGfb}\left(\frac{g_m}{I_d}\right)^2\left(1+\Omega\,\frac{I_d}{g_m}\right)^2 \qquad (6)$$

Where $S_{VGfb}$ and $\Omega$ are fitting parameters obtained from the experimental curve $\frac{S_{Id}}{I_d^2}$ versus $I_d$, $S_{VGfb}$ is the normalized flat-band voltage noise spectral density, $\Omega = \alpha_{sc}\mu_{eff}C_{ox}$, $\alpha_{sc}$ the Coulomb scattering coefficient, $\mu_{eff}$ is the effective mobility and,

$$S_{VGfb} = \frac{q^2\lambda\, kT\, \boldsymbol{N_{it}}}{WL\, C_{ox}^2 f} \qquad (7)$$

Where $\lambda$ is the tunnel attenuation distance (=0.1 nm in $SiO_2$).

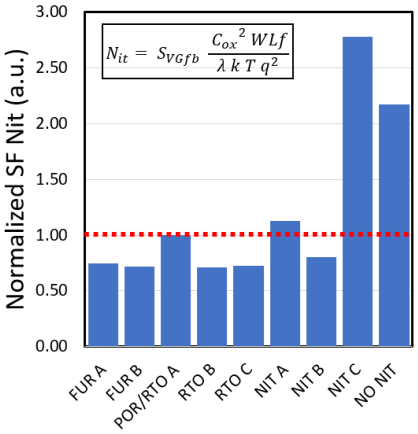


*Fig 10: Normalized trap number density $N_{it}$ evolution at 10Hz according to the process split for Source Follower*

It is observed that NIT C and NO NIT have higher $N_{it}$ than POR, since they are significantly affected either by interface density degradation or EOT increase. For the others process trials, limited variations are observed compared to POR.

A map is plotted in Fig 11 between T1 threshold population and $N_{it}$, to evaluate if a correlation exists.

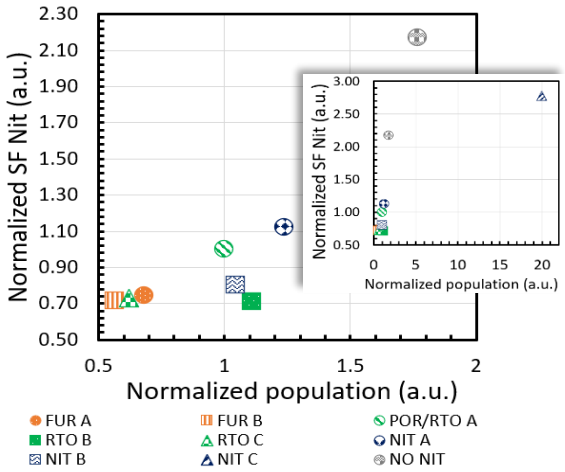


*Fig 11: Plot map $N_{it}$ versus RTS pixel population at T1*

FUR A, FUR B and RTO C conditions show an improvement for both metrics. However, some GO processes highlight an improvement on $N_{it}$ metrics without improving TN population, such as NIT B and RTO B. $N_{it}$ sampling rate extraction is assumed to be much more limited than TN sampling. It could be part of the discrepancy observed.

Moreover, it can be assumed that some process trials are more uniform or have a better quality, leading to less extrinsic variabilities and $N_{it}$ improvement observed at the same time.

Regarding defect localization, since central MOS size is reduced in SF, it is assumed here that shallow trench isolation (STI) defects could have a more important contribution in $N_{it}$ values but also on RTS population. The effects of the STI edge on low frequency noise characteristics of SF transistors have been studied in some publications [KWO16]. It has been shown that SF transistors with STI edge in contact with the channel show greater RTS amplitudes due to the enhanced trap density induced by STI-induced damage. An additional study is needed to confirm the contributors between edge and central MOS.

## V. Conclusion

Throughout this study, it was demonstrated that 3D-stacking technologies open new opportunities to improve RTS pixel in top-tier wafer without influencing the performance of the bottom-tier devices. It is highlighted that oxidizing process tuning is fully part of temporal noise optimization techniques in 3D CIS. Three conditions were clearly identified as best candidate (FUR A, FUR B and RTO C) on RTS point of view for narrow channel SF device, likely sensitive to planar oxide or top sidewall trench interface quality. This optimization could be freely cumulated to other known processes [YEN21]-[KWO13]-[KIM13], design [HAS19] or device approach [KIT22] to limit overall noise of the pixel.

Based on this noise analysis, it is observed that intrinsic defect density value $N_{it}$ and RTS extrinsic temporal noise [WAN06] are not always correlated throughout the different GO processes investigated. Although, for the three best candidates both metrics are likely improved.

In this study, no wafer-to-wafer variability problem is observed between best candidates as not enough wafers/lots have been measured, not allowing us to come out with a better candidate among the three processes mentioned above. However, from a production point of view, RTO processes are often preferred for thin gate oxide growth compared to Furnace ones especially for temperature and oxide uniformity control.

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