R2.4

Low Temperature Lag-induced FPN of Dual Transfer Global Shutter Pixels under Low Illumination Condition

Xiaoliang Ge[1], Yangyu Guo[2], Yang Liu[2], Ning Cui[2], Tadashi Imoriya[3],
Masafumi Tsutsui[3], Masakatsu Suzuki[3], Assaf Lahav[1]
[1]Gpixel Inc, Hangzhou, China; [2]Gpixel Inc, Changchun, China;
[3]Tower Partners Semiconductor Co. Ltd., Uozu, Japan
Email address: xiaoliang.ge@gpixel.com

***Abstract* — This paper presents the lag-induced Fixed Pattern Noise (FPN) of dual transfer global shutter pixels. Instead of focusing on analyzing the inter-frame charge smear between bright and dark frames, we investigate the black dots pattern artifact arising from the lag along the charge transfer path of the pixel. The presence of this image artifact in a CMOS image sensor (CIS) result in a poorer FPN for still images application. We explore the behavior of this FPN under low illumination and low temperature conditions, explain the mechanism of these lag artifacts, and further discuss the experiments that have been undertaken to enhance the charge transfer efficiency of the pixel.**

I. Introduction

In recent times, global shutter pixels [1] have gained significant popularity and are being employed in various applications. Among them, the Intelligent Traffic Systems (ITS) are particularly intrigued by this global shutter pixel technology for its capability to track fast-moving vehicles without any motion distortion. This feature facilitates the CMOS image sensors (CIS) to provide accurate and reliable data for traffic analysis and evaluation, thus, allowing the ITS to gain insight into traffic trends and help improve the traffic flow in their perspective area. Nonetheless, this ITS application necessitates an image sensor that is able to perform well in a wide range of circumstances. For instance, the camera must be able to offer clear images and ensure a high-level performance in low light conditions and extremely cold temperatures, such as -40°C. In this paper, we evaluate the performance of a 3.8um pixel pitch charge domain global shutter pixel in this kind of challenging conditions, with a focus on assessing the lag-induced FPN, and discuss the improvement trials that have been attempted.

II. Mechanism and Challenge

The charge domain dual transfer global shutter pixel schematic and operating timing are shown in Fig. 1. In this pixel, TX1 functions as a transfer gate from the Pinned-Photodiode (PPD) to Memory Node (MN), as well as acts as a storage-gate over MN. TX2 is served as a transfer gate from the MN to the Floating Diffusion (FD) node. Therefore, the incomplete charge transfer may not only take place on the typical path from PPD to the MN, but also from the MN to the FD.

Fig.2 (a)-(b) shows the captured contrast-enhanced images when the die temperature is at -40°C and 0°C. We could observe that the black dots appear in the region where the median signal level is below or around 100e-. It can be considered that the pixels with lag lost electrons during the charge transfer, resulting in darker signals and showing as black dots pattern. These black dots are camouflaged by the photon shot noise under strong light conditions, yet they become more visible when the illumination is faint, leading to a higher FPN spec. Therefore, under weak illumination conditions, the number of black dots and their associated FPN value can be leveraged to study the impact of lag on image quality.

Fig. 3 shows the signal histogram across three different temperatures, -40°C, -20°C, and 0°C. It can be observed that when the temperature decreases, the number of tail pixels over the lower signal side increases, leading to a higher FPN. This phenomenon is in line with the findings between temperature and thermionic emission charges that jump across the charge transfer potential barrier [5-6], which is expressed as:

$$Q = AT^2 exp(-X_0/kT) t_{TX\text{-}on}, \qquad [1]$$

where A is the Richardson constant, T is the temperature, X_0 is the barrier height, k is the Boltzmann constant, and $t_{TX\text{-}on}$ is the TX1/TX2 transfer time. When the internal

potential of the PPD is close to the potential barrier of charge transfer, the thermionic emission takes over the transfer process, and the amount of charge that can cross the barrier is contingent upon the environment temperature. As the temperature decreases, fewer of the charges can pass through the barrier, causing a more pronounced black dots pattern on the image. This mechanism poses a challenge in terms of achieving full charge transfer under low temperature conditions when operating this global shutter pixel.

What's more, it is noteworthy that the TX2 of this pixel works in a row-by-row manner. When a high frame-rate request is made, the TX2 switch-on period can be as short as a few hundred nanoseconds, due to the limitation of the row time. This tight transfer time presents a difficulty for complete charge transfer between MN, TX2, and FD in the design of this charge domain global shutter pixel [4].

To address these challenges, several characterizations have been done to analyze the impact of lag-induced FPN, and various design strategies have been proposed and applied in the development of this charge domain global shutter pixel.

III. Characterization Results

We evaluated the lag-induced FPN artifact by setting up the sensor in a way that the image plane could be uniformly illuminated with a light source. The illumination level and the exposure time were adjusted to ensure that the median signal reaches 100 e-. The sensor was operated at the frame rate of 65fps and 8 frame images from the pixel-array active region were obtained consecutively for statistical analysis.

Fig. 3 shows signal histograms of the die temperature under -25°C with different TX1/TX2 high voltage and charge transfer time. It can be observed that a shorter TX1 transfer time (Fig.3 (a)) and a lower TX1 switch-on voltage (Fig.3 (b)) result in more lag-induced black dots. This indicates that there is a potential hump might be present in the PPD-TX1 overlap region (Fig.4 (a)) and an edge barrier appearing on TX1 (Fig.4(b)).

Besides, the number of black dots drops as the TX2 transfer time becomes longer (Fig.3 (c)), while the number remains the same for different TX2 switch-on voltages (Fig.3 (d)). This implies that the charge transfer speed in MN is not high enough (Fig.4(c)) and a surface potential dip appears under TX2 (Fig.4(d)).

IV. Improvement and Measurement Results

Based on the study of the measurement results and TCAD simulation, optimized process splits have been proposed to improve the charge transfer performance. This optimization involves the Vpin adjustment on the PPD, electric field enhancement in the MN, and the surface potential dip flattening under TX2.

Fig. 5 (a) and (b) show the TCAD simulation results of the electrostatic potential and electric field in the MN with different additional implants. It can be observed that the electric field is enhanced with this additional n implant. Apart from that, as demonstrated in Fig.5 (c) and Fig.5 (d), the utilization of an extra implant beneath TX2 is successful in eliminating the surface potential dip and enhancing the electric field.

Fig. 6 shows the results of the experiment both at the bench-level and the wafer-level of the new DOE lot. These measurements are done with the same settings. The DOE#4 has the best results which can be explained that two times higher electric field is applied on MN combined with the optimized conditions on this split process.

V. Conclusions

This paper describes the lag-induced FPN of dual transfer global shutter pixels under low temperature and low illumination level. We investigate the behavior of this type of FPN, the causes of these lag effects, and further analyze the simulation and experiments that have been done to increase the charge transfer efficiency of the pixel.

Reference

[1] W. Gao, et al., "Photodiode Barrier Induced Lag Characterization Using a New Lag versus Idle Time Methodology", *IISW*, June 2017.

[2] L. Anzagira, et al., "Lag-Induced Image Artifacts in Still Imaging with CIS", *Electronic Imaging*, 2018.

[3] E. Fossum, et al., "Charge Transfer Noise and Lag in CMOS Active Pixel Sensors", *IISW*, June 2003.

[4] M. Tsutsui, et al., "Development of Low Noise Memory Node in a 2.8um Global Shutter Pixel with Dual Transfer", *IISW*, June 2017.

[5] E. A. Irene, et al., "Thermionic emission model for the initial regime of silicon oxidation", *Appl. Phys. Letter*, 51:767, 1987.

[6] L. Bonjour, et al., "Experimental Analysis of Lag Sources in Pinned Photodiodes", *IEEE Electron Device Letters*, vol.33, no.12, pp.1735-1737, 2012

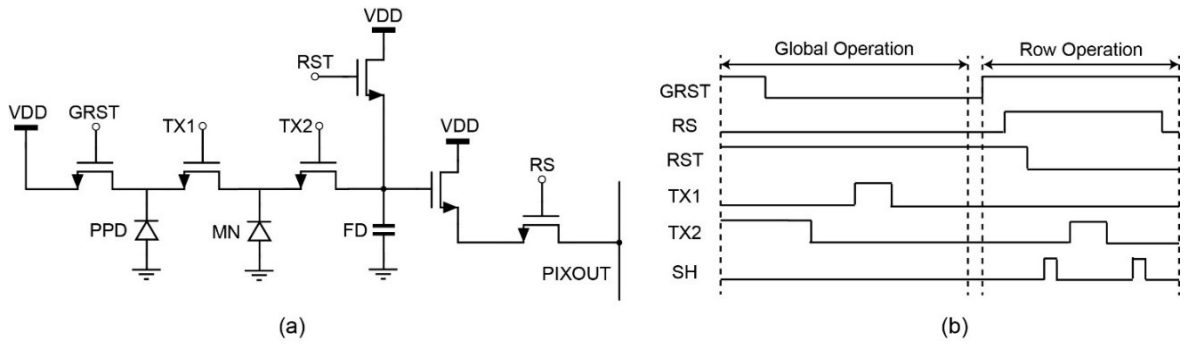

Fig. 1 Dual transfer charge domain global shutter pixel structure (a) Pixel circuit schematic; (b) Timing diagram.

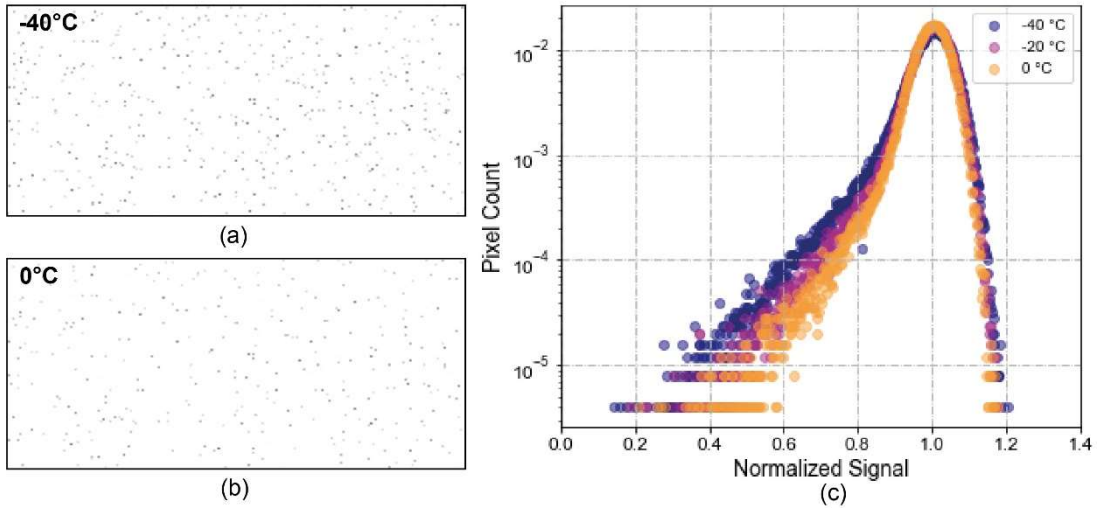

Fig. 2 Contrast-enhanced images under (a) -40°C; (b) 0°C; and (c) the normalized histogram across different temperatures.

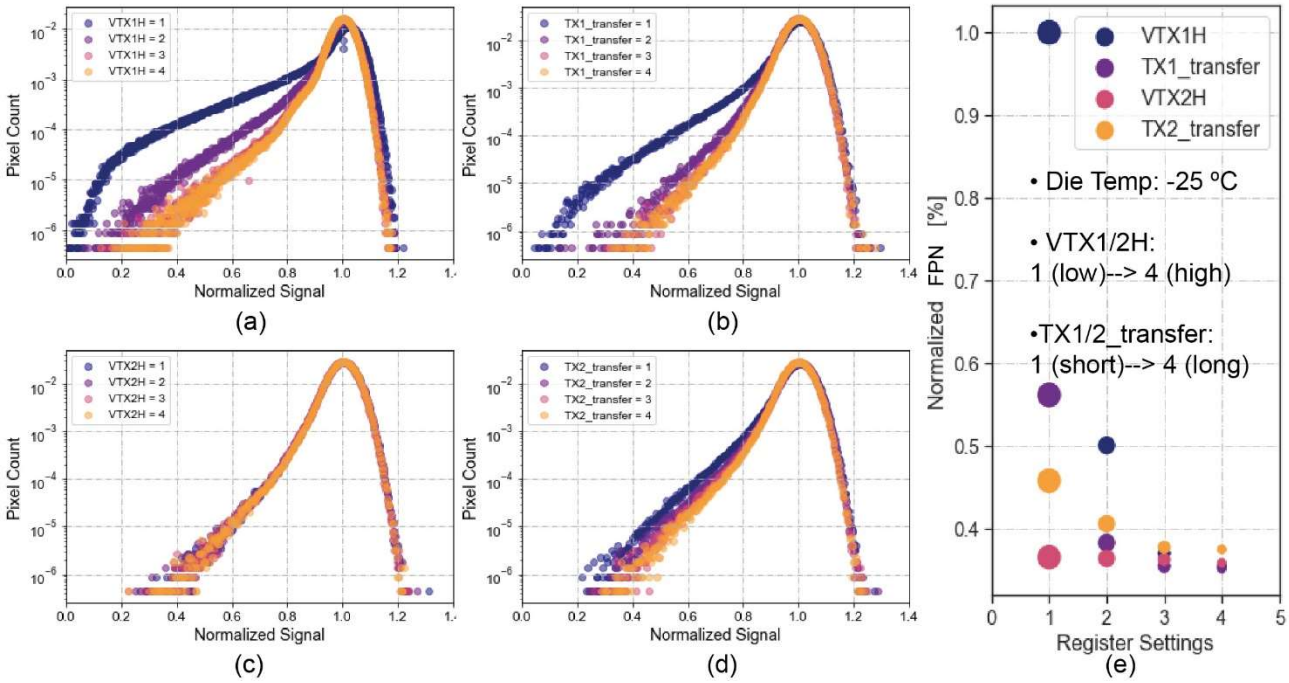

Fig. 3 Signal histograms at -25°C with TX1/ TX2 high voltage and charge transfer time @ mean signal = 100e-

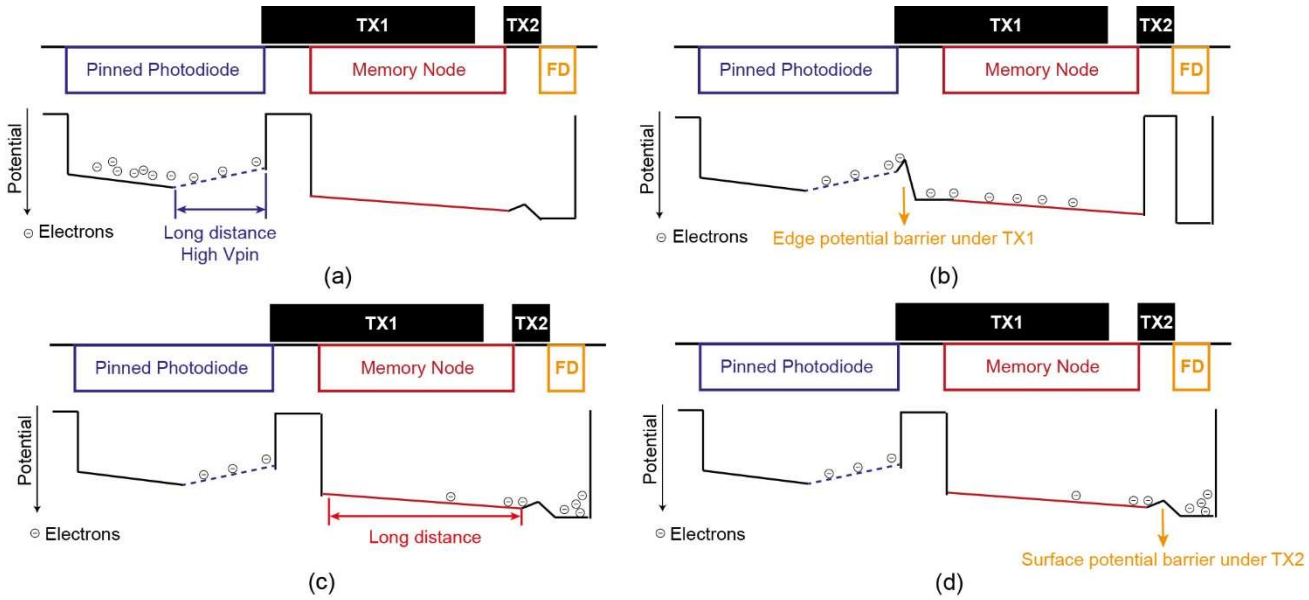

Fig. 4 Barrier locations (a) PPD; (b) TX1; (c) MN; (d) TX2.

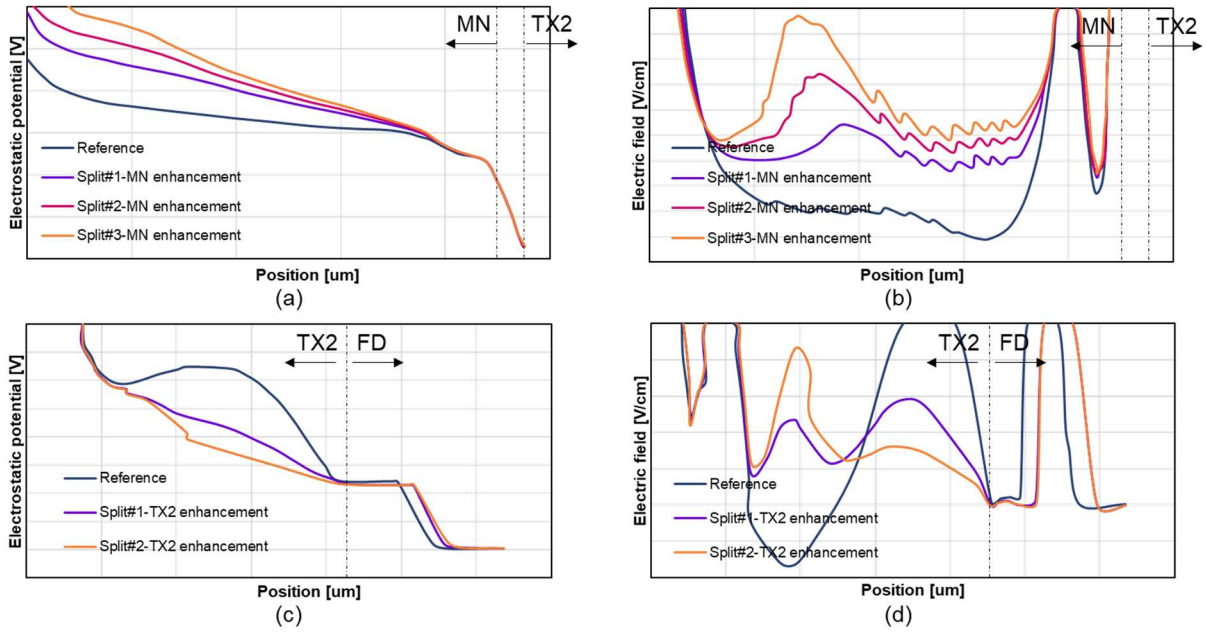

Fig. 5 MN enhancement split (a) Electrostatic potential; (b) Electric field; and TX2 enhancement split (a) Electrostatic potential; (b) Electric field;

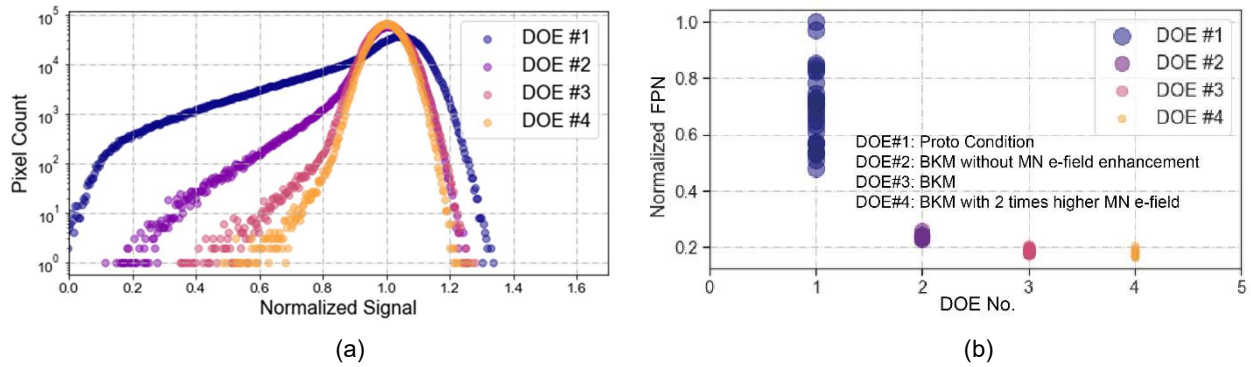

Fig. 6 (a) Signal histogram (measured at bench level); (b) Normalized PRNU (measured at wafer level)