Reduction of RTS noise by optimizing fluorine implantation in CMOS image sensor

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Abstract— In-pixel source follower transistors in CMOS image sensors play an important role in their noise characteristics. As the pixel shrink continues due to the demand for high resolution in the mobile market, the SF transistors must also become smaller. Despite the limited size of SF gates, one of the ways to prevent the degradation of noise performance is to improve the interface traps between Si and SiO_2 in the gate oxide. Additionally, RTS noise caused by these traps dominates the overall noise performance in small-pitch, high resolution CISs. In this study, we present a method to improve the RTS noise by optimizing fluorine implantation process for the SF gate. To determine the effect of the fluorine implantation on the noise performance, we fist present the experiments with various implant doses. We also presented an evaluation of the side effect of too high implantation dose and the potential for additional noise reduction by preventing the diffusion of fluorine atoms out of the gate oxide, which can occur through subsequent thermal processes.

Keywords—CMOS Image Sensors, Fluorine implantation, Source follower amplifiers, Random Telegraph Signal Noise, RTS,

I. INTRODUCTION

In CMOS image sensors (CISs), random telegraph signal (RTS) represents a noise source that causes random variations in output voltage over time [1]. The RTS noise is caused by the random trapping and de-trapping of charge carriers in the gate oxide layer resulting in threshold voltage fluctuations [1]. The RTS noise can degrade the image quality of CISs by causing image artifacts and have a significant impact on the performance of CISs in low light conditions [1].

As pixel pitch decreases, recent studies have demonstrated that RTS noise introduced by traps located at the Si-SiO2 interface of the source follower (SF) amplifiers dominates the noise performance of CISs [1,2]. On the other hand, the SF gate area has been the bottleneck of pixel shrinkage while the demand of smaller CISs with more resolutions kept on growing with the expansion of the mobile market [3]. As a result, the interface trap density has become a primary source of noise performance in small-pitch, high resolution CISs.

Fluorine implantation is commonly applied to improve the RTS noise by reducing the interface trap density [4]. Fluorine ions can passivate the traps in the gate oxide layer, which reduces the number of traps available to capture charge carriers and improves the electrical properties of SF transistors [4]. However, the use of fluorine ions must be carefully controlled to maximize RTS noise reduction and avoid side effects for the following reasons.

First of all, high-dose fluorine implantation can increase the gate oxide thickness by introducing excess fluorine atoms into the oxide layer [2]. When the fluorine atoms are introduced into the oxide layer, they can bond with the silicon atoms in the oxide layer to form silicon-fluorine bonds. Once the interface is saturated with the silicon-fluorine bonds, the Si-O bonds in the bulk oxide layer are broken by fluorine and the oxygen diffuses towards the interface to oxidize additional silicon as illustrated in Figure 1 [2]. Also, it is known that increased gate oxide thickness can lead to deterioration of RTS noise characteristics [5]

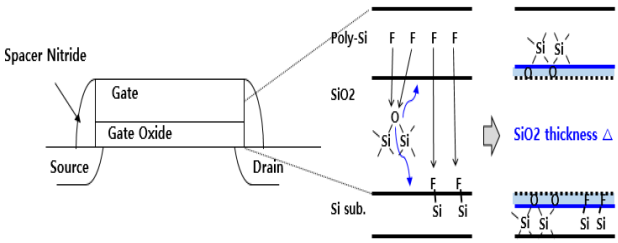

Fig 1. Schematic diagram of a SF transistor (left) and fluorine effects on SiO_2 (right)

Second, the net fluorine concentration in the gate oxide layer, which is responsible for the passivation of interface traps, may decrease due to out-diffusion by the post-thermal processes [6]. As the gate size decreases, fluorine diffusion to the gate edge is the main cause of the decrease in net fluorine concentration [6].

The paper is organized as follows. We first present a typical gate fabrication process and experiments using different fluorine doses and process sequences. We also describe how to measure interface trap density, electrical gate oxide thickness, and RTS noise. Finally, we propose optimized fluorine implantation conditions that result in the most RTS noise reduction without adverse effects.

II. Methods

The fabrication of the SF amplifier used in the experiments is a general polysilicon gate fabrication process. Gate and field oxide films are grown, polysilicon is deposited on the surface of the oxide films, and then patterned. The polysilicon gate is oxidized, then nitride sidewall spacers are formed and source-drain regions are ion-implanted.

Fluorine implantation is processed prior to formation of the nitride sidewall spacers with different implant doses, and interfacial trap density, gate oxide thickness and RTS noise are quantified. In addition, the fluorine implantation is performed twice to confirm the side-effects of excessive fluorine dose. Finally, in order to investigate the degree of RTS noise reduction according to the presence or absence of the diffusion barrier., an additional experiment is conducted on the fluorine implantation after forming the nitride sidewall spacers.

We use a charge pumping method to quantify the interface state density of the gate oxide layer. The charge pumping method is based on the idea that interface traps can capture and release charges by applying a periodic voltage to the gate of the transistor. The charges trapped in the interface traps result in a shift in the threshold voltage of the transistor, which can be measured as a change in the drain current (Icp). By measuring the change in the drain current as a function of the gate voltage, it is possible to calculate the density of the interface traps in the gate oxide layer.

We use a high-frequency capacitance-voltage (HF-CV) measurement method to obtain the electrical gate oxide thickness (Tinv). The HF-CV method is a technique used to measure the capacitance of a transistor as a function of the voltage applied to its gate at high frequencies. Measurements can provide information about interface density of states, oxide thickness, and other key parameters that can affect a transistor's performance.

For RTS noise measurements, we take two consecutive image frames under dark conditions with high analog gain. Then we plot the pixel-by-pixel output difference on a histogram. In addition, the RTS noise is obtained by counting the number of pixels that differ by more than a certain standard in parts-per-million (ppm) units.

III. Results and Discussion

During the fabrication process, fluorine atoms are first introduced via ion implantation into the polysilicon and diffused into the gate oxide after annealing, as shown by the SIMS measurements in Figure 2(a). Also, Figure 2(b) shows that 1.6 times more fluorine atoms exist in the gate oxide film when the fluorine implantation process is performed twice than the standard condition. This result indicates that the more fluorine atoms implanted into the polysilicon, the more fluorine atoms can be located in the oxide layer after annealing to passivate more traps on the interface surface.

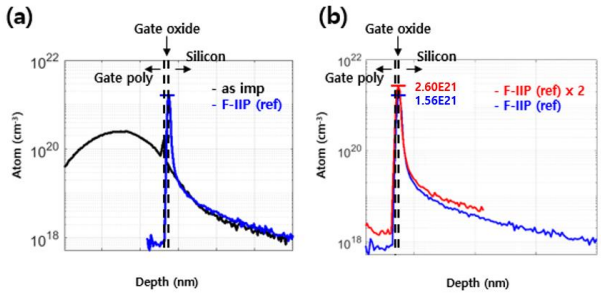

Fig 2. SIMS fluorine profiles. (a) Fluorine dose profile before (black line) and after anneal (blue line) (b) Comparison of fluorine profiles for once (blue line) and twice implantations (red line).

To confirm the above result, we performed CP measurements with different fluorine doses as describe in Methods section. Figure 3(b) shows that Icp decreases with increasing the dose of fluorine implantation. It indicates that interfacial properties appear to improve with higher dose of fluorine implantation. The HF-CV measurements show that the gate oxide capacitance decreases with increasing fluorine implantation doses, as shown in Figure 3(a). This result represents the actual increase in gate oxide thickness as mentioned in the introduction section.

Interfacial properties and gate oxide thickness are one of the key parameters for RTS noise characteristics as described in the equation in Figure 3. Therefore, RTS noise measurements were performed with different implant dose and we found that the improvement of interfacial properties (i.e. Nit) has a more dominant effect on the RTS noise than the increase in gate oxide thickness (Tinv) caused by fluorine implantation. As results, we were able to reduce RTS noise about 20% by increasing fluorine implantation dose, as shown in Figure 4.

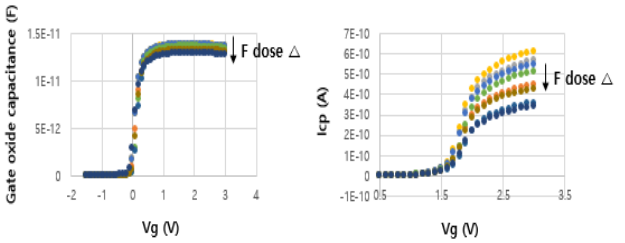

Fig 3. Results of charge pumping (left) and high-frequency capacitance-voltage measurements (right) as a function of fluorine implantation doses.

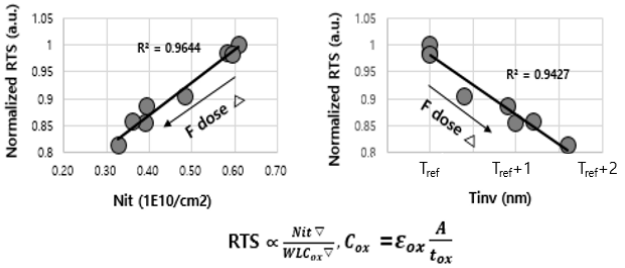

Fig 4. Correlation between RTS noise and gate oxide properties according to different fluorine implantation. In the right figure, T_{ref} represents thickness of inversion layer at the interface between the silicon and silicon oxide (T_{inv}) when F-IIP is not applied. Ref+1, Ref+2 indicate T_{inv} that is 1 and 2 greater than the T_{ref}, respectively.

To determine the side effects of high-dose fluorine implantation, we also performed fluorine implantation twice after gate poly-silicon deposition as described in Methods section. Then, we found that high-dose fluorine implantation caused a large number of gaseous bubble defects in silicon oxide.

This is because fluorine ions can react with the silicon atoms in the oxide to form SiF4 gas, which can create gaseous voids or bubbles as shown in Figure 5. The process typically begins with implantation of fluorine ions into the silicon oxide, which can damage the lattice structure of the oxide layer. During the post annealing steps, the fluorine ions can react with the silicon atoms in the oxide to form SiF4 gas. The SiF4 gas can then accumulate in the oxide, forming gaseous bubbles. As a results, it was shown that the fluorine implantation dose could not be continuously increased due to the side effects mentioned above.

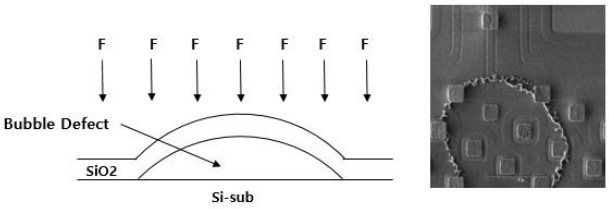

Fig 5. Bubble defects inside the surface oxide under the high dose fluorine implantation condition.

Due to the above bubble defects, there is a limit to increasing the fluorine implantation dose, so another method to improve RTS reduction with a limited fluorine implantation dose is needed. Therefore, we move the fluorine implantation process step after the nitride sidewalls spacers to use the nitride spacer as diffusion barrier. As a result, we expected to increase the net fluorine concentration in the gate oxide layer by minimizing the out-diffusion of fluorine atoms at the gate edge, as described in Methods section. The results show an additional 4% improvement in RTS noise reduction when nitride spacer formation is followed by fluorine implantation. This indicates that retained fluorine concentration increased as illustrated in Figure 6. Finally, we were able to reduce the RTS noise in our device by approximately 14% by optimizing the fluorine implantation process, without side effects on the gate oxide layer, as illustrated in Figure 6.

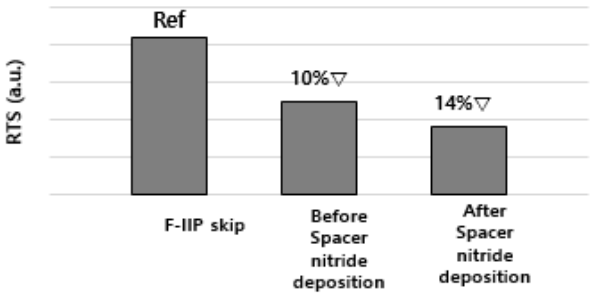

Fig 6. RTS noise results according to the different fluorine implantation process sequence.

IV. Conclusion

We conducted a study on the mechanism of fluorine implantation in order to improve RTS noise by reducing interface traps in the gate oxide layer of SF transistors. We found that RTS noise improved with increasing the dose of fluoride implantation. However, we confirmed that the dose could not be continuously increased due to the bubble defect, and RTS noise could be improved by about 10% compared to the case where fluorine implantation was not applied. We also found that in a limited dose of fluorine implantation, RTS noise could be further improved by 4% by using the nitride spacers used as diffusion barriers to reduce the diffusion of the fluorine atoms to the gate edge. This achievement can allow further pixel shrink for the high-resolution CISs without the inevitable noise degradation at a limited SF sizes.

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