0.6μm F-DTI based Quad-cell with Advanced Optic Technology for All-pixel PDAF and High Sensitivity/SNR Performance

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Abstract

Smaller pixels with high auto-focus (AF) performance are high in demand and Quad-cell (Q-cell) structure where four photodiodes (PD) are located under a single micro-lens is regarded as a solution. In this paper, we presented a 0.6μm F-DTI Q-cell CMOS image sensor with advanced optic technology such as DTI center cut (DCC) and increased thickness of DTI reflecting oxide layer (ROL). As a result, sensitivity and SNR were increased by 112% and +0.5dB, respectively compared to the conventional Q-cell and a brighter image was also obtained at low light environment.

Introduction

Recently, strong demands for smaller pixel size and better AF performance of image sensors are emerging throughout the years. Several pixel structures have been developed to ensure high AF performance. [1, 2] Among them, the Q-cell structure where one micro-lens covers four PDs enables both high resolution and high AF performance owing to their small-sized pixel and 100% AF density. In addition, full-depth deep-trench isolation (F-DTI) technology is essential to achieve low crosstalk between neighboring pixels and large full-well capacity (FWC) of small pixels. [3, 4] In this paper, we developed 0.6μm-pitch F-DTI based Q-cell and proposed advanced optic technologies to achieve high sensitivity and SNR performance.

Pixel micro-lens technology

Figure 1(a) and (b) show the schematics of Tetra-cell and Q-cell and their AF disparity performances according to illuminance. Q-cell demonstrated improved AF performance especially at low light compared to the Tetra-cell with sparse AF since all the pixels of Q-cell operate as AF pixels. However, due to the physical structure where 4 PDs are located under the single micro-lens, the light is focused on the boundary of the 4 PDs. So the signal difference between 4 pixels occurs more sensitively, and this difference is denoted as “intra tetra pixel difference”. Intra tetra pixel difference causes image quality degradation because the light entering each PD is not uniform. Generally, intra tetra pixel difference is highly affected by the mismatch of chief ray angle (CRA) between the micro-lens and the pixel arrays, and micro-lens mis-alignment. As shown in Figure 1(c), in the Tetra-cell structure, the light passing through each micro-lens reaches each PD uniformly regardless of CRA difference and micro-lens misalignment. On the other hand, Q-cell is more sensitive to these two factors than Tetra-cell, and an optimized Q-cell design suitable for these characteristics was required. In addition, in Q-cell structure, the light is focused on the DTI center of intra four pixels. Since the DTI center is composed of poly-silicon which absorbs

visible light, sensitivity and SNR loss occur. Figure 2 shows the schematic and beam profile simulation of light loss from gap-filled poly-silicon.

Experimental results

In order to reduce the sensitivity loss, we applied advanced optic technologies such as DCC and increased thickness of total reflection material by thickening the DTI ROL. As shown in images in Figure 3 (a), the DCC technology, which partially removed the DTI located in the center of the 2 by 2 pixels, allowed the light entering the Q-cell micro-lens to reach the center of DTI and prevented the light lost by the gap-filled poly-silicon. Sensitivity improvement as the increment of DCC width was verified by the simulation and measured data as shown in the graph in Figure 3 (b). Furthermore, sensitivity was also improved by increasing the thickness of the DTI ROL. Images in Figure 4 (a) shows the DTI ROL between the Si and poly-silicon. Since poly-silicon has the same absorption coefficient and refractive index with Si, the light penetrating the ROL was absorbed into poly-silicon, which reduced sensitivity loss. As the thickness of ROL increased, the poly-silicon area was reduced and the reflected light also increased. As shown in Figure 4 (b), QE improvement as the increment of the thickness of ROL was confirmed from the optical simulation and measurement data. Figure 5 (a) shows the normalized QE of the conventional and advanced Q-cell according to the wavelength. The QE peak and overall sensitivity of the advanced Q-cell were improved by 12% compared to the conventional Q-cell with non-DCC and thin DTI ROL. Photographic images in Figure 5(b) also showed that a brighter image was taken in advanced Q-cell owing to the improved sensitivity and SNR. Major pixel characteristics of the conventional and advanced Q-cell are summarized in Table 1. These results demonstrated that high sensitivity and SNR were implemented in 0.6µm Q-cell structure with high AF performance.

Conclusion

In conclusion, we have proposed advanced optic technologies such as DCC and thick DTI ROL and achieved high sensitivity and SNR of 0.6µm F-DTI Q-cell. The sensitivity and SNR have dramatically improved, reaching up to 112% and +0.5dB compared with the conventional Q-cell. This advanced Q-cell with high AF performance can be essential technology for high sensitivity and SNR of CMOS image sensors in the future.

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Figures

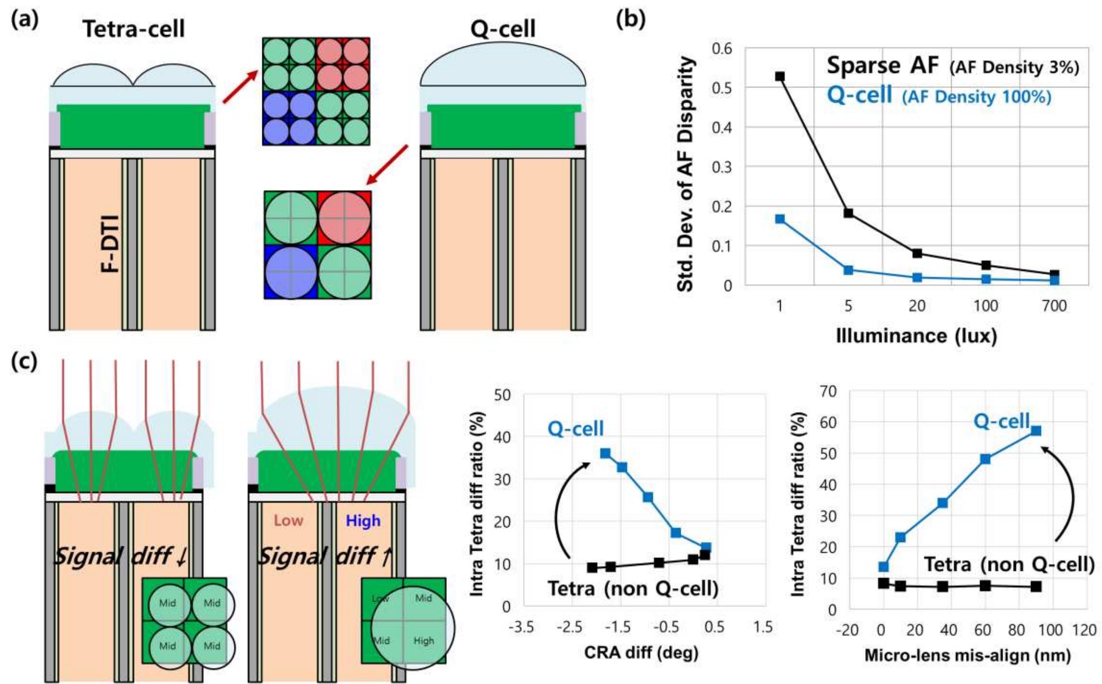

Figure 1. (a) Schematics of Tetra-cell and Quad-cell (Q-cell). (b) Standard deviation of AF disparity of Q-cell and Tetra-cell according to illuminance. (c) Tetra difference according to CRA mismatch and mis-alignment of micro lens.

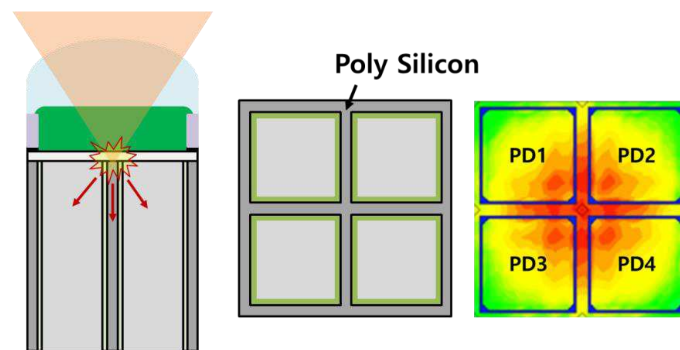

Figure 2. Schematic and beam profile simulation of light loss from poly-silicon.

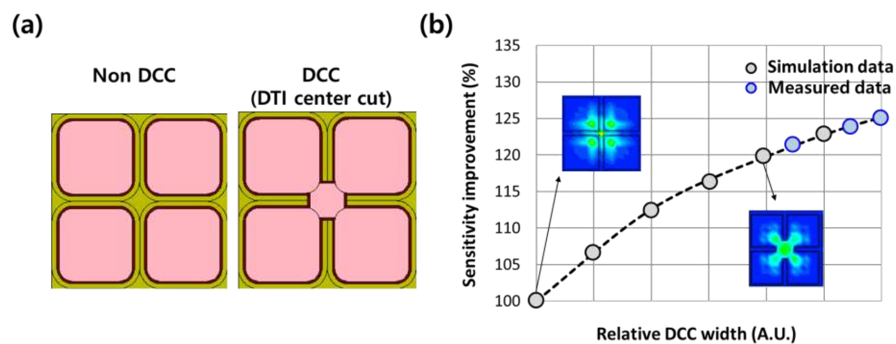

Figure 3. (a) Non DCC and DCC images. (b) Sensitivity improvement according to the DCC size.

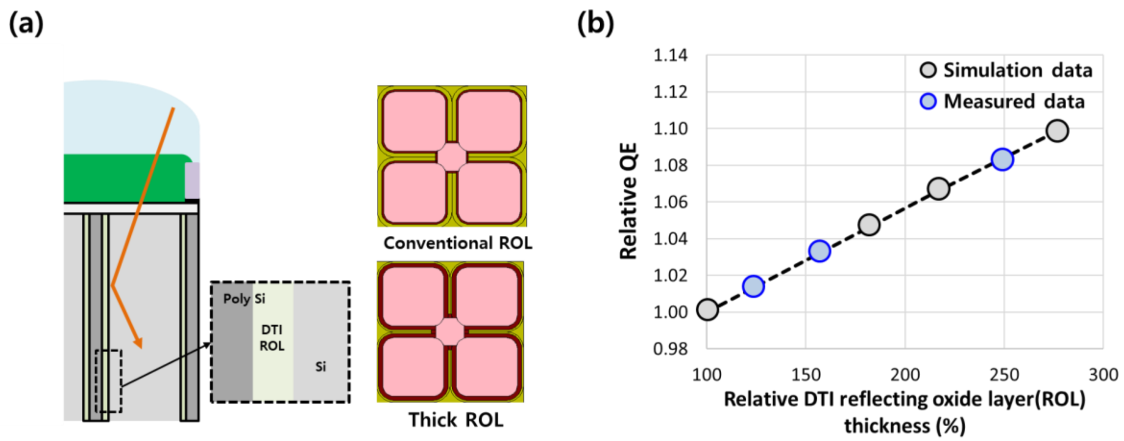

Figure 4. (a) Schematics of DTI reflecting oxide layer (ROL). (b) Relative quantum efficiency (QE) according to the DTI ROL thickness.

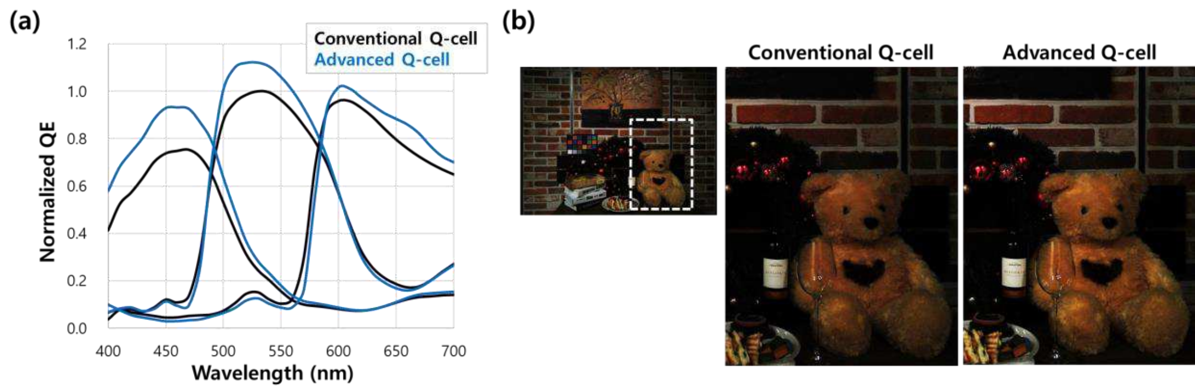

Figure 5. (a) Normalized quantum efficiency and (b) Photographic images of conventional and advanced Q-cell. The photographic images were taken at low light illuminance of 10lux.

	unit	Conventional Q-cell	Advanced Q-cell
Pixel Size	μm	0.6	0.6
Sensitivity	%	100	112
SNR	dB	-	+0.5
AF density	%	100	100
AF contrast ratio	-	2.75	2.6
Intra Tetra diff ratio	%	29	26
Gr/Gb ratio	%	2.2	2.0

Table 1. Characteristics of the conventional Q-cell and new Q-cell.

Low-noise 3-D Bending Pixel Transistor for Small Pixel CMOS Image Sensors

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Abstract— We demonstrated a low-noise back-illuminated CMOS image sensor, employing a three-dimensional (3-D) vertical gate structured bending transistor for in-pixel source-follower (SF) amplifiers. The 3-D gate structured SF was simply formed by adding a field oxide recess process near the channel region. To maximize the effective channel area, a considerate 3-D gate structure into a bending-type SF was devised. Firstly, the vertical gate structure was partially adopted on the current path in bending-SF. Three different types of 3-D bending SF were compared in terms of trans-conductance (g_m) and the effective channel width (W_{eff}). Then, in an optimized SF structure, the g_m and W_{eff} were improved up to 9% and 20%, respectively, compared to the planar bending-SF. This leads to the reduction of temporal random noise by 2% compared to the planar one. Furthermore, as the depth of vertical gate increases from *0.63×W* to *0.88×W*, where *W* is the width of planar channel, the random noise decreased more by 7%. Finally, the wafer-level random telegraph signal (RTS) noise was evaluated and it decreased about 62% compared to the planar one. We expect this result to accelerate the scaling down of a pixel pitch which is crucial for high-resolution image sensors in the future mobile market.

Keywords—CMOS Image Sensors, Vertical gate transistors, Source follower amplifiers, Bending transistor, Random noise, Thermal noise, Flicker noise, Temporal noise, Random Telegraph Signal Noise, RTS

I. INTRODUCTION

CMOS image sensor (CIS) industry have moved fast toward small-pitch and high-resolution sensors due to strong demand from growing mobile markets for the past several years. To make pixel pitch smaller, transistors in each pixel have been rapidly scaled down as well [1, 2]. However, such scaling of in-pixel transistors inevitably deteriorates their own electrical characteristics, such as trans-conductance (g_m) and leakage current, which leads to deterioration in image quality of CISs [3, 4]. In particular, a source follower (SF) amplifier transistor is of utmost importance as it determines several important characteristics of sensor including linearity and noise performances. For instance, as the channel length of SF transistor decreases, the short channel effect, i.e. drain-induced barrier lowering *(DIBL)*, results in non-linear SF gain in dynamic light range. In addition, the smaller the SF channel area is, the more severe temporal signal fluctuation becomes as it originates from the interface traps at the SF channel area. Therefore, there have been consistent efforts to maximize the effective channel area of SF in a given pixel area [5, 6].

In this work, we firstly demonstrated 3-D bending SF transistors in a *0.5 μm* pitched *64 Mega-pixels'* image sensor. By adopting a bending SF rather than a conventional straight SF, the longer effective channel length (L_{eff}) was achieved in a same footprint. Then, to maximize the effective channel width (W_{eff}), a 3-D vertical gate structure was introduced to a bending transistor. In particular, a 3-D gate structure was needed to be considerately optimized for a bending SF as the current path in bending SF is not uniform like that in the conventional straight SF.

II. DEVICE FABRICATION

We fabricated a 4-transistor active pixel sensor (4-T APS) as shown in Figure 1(a). In order to maximize the SF area within the limited pixel pitch, a bending SF was adopted instead of a conventional straight SF. By adopting a bending SF, the longer effective channel length ($L_{Bending}$) was achieved compared to that of the conventional straight SF ($L_{Straight}$) in a same foot-print as shown in Figure 1(b).

Then, to maximize the effective channel width (W_{eff}), a 3-D gate structure was adopted to a bending SF transistor. The 3-D gate structure was simply formed by replacing a field oxide near the channel to a vertical gate stack. A fabrication processes added from a planar SF, to form a 3-D gate, are illustrated in Figure 1(c). First, the p-type doped active Si was defined by the shallow trench isolation (STI) for a channel of SF. Then, a hard

mask and a photoresist are patterned by a photolithography to define a 3-D vertical gate region. To recess a field oxide in a vertical gate region, dry etching process was conducted followed by removal of hard mask and photoresist. Then, a gate oxide was grown by a thermal oxidation for both regions of vertical gate and planar gate. Finally, a Poly-Si was deposited and patterned followed by metallization.

In particular, a considerate 3-D gate structure was needed to maximize its effective channel area, as the current density in bending SF is not uniform like in conventional straight SF. We carefully optimized a 3-D gate layout considering the current path in bending SF. First, we found that a Bi-gate structure, shown in Figure 1(d), is more efficient to maximize the effective channel area in bending SF than a Tri-gate structure. Then, we further optimized the Bi-gate layout precisely for a bending SF. Three different vertical gate layouts of bending 3D-SF (1), (2) and (3) were fabricated and evaluated in terms of noise performances. Also, a depth of vertical gate was investigated in an optimized bending 3D-SF layout.

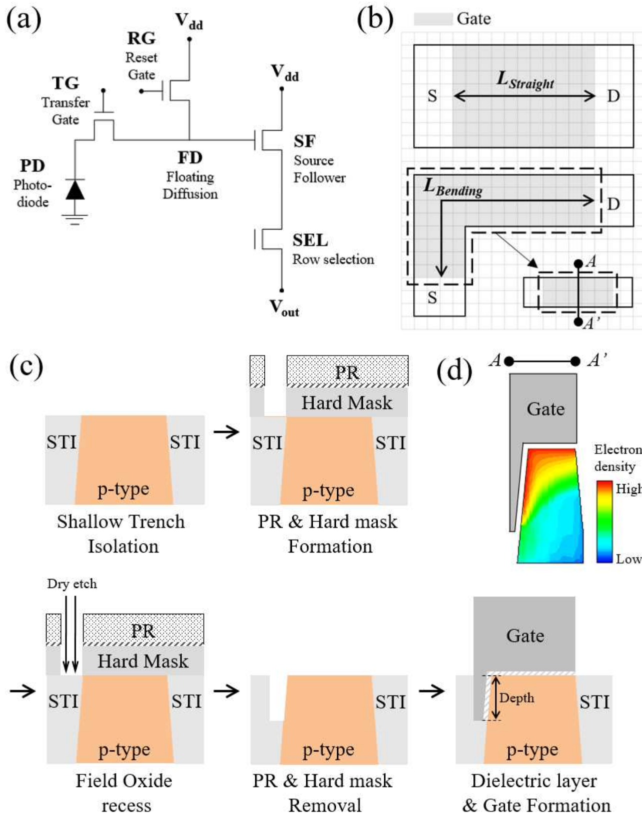

Figure 1. A schematic illustration of (a) pixel representation, (b) straight and bending in-pixel source follower (SF) transistor. (c) The fabrication process to form a 3-D gate structure into a bending SF. (d) The schematic illustration of a Bi-gate 3-D bending SF at A-A' cross-section with an electron density.

III. Results and Discussion

The fabricated 3-D bending SFs were electrically characterized by the test element structures, which are placed adjacently to the actual pixel arrays. Typical transistor performance metrics, such as threshold voltage, sub-threshold swing and DIBL, show that the gate-controllability of 3-D bending SF was much improved than a planar one. However, the trans-conductance (g_m) at the actual pixel operation conditions was more importantly considered in terms of pixel linearity and noise performances of sensors considering that SF amplifiers are operated at saturation mode,

In Figure 2(a), the fabricated bending SFs, 3D-SF (1), (2) and (3), were compared in terms of g_m with a fixed depth of vertical gate as $0.63\times W$, where W is the channel width of planar SF. It shows that the g_m in 3D-SF (3) was most improved up to 9% compared to the planar one. On the other hand, the 3D-SF (1) shows rather decreased g_m compared the planar one by 13% and the 3D-SF (2) shows comparable g_m to the planar one.

Then, the effective channel width, W_{eff}, was also estimated by using the Equation (1).

$$W_{eff} = \frac{L\cdot(g_m{}^2)}{2\mu C_{ox} I_{bias}} \qquad (1)$$

Assuming the channel length is constant in all structures, approximately ~20% of W_{eff} was improved in 3D-SF (3) compared to the planar one in Figure 2(a).

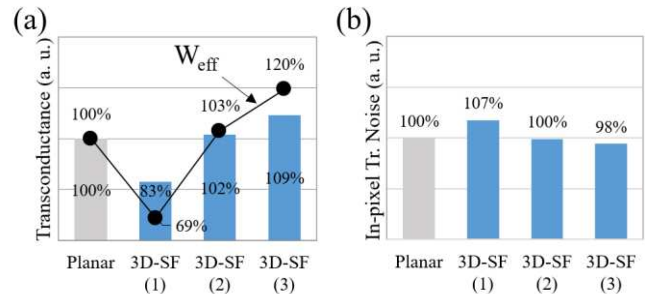

Figure 2. Comparison of (a) trans-conductance (g_m) and (b) total in-pixel transistor temporal noise between planar bending SF and 3D-bending SF (1)~(3) with a vertical channel depth of $0.63\times W$.

This result led to the improvements in noise performances. In Figure 2(b), only 3D-SF (3) shows ~2% of reduction of in-pixel transistor temporal noise. Meanwhile, other structures show comparable or rather increased noise level compared to the planar one. For the details, in 3D-SF (3), ~2% of thermal noise and ~1% of flicker noise were reduced compared to the planar one. Generally, the thermal noise and flicker noise are mainly

governed by g_m (∝~g_m) [7] and area *(~1/(W×L))* [7] of channel, respectively. Even though, the g_m and W_{eff} in test element above cannot be exactly same in actual pixel operation, this improvement is mainly understood by the improvement in g_m and W_{eff}. It implies that an appropriate gate structure, i.e. like 3D-SF (3), is needed to improve g_m the noise performance in bending SF.

The effective channel length (L_{eff}) and the consequential effective channel area also can be changed depending on the gate structure. However, considering a not uniform bending current density, it is hard to evaluate accurate values of them.

By using the optimized layout of 3D-SF (3), we further investigated the noise performance by increasing a depth of vertical gate. As the depth increase from *0.63×W* to *0.88×W*, the thermal noise and flicker noise were decreased by ~9% and ~4%, respectively, in Figure 3(a) and Figure 3(b). The total in-pixel temporal transistor noise was reduced approximately ~7% as the depth increase.

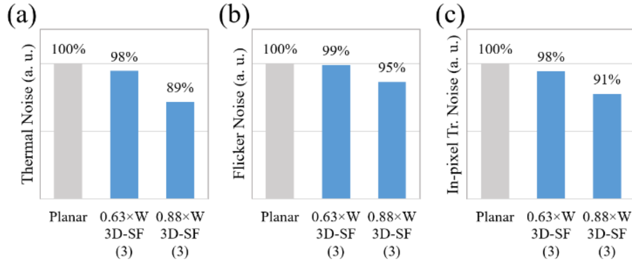

Figure 3. Comparison of (a) thermal noise, (b) flicker (*1/f*) noise, (c)) total in-pixel transistor temporal noise between planar bending-SF and 3D-bending SF (3) with a vertical gate depth of *0.63×W* and *0.88×W*.

These results are also shown in the distribution of pixel-by-pixel random noise in Figure 4 (a). The body of the pixel distribution is slightly narrower in *0.63×W* 3D-SF (3) than planar one. Then, it becomes narrower in *0.88×W* 3D-SF (3) and slightly left-shifted than planar one, which indicates the reduction of thermal noise. The tails of distribution also descend further as the depth increase, which suggest the flicker noise components are decreased.

The random telegraph signal (RTS) noise are also evaluated. Two consecutive frames of images were taken at a dark condition and the pixel-by-pixel output differences were plotted in histogram Figure 4 (b). First, the distributions near the zero difference was slightly reduced in 3D-SF (3) compared to planar one. And the slope of tails also becomes steeper in 3D-SF (3) than planar one, which means that the temporal current fluctuations have been lowered in 3D-SF (3). This can be understood by a general explanation of RTS *(~1/(W×L))* [8] and it corresponds to the improvement in flicker noise above.

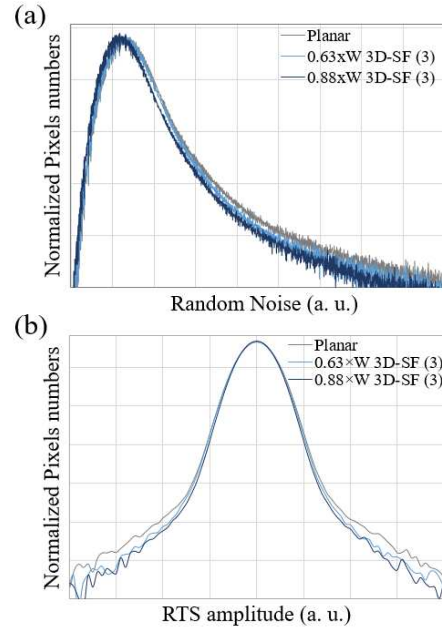

Figure 4. The distribution of pixel-by-pixel (a) temporal random noise (R.N.) and (b) Random telegraph signal (RTS) noise in comparison with planar bending-SF and 3D-bending SF (3) with a vertical gate depth of *0.63×W* and *0.88×W*.

In addition, we also evaluated the RTS noise in the wafer-level tests. In Figure 5, the RTS in y-axis represents the counted number of pixels in a chip that showed higher output differences than a certain criterion. In a wafer, the RTS of a considerable number of chips were obtained and the median value of them are presented in Figure 5.

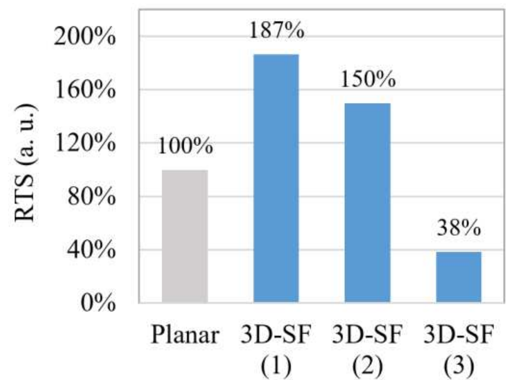

Figure 5. The wafer-level testing results of the Random telegraph signal (RTS) noise between planar bending-SF and 3D-bending SF (1)~(3) with a vertical gate depth of *0.63×W*.

In Figure 5(a), 3D-SF (3) shows ~38% of RTS value compared to the planar one. Meanwhile, 3D-SF (1) and (2) show much increased value. This dramatic result implies that 3D-SF (3) is promising option for a mass production of CIS chips.

IV. Conclusion

We firstly demonstrated a 3-D bending in-pixel SF transistor integrated into the submicron 4-T APS chip. By optimizing a 3-D gate structure suitable for a bending SF, the effective channel width of the SF transistor is maximized resulting in improved pixel noise characteristics without adversely affecting other pixel performance. This achievement may allow further scaling down of pixel pitch for the future image sensors of high-resolution applications without the inevitable deterioration of noise performance in a minimized SF area.

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Near-infrared sensitivity enhancement of silicon image sensor with wide incident angle

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***Abstract*—We proposed silicon-based image sensor with metal gratings and metal-filled deep trench isolation which improved near-infrared (NIR) sensitivity by plasmonic diffraction. The absorption efficiency was improved to 53% at an NIR wavelength 940 nm with 3-µm thick of silicon. Although, it has severe incident angle dependence of sensitivity, we devised the grating period and width to allow wide range for incident angle.**

Keywords—Si image sensor, metal grating, metal trench, surface plasmon, near-infrared

I. INTRODUCTION

Silicon complementary metal-oxide semiconductor (CMOS) image sensors have been applied not only in visible color imaging but also in near-infrared (NIR) imaging such as biological inspection, Time-of-Flight (ToF), surveillance, and fiber optic communication [1-5]. NIR wavelength of 940 nm is mostly used for near-infrared imaging because it is invisible to the human eye and is less affected by sunlight. However, silicon has low absorption efficiency in NIR. Therefore, improving NIR sensitivity is a significant issue for further advancement in NIR imaging technology using silicon CMOS image sensors.

Extending the effective absorption length in a limited thickness of silicon is one of the approaches to improve the sensitivity. It has been reported that silicon pyramid arrays and SiO_2 deep trench isolation (DTI) improved NIR absorption efficiency by the refraction of incident light and repetition of the reflection in silicon layer [6]. Polysilicon nano-grating has been proposed for light confinement in silicon absorption layer with the diffraction [7]. Thus, in recent years, NIR light sensitivity improvement techniques have been actively researched to extend the effective absorption length in silicon.

Our group has proposed silicon-based backside illumination (BSI) image sensor with metal gratings and metal-filled DTI which improved NIR sensitivity by plasmonic diffraction [8,9]. The diffraction efficiency is quite high as ~50% due to the electric field enhancement effect. The diffraction angle was approximately 90 degrees, namely around 80 degrees and the diffracted light was reflected by the metal DTI. Under this large diffraction angle, the effective propagation length dramatically increases in a limited thickness of silicon. Recently, we devised this construction to confine photons in silicon absorption layer, and the absorption efficiency was improved to 53% at an NIR wavelength 940 nm with 3-µm thick of silicon in simulation (Fig. 1) [10,11]. However, this technique is utilized for only normal incidence due to the wave-vector matching conditions of grating. Applying for image sensor pixels, a breakthrough is required to significantly expand the tolerance of the incident angle range. In this paper, we present how to improve the sensitivity with wide incident angles.

II. NEAR-INFRARED SENSITIVITY ENHANCEMENT

A. Plasmonic diffraction

Surface plasmon resonance is excited on a periodic metal grating by light irradiation. The incident photon energy couples with electron oscillation in metal. The resonant oscillation of electrons generates enhanced electric field on the surface of the metal. According to this energy coupling between photons and electrons, the incident light diffracts to horizontal direction, and propagates on the surface of the grating. The resonance wavelength for normal incidence is determined under the matching conditions between the wave vector of surface plasmon and the lattice vector of the metal grating.

We found that the incident light efficiently diffracted to transmission side (silicon side) with a large angle nearly 90 degrees by slightly changing the period of the grating that is corresponding to change the lattice vector. We call this condition quasi-resonance. Fig. 2(a) and Fig. 2(b) show the

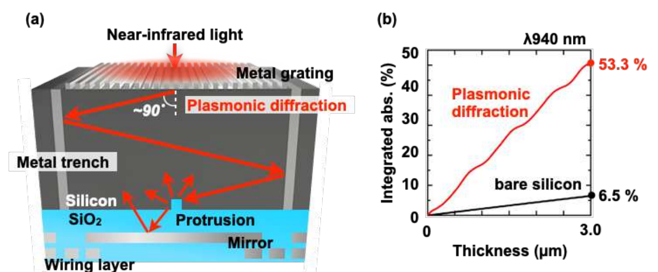

Fig. 1(a) Schematic diagram of the silicon-based image sensor with metal gratings and highly reflective metal DTI. The protrusion scattered photons and the mirror contributed to photon harvesting. (b) Silicon integrated absorption dependence on the silicon thickness [10].

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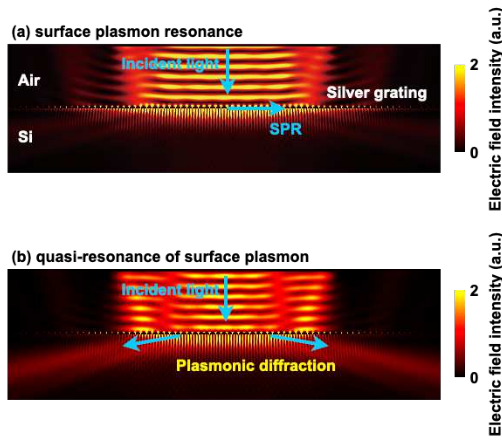

Fig. 2 Electric field intensity distributions in (a) surface plasmon resonance and (b) quasi-resonance of surface plasmon

electric field intensity distributions of a metal grating with the period for surface plasmon resonance condition and for the quasi-resonance condition, respectively. In Fig. 2(a), the incident light from the top excited surface plasmon resonance and the enhanced electric field was observed on the grating. In Fig. 2(b), the incident light diffracted by the grating to the silicon side.

The diffraction angle was about 80 degrees which was extremely high diffraction angle compared with conventional grating. The diffraction efficiency was achieved to ~50% by designing the grating period, width, and height [10-12]. Under the quasi-resonance of surface plasmon, the incident photon energy coupled with the electron oscillation. Re-radiation of the electric dipoles contributed to both high diffraction angle and high diffraction efficiency, that we named "plasmonic diffraction".

B. *Near-infrared sensitivity enhancement for Si image sensor*

NIR sensitivity was drastically improved by applying the plasmonic diffraction to silicon CMOS image sensor [8-12]. Our proposed construction of image sensor is back-illuminated silicon image sensor pixel with silver grating, silver trench, SiO_2 protrusion, and cupper mirror. Fig. 3 shows the simulation result of electric field intensity distribution. The incident wavelength was set to 940 nm. The structural

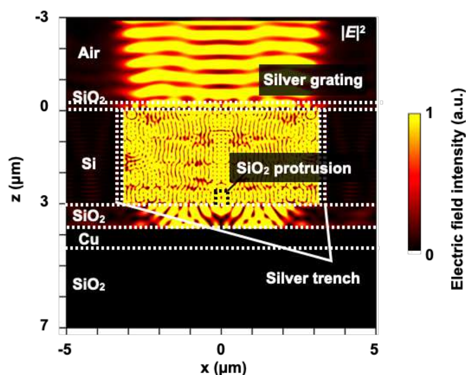

Fig. 3 Simulation result of electric field intensity distribution for photon confinement in silicon absorption pixel using silver grating, silver trench, SiO_2 protrusion, and Cu mirror.

parameters of silver grating were period (p): 265 nm, width (w) 230 nm, and height (h): 85 nm. The plasmonic diffraction light was reflected by the silver trench. The effective absorption length in a limited thickness of 3-μm silicon was extended by confining the photons in silicon absorption layer.

III. Incident Angle Management

Fig. 4 shows the incident angle dependence of the silicon absorption efficiency. The highest absorption efficiency appeared at the incident angle of 0 degree, and the absorption efficiency was drastically dropped over 10 degrees of incidence. Therefore, the incident allowance angle for the proposed image sensor was limited in ±5 degrees. Sensitivity enhancement with wide incident angle is a crucial issue for image sensor with plasmonic diffraction.

The NIR sensitivity for silicon image sensor will be enhanced in the central area of sensor pixels by plasmonic diffraction technique, but the sensitivity will decrease at the area near the edge of sensor because of the angled chief ray. Severe sensitivity enhancement limitation in incident angle is caused by the wave vector matching conditions. From the viewpoint of improving the sensitivity to the angled chief ray, we managed for wide range of incident angles by changing the grating period and width in each pixel toward the edge of the sensor (Fig. 5).

Fig. 6 shows the plasmonic diffraction in each optimized

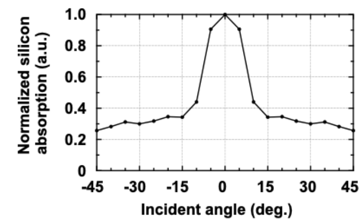

Fig. 4 Simulation result of silicon absorption efficiency dependence on the incident angle.

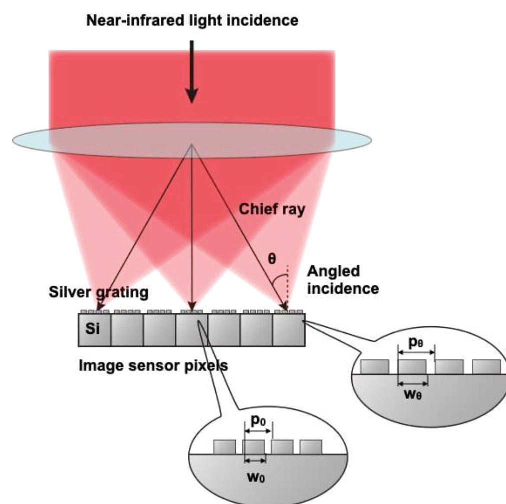

Fig. 5 Schematic image of gradual variation of the period and width of silver grating on silicon image sensor according with angled chief ray incidence. Set (p_0, w_0) and (p_θ, w_θ) were optimized to 0 degree and θ degree incidence, respectively.

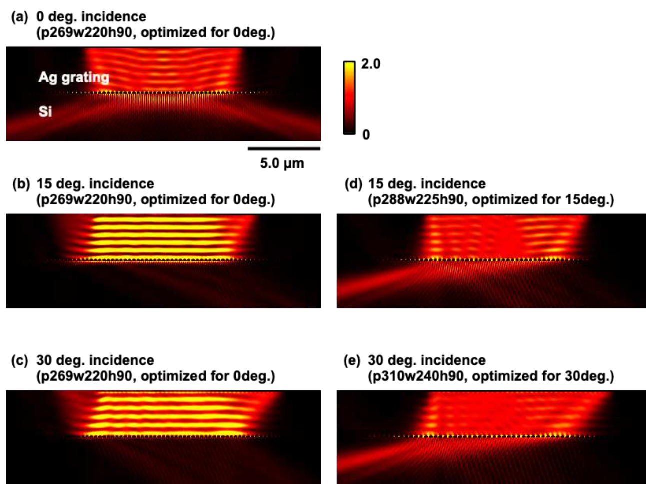

Fig. 6 Simulation results for the plasmonic diffraction with various incident angles. (a)-(c) silver grating was optimized for normal incidence, (d) optimized for 15 degrees of incidence, and (e) optimized for 30 degrees of incidence.

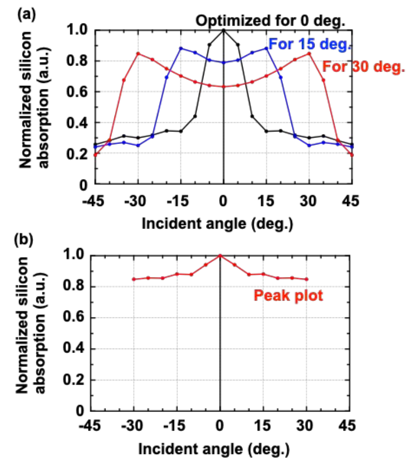

Fig. 7 Simulation results of the normalized silicon absorption efficiency dependence on the incident angle.

parameters for the various incident angles 0, 15, and 30 degrees to keep the absorption efficiencies for wide incident angle. Here, the height of the silver grating was fixed at 90 nm. Although the width and height of the grating will be variable in optimization for each incident angles, it is difficult to change the height in each pixel in the sense of the fabrication process. Lateral patterning parameters such as period and width are easily controlled by mask lithography patterning, but the vertical parameter of height should be the same considering the silver layer formation process. Fig. 6(a)-(c) shows the plasmonic diffraction behavior with parameters of p269 nm, w220 nm, and h90 nm in 0, 15, and 30 degrees of incident angles, which was optimized for 0 degree of incident case. In Fig. 6(a) of normal incidence, incident light diffracted to Si with large diffraction angle. On the other hand, in Fig. 6(b) and 6(c), plasmonic diffraction was not observed and the incident light was reflected back. When the parameters were changed to p288 nm, w225nm, and h90 nm, the angled incident light with 15 degrees diffracted to one side with large diffraction angle. This diffraction will contribute to the absorption enhancement in Si due to the extension of the absorption length (Fig. 6(d)). With the same analogy, the parameters were optimized to p310 nm, w240 nm, and h90 nm for the incident angle at 30 degrees. In Fig. 6(e), the diffraction light was observed in 30 degrees of incident light.

Fig. 7 shows silicon absorption efficiency dependence on the incident angle in each optimized grating parameters. The absorption efficiency was normalized by a peak value at 0 degree of the optimized grating for the normal incidence. In Fig. 7(a), the optimized gratings for 15 and 30 degrees of the incidence exhibited a peak at 15 and 30 degrees, respectively. Fig. 7(b) shows peak plot of the silicon absorption efficiency dependence on the incident angle. By applying each optimized grating parameters for each incident angle, normalized silicon absorption efficiencies were maintained more than 80% in the incident angle range ±30 degrees with 3-µm thick of silicon.

IV. Conclusions

Our proposed silicon-based image sensor with silver gratings and silver filled trench improved NIR sensitivity by plasmonic diffraction which extends the effective absorption length in a limited thickness of silicon. The period, width, and height of silver grating were optimized to efficiently diffracts the incident light with large diffraction angles. Although the incident allowance angles were limited in ±5 degrees because of the wave-vector matching conditions, we clarified that sensitivity improvement by our proposed construction maintained high efficiency between ±30 degrees of incidence by changing the grating period and the width according to each incident angles of chief ray.

Acknowledgment

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Light Intensity and Charge Holding Time Dependence of Pinned Photodiode Full Well Capacity

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In this paper, light intensity and charge holding time dependence of pinned photodiode (PPD) full well capacity (FWC) are studied for our pixel structure with a buried overflow path under the transfer gate. The formula for the PDFWC derived from a simple analytical model has been successfully validated by the technology computer-aided design (TCAD) device simulation and actual device measurement.

I. INTRODUCTION

High dynamic range (HDR) is one of the most important characteristics of recent CMOS image sensors. To achieve over 100dB DR, a lateral overflow integration capacitor (LOFIC) scheme[1-2] and a triple quantization digital pixel sensor[3-4] have been developed.

In these sensors, one of the factors to define the performance at the mode transition points, such as signal-to-noise ratio and linearity, is PDFWC[1].

During the course of our HDR sensor development, we have found that the PDFWC increases as the incident light intensity increases, as shown in Fig. 1 (a). Also, we have known that PDFWC decreases as the time interval between the exposure end of pulsed light and the signal readout, which is referred to as the charge holding time, increases, as shown in Fig. 1 (b). Pulse timing diagrams to obtain the results shown in Fig. 1 (a) and (b) are shown in Fig. 2.

Though analytical models for such dynamic behaviors of the PDFWC have been proposed in the literatures [5-11], minor modifications are needed for our pixel[3-4], because of its unique structure with the buried overflow path under the transfer gate. In this paper, we attempt to understand both the light intensity dependence and the charge holding time dependence of our PPD pixel by simple analytical modeling, TCAD simulations, and measurements.

II. ANALYTICAL MODEL

Contrary to the conventional PPD pixel structure, a buried overflow path has been implemented in our device [3-4]. Its cross-sectional structure and a potential diagram along the z-z' line are shown in Fig. 3. In this structure, the previously reported PDFWC models[5-11] are not applied as they are. The simple model for theoretical analysis is shown in Fig. 4, where three components, the photo-generated current I_{ph}, the intrinsic diode current I_{PPD}, and the overflow current I_{of}, are considered[6].

Models which present the basic concept of our analysis are shown in Figs. 5 and 6. Fig. 5 shows potential changes from the PD reset to high illuminance PD saturation with static light, and Fig. 6 shows potential changes from high illuminance PD saturation to the equilibrium with long t_{hold}.

a. Light Intensity Dependence

Referring to Figs. 3 and 4, formulae for the light intensity dependence of PDFWC will be derived. The photo-generated current I_{ph} and the intrinsic PD current I_{PPD} are formulated, respectively, by

$$I_{ph} = q \cdot R \cdot P \qquad -(1)$$

where q, R and P denote the unit electron charge, the responsivity, and the face-plate illuminance, respectively, and

$$I_{PPD} = I_{sat} \cdot \left\{ e^{\left(\frac{-V_S}{V_T}\right)} - 1 \right\} \qquad -(2)$$

where I_{sat}, V_S, and V_T are the PN junction current at reverse bias condition, the PD potential, and the thermal voltage ($=kT/q$), respectively. If we assume the reverse bias condition with $|V_S| \gg V_T$, in eq. (2), I_{PPD} is approximated by $-I_{sat}$. Then, the overflow current I_{of} is formulated by

$$I_{of} = I_0 \cdot e^{\left(\frac{-\Delta V_b}{n \cdot V_T}\right)} \qquad -(3)$$

where ΔV_b , I_0, and n denote the barrier height between the PD and the overflow path (i.e., $V_S - V_{of}$), the overflow current that would flow at $\Delta V_b = 0$, and the non-ideality factor, respectively. Under the PD saturation conditions, the input and the output currents should be balanced. Therefore, the following relationship holds.

$$I_{ph} = I_{of} + I_{PPD} \qquad -(4)$$

From eq. (1)-(4), the minimum PD potential under PD saturation is given by

$$V_{S_min} = V_{of} - n \cdot V_T \cdot ln\left(\frac{I_{sat}}{I_0} + \frac{qR}{I_0}P\right) \qquad -(5)$$

Eq. (5) shows that V_{S_min} decreases to flow larger I_{of} when I_{ph} increases.

On the other hand, PDFWC is expressed as

$$N_{FWC} = \frac{C_{PD}}{q}\left(V_{pin} - V_{S_min}\right) \quad -(6)$$

From eq. (5) and (6), PDFWC is given by

$$N_{FWC} = \frac{C_{PD}}{q}\left\{V_{pin} - V_{of} + n \cdot V_T \cdot ln\left(\frac{I_{sat}}{I_0} + \frac{qR}{I_0}P\right)\right\} \quad -(7)$$

Therefore, PDFWC is a function of face-plate illuminance P, and it increases logarithmically with the face-plate illuminance. The equilibrium PDFWC[6-8], N_{FWC_eq}, for our pixel structure is obtained from eq. (7) with $P=0$.

$$N_{FWC_eq} = \frac{C_{PD}}{q}\left\{V_{pin} - V_{of} + n \cdot V_T \cdot ln\left(\frac{I_{sat}}{I_0}\right)\right\} \quad -(8)$$

The equilibrium PDFWC is PDFWC with the equilibrium condition between the n-layer and the V_{of} barrier of PD.

b. Holding Time Dependence

As shown in Fig. 2(b), $I_{ph} = 0$ during t_{hold}. The PD potential change during t_{hold} is formulated by

$$\frac{dV_S}{dt} = \frac{I_{out}}{C_{PD}} - \frac{I_{in}}{C_{PD}} = \frac{(I_{of}+I_{PPD})}{C_{PD}} - \frac{I_{ph}}{C_{PD}} = \frac{I_0 \cdot e^{\left(\frac{-\Delta V_b}{n \cdot V_T}\right)} - I_{sat}}{C_{PD}} \quad -(9)$$

Solving eq. (9) yields the PD potential as

$$V_S = V_{of} + n \cdot V_T \cdot \ln\left\{e^{\left(-\frac{I_{sat}}{C_{PD} \cdot n \cdot V_T}t + A\right)} + \frac{I_0}{I_{sat}}\right\} \quad -(10)$$

where A is a constant. With eq. (6), PDFWC is obtained as

$$N_{PD} = \frac{C_{PD}}{q}\left[V_{pin} - V_{of} - n \cdot V_T \cdot \ln\left\{e^{\left(-\frac{I_{sat}}{C_{PD} \cdot n \cdot V_T}t + A\right)} + \frac{I_0}{I_{sat}}\right\}\right] \quad -(11)$$

Therefore, PDFWC is a function of the charge holding time $t(=t_{hold})$, which demonstrates PDFWC has charge holding time dependence. When t is very long, eq. (10) becomes

$$V_S = V_{S_long} = V_{of} - n \cdot V_T \cdot \ln\left(\frac{I_{sat}}{I_0}\right) \quad -(12)$$

From eq. (6) and (12),

$$N_{PD_long} = \frac{C_{PD}}{q}\left\{V_{pin} - V_{of} + n \cdot V_T \cdot \ln\left(\frac{I_{sat}}{I_0}\right)\right\} \quad -(13)$$

Eq. (13) is identical to eq. (8), which demonstrates the PDFWC after long t_{hold} (N_{PD_long}) also reaches N_{FWC_eq}. The potential changes during this process are shown in Fig. 6. During the charge holding period, I_{of} draws the charges from PD to FD and finally I_{of} becomes equal to I_{sat}, reaching the equilibrium condition.

III. EXPERIMENTAL VALIDATION

The simulation set-up, simulated $I_{of} - \Delta V_b$ curves, and potential along the x–x' line as a function of the PD potential V_S, are shown in Fig. 7 (a), (b), and (c), respectively. In this simulation, electrons are injected into PD from the inserted PD electrode. With these $I_{of} - \Delta V_b$ curves, the relation between ΔV_b and I_{of} was confirmed.

Fig. 8(a) shows another simulation set-up for light intensity dependence (Fig. 9) and charge holding time dependence (Fig. 10) of PDFWC. The PD electrons are generated by an external light source in this simulation. Fig. 8(b) shows the photo-response curve. In the PD saturation region, it is obvious that eq. (4) holds with $I_{of} \gg I_{PPD}$.

Fig. 9 shows the light intensity dependence of PDFWC and PD potential. The simulation result of (a) and eq. (5) agree well, and the simulation result of (b) and eq. (7) reproduce the measurement result.

Fig. 10 shows the t_{hold} dependence. The simulation result of (a) agrees well with eq. (10). Eq. (11) reproduces the measurement result, as shown in (b). Figs. 9(c) and 10(c) show potential changes from PD reset to PD saturation and potential changes from PD saturation to equilibrium PDFWC, respectively. The black and dashed gray lines show the PD potentials under the fully depleted condition, and low illuminance saturation or after a long t_{hold}, respectively.

The potential distributions at low illuminance saturation and after long t_{hold}, as shown with the dashed gray lines of Fig. 9(c) and Fig. 10(c), are re-plotted in Fig. 11. It is understood that the equilibrium PDFWC condition is reached in both cases.

IV. CONCLUSION

In this paper, the light intensity dependence of PDFWC and the PD charge reduction phenomenon during the charge holding time have been formulated. They were verified with TCAD simulations and measurement results for our pixel with a buried overflow path. During the charge integration period, electrons flowing into and those flowing out from the PD should be balanced. Therefore, the potential barrier between the PD and the overflow path is a function of input light intensity. It decreases with the light intensity logarithmically, increasing the PDFWC logarithmically. For both cases where the signal charges remain in the PD at dark before they are read out, and where the light intensity is close to zero, PDFWC becomes identical to the equilibrium FWC.

V. ACKNOWLEDGMENT

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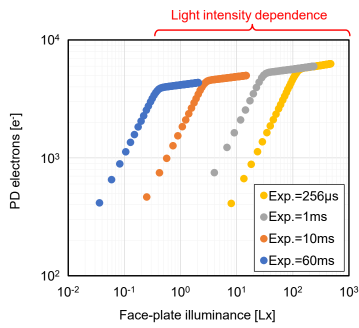
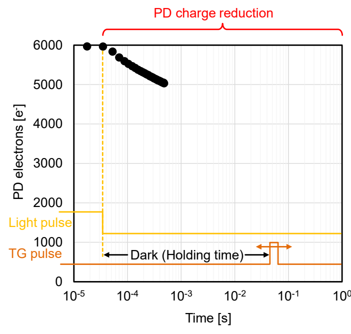
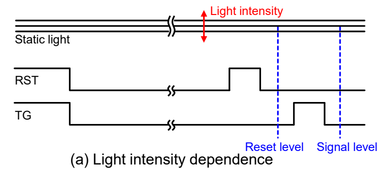




(a)Photo-conversion characteristics (b) PDFWC dependence on the t_{hold}

Fig. 1 Measured dynamic behaviors of PPD.



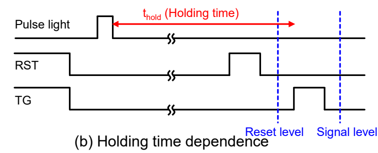
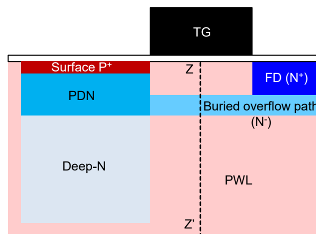


Fig. 2 Pulse timing for evaluation.



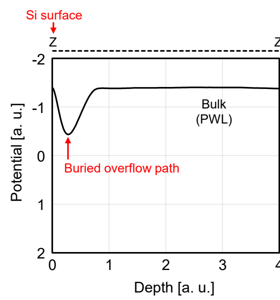


Fig. 3 PD cross-section and potential of the buried overflow path.

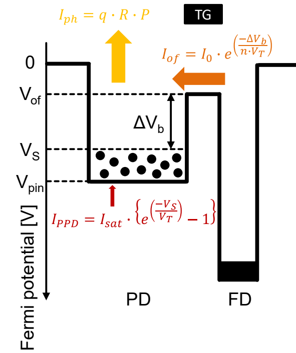


Fig. 4 Simple model for theoretical analysis.

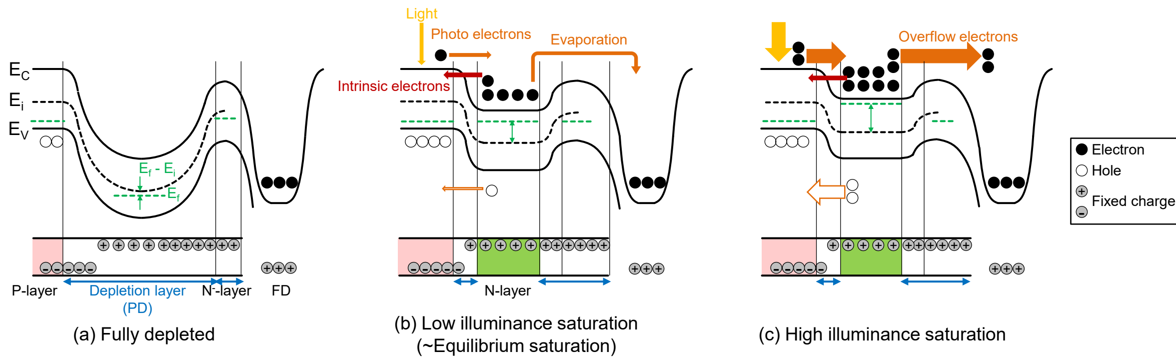


Fig. 5 A simple model of potential changes from PD reset to PD saturation.

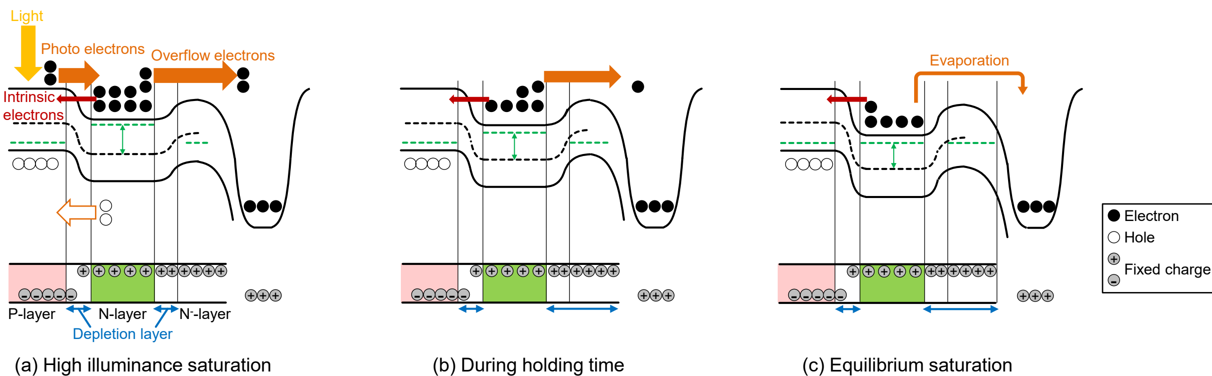
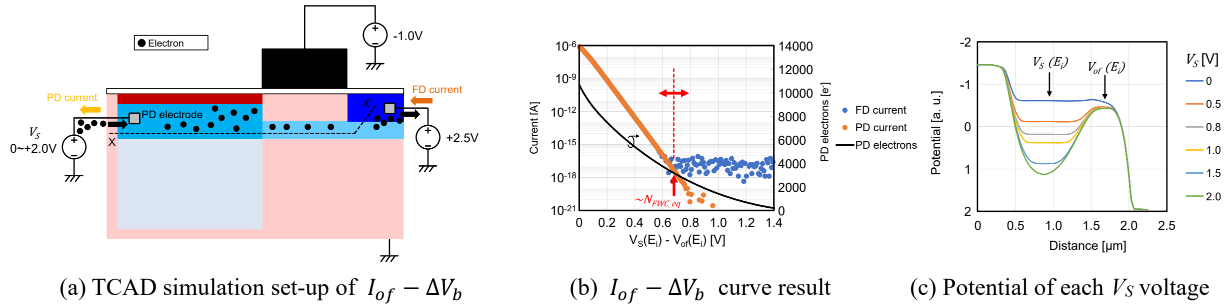
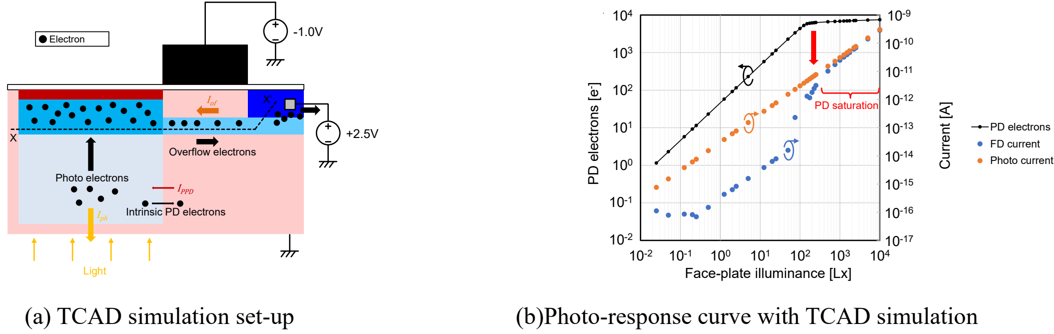


Fig. 6 A simple model of potential changes from PD saturation to equilibrium PDFWC.



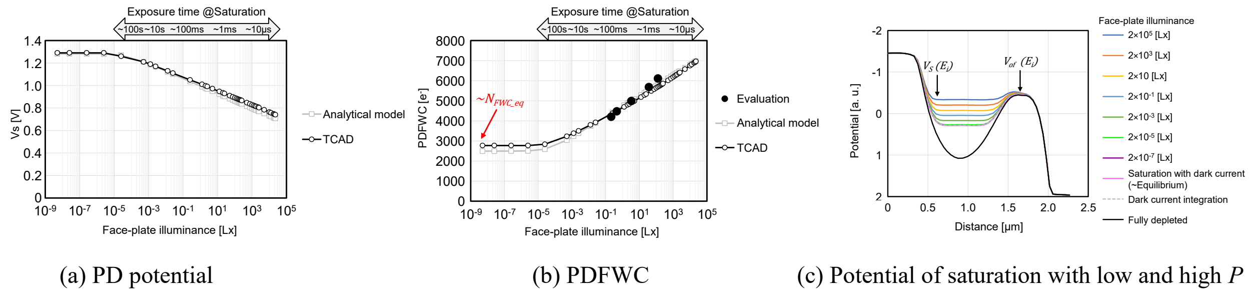
(a) TCAD simulation set-up of $I_{of} - \Delta V_b$ (b) $I_{of} - \Delta V_b$ curve result (c) Potential of each V_S voltage

Fig. 7 Relation between ΔV_b and I_{of} with TCAD simulation.



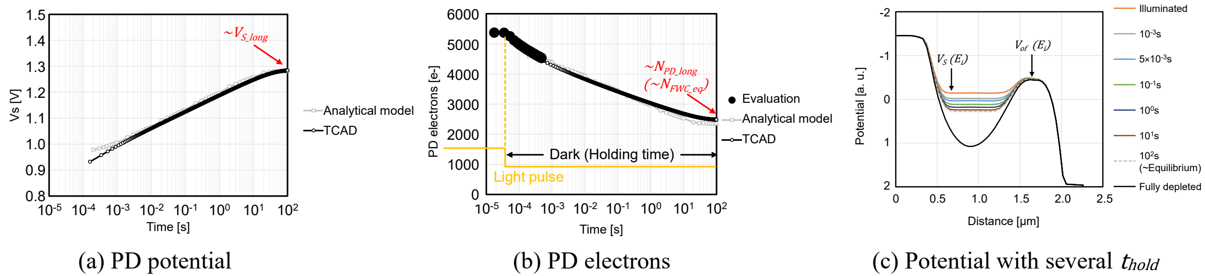
(a) TCAD simulation set-up (b)Photo-response curve with TCAD simulation

Fig. 8 TCAD simulation and evaluation set-up for light intensity (Fig. 9) and charge holding time (Fig. 10) dependence.



(a) PD potential (b) PDFWC (c) Potential of saturation with low and high P

Fig. 9 PDFWC with various light intensity conditions.



(a) PD potential (b) PD electrons (c) Potential with several t_{hold}

Fig. 10 PDFWC with long charge holding time.

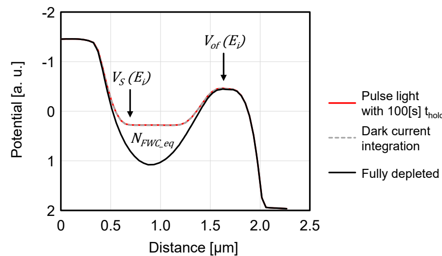


Fig. 11 Equilibrium PDFWC potential with TCAD

Improved QE in CMOS image sensors with nano-black antireflection layer

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***Abstract*— A novel anti-reflection process is demonstrated which improves the quantum efficiency (QE) of a CMOS image sensor, with particular benefits at the ultraviolet (UV) and near infrared (NIR) ends of the electromagnetic spectrum. Also, the dark current and photoresponse non-uniformity (PRNU) were reduced to about 33% and 55%, respectively, of the values for a conventional control sensor. The nano-black anti-reflection layer was made using a reactive-ion-etch technique to form nano-scale spikes at the surface which greatly reduce the reflectivity of the surface, which has a matt-black appearance. The sensor used, a CIS115 from Teledyne-e2v, is a back-side-illuminated (BSI) device with ≈10 µm active silicon thickness and 2000 × 1504 pinned photodiode pixels with a pitch of 7 µm. The improved QE is most impressive at UV wavelengths, below 400 nm, where the QE increases towards 100%, although no correction was made for an increased electron generation rate, as this is not easily quantified. This high QE result is compared with a conventional antireflection (AR) coating which shows a steep drop in QE below 400 nm. There is also an improvement in QE in the NIR (from 700 nm to 1100 nm) for the nano-black sensor, and this is despite the approx. 1 µm thinning of the silicon by the etching process, which would normally reduce the QE. Some of the QE improvement may be the result of increased scattering of the incident light, which is supported by the reduced PRNU.**

Keywords — image sensor, CMOS, quantum efficiency, antireflection coating

I. INTRODUCTION

Silicon image sensors are prone to poor QE at UV wavelengths because conventional surface passivation tends to be thicker than the absorption depth (only a few nm). Whereas at NIR wavelengths, the absorption depth required is 10s to 100s of µm, so thick layers are required. The CIS115 sensor [1] used in this work was optimised for high QE in the visible range and for high spatial resolution, so its active silicon thickness of 10 µm is not very suitable for NIR use. However, an anti-reflection process which improves QE at both ends of the visible spectrum would enable more applications for conventional CMOS sensors, which are the world's widest used image sensor technology.

The nano-black process has previously demonstrated high QE in discreet photodiodes [2]. To the authors' knowledge, this is the first time that such a process has been applied to a monolithic CMOS image sensor. The nano-black anti-reflection layer was fabricated without modifying the standard BSI process, as a last step, in place of applying an AR coating. The nano-black fabrication process is a low-temperature (-120 °C) reactive-ion plasma etch which produces a nano-structured surface of closely spaced spikes with average height 500 nm and width 100 nm. This surface then receives a conformal coating of 20 nm Al_2O_3, deposited by atomic layer deposition, with negative surface charge to provide a suitable electric field in the sensor. Fig. 1a shows an electron micrograph of the nano-structured silicon surface, the spike shapes cause multiple reflections between the structures, and this allows a gradual change in refractive index as light approaches the surface, improving the light absorption. Fig. 1b shows a CIS115 sensor with nano-black layer covering the lower half of the pixel array.

For QE measurements, nano-black sensors were compared to control sensors with a conventional multilayer AR coating for visible light. UV AR coatings were available [1], [3], but their QE was limited to 60% at UV and visible wavelengths, so the visible optimised AR coating (named by the manufacturer as multilayer-2) was chosen as a more suitable comparison.

For the dark current and PRNU measurements, comparison was made using a sensor where the nano-black

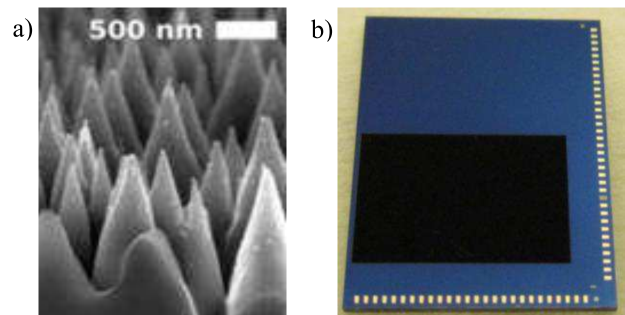

Figure 1. (a) electron micrograph of the nano-black surface, reproduced from [2], (b) nano-black layer on lower half of a CIS115 sensor

This work was funded by the European Space Agency (ESA) under contract No. 4000135291/21/NL/GLC/ov (Nano-Black Coating on Silicon CMOS Image Sensors for Extreme Sensitivity)

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process was performed on only one half of the pixel array surface, the other half having the control CIS115 BSI passivation consisting of a shallow boron implant, laser anneal and anodization, but coated with the 20 nm Al_2O_3 layer and having no AR coating.

During all measurements, the sensors were mounted in a vacuum chamber, and the temperature was controlled to 20 °C with a stability within ±0.05 °C, using a water-cooled thermoelectric cooler (TEC).

II. Experimental Results

A. QE measurements

Quantum efficiency (QE) is the percentage ratio of the number of photogenerated electrons N_e measured for a given number of incident photons N_p of specified wavelength λ:

$$QE(\lambda) = \frac{N_e(\lambda)}{N_p(\lambda)} \times 100\%. \quad (1)$$

QE measurements were taken in the wavelength range 300 nm to 1100 nm, in 20 nm steps, following a procedure established for a previous work [4]. Ten images were averaged for each measurement to reduce noise. Dark images were subtracted from lit images at each wavelength. Because of the wavelength-dependency of the intensity of the light source, the throughput of the optical components, and the device QE, integration times were optimised for each wavelength to keep the signal below saturation (ideally at ½ full well capacity) and for low signals the integration time was limited to 25 s, to prevent dark current becoming significant.

To perform the QE measurement, the optical system was assembled as shown in Fig. 2. An aperture mask was positioned in front of the sensor, its circular opening was offset from the pixel-array centre, and depending on the orientation of the clamp, the aperture could be either in the upper or lower half of the pixel array. The diameter of the beam reaching the sensor was chosen so that only negligible numbers of photons fell outside the edge of the pixel array.

A measurement with photodiode #2 behind the aperture in the focal plane of the DUT was used for reference measurements. The photodiode active area (with 9.5 mm diameter) was overlaid on the sensor image to check the beam position and was used as the region of interest (ROI) for QE calculations. Because the vast majority of the photons are concentrated within the aperture region, which is smaller than the photodiode area, the DUT and photodiode #2 capture the same number of photons. For calibration, readings from reference and monitor photodiodes were recorded simultaneously and used to calculate the throughput ratio (at each wavelength) of the focal plane versus the monitoring

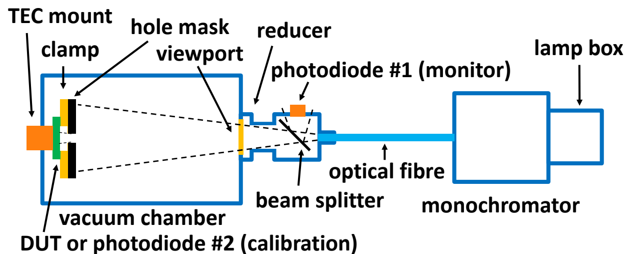

Figure 2. Experimental setup for QE measurements, for PRNU the beam splitter was replaced by a 50% ND filter

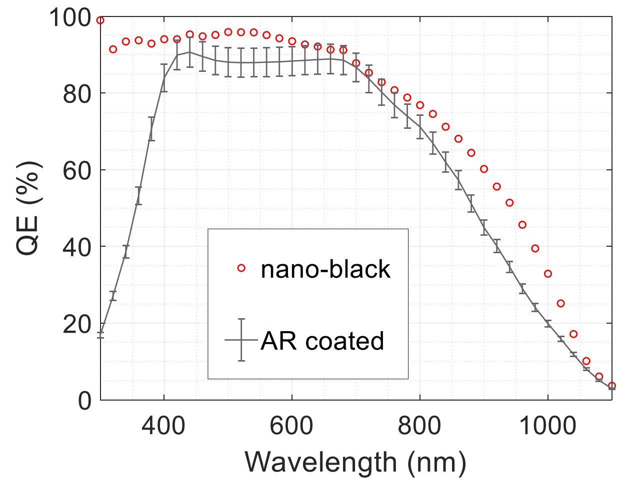

Figure 3. QE results, comparing a nano-black sensor (red circles) to the control AR coated sensor (gray curve with error bars).

location (at the beam splitter) i.e. photodiode #2 : photodiode #1. This was then used to infer the power density of photons at the focal plane from photodiode #1 readings taken whilst the DUT was in position.

A nano-black sensor is compared to the AR coated control in Fig. 3. The experimental error in the QE results is about 4%, as indicated by error bars for the control sensor (error bars are not shown for the nano-black sensor to aid clarity). The nano-black QE results are higher across most of the wavelength range, but the increase in QE is greatest at the UV end of the spectrum, because for the AR coated sensor the QE drops sharply for wavelengths below 400 nm. QEs greater than 100% are a result of higher quantum yield, i.e. more than one electron generated per photon which occurs for wavelengths below ≈330 nm.

B. X-ray calibration

An X-ray calibration of system-gain was performed for each sensor, using an Fe-55 source, taking an average of 1000 frames collected using an integration time of 2 s, with dark frames subtracted. The system-gain was used to convert the digital numbers (DN), output by the electronics, to the number of electrons that were collected in each pixel. System-gain was close to 1.8 DN/electron for all the sensors tested.

C. Photoresponse non-uniformity (PRNU)

For the PRNU measurements, the optical setup was modified from that shown in Fig. 2 to obtain an improved flat-field illumination. The beam splitter of the QE setup was removed because it had a fine speckled pattern of reflective material (for wide bandwidth of reflectivity) which caused non-uniform illumination. A neutral density (ND) filter was used instead, with a 50% transmission to match the previous beam splitter. The PRNU is a measure of how the pixel signal varies across the pixel array for a flat-field illumination. In practice it is difficult to achieve perfectly flat-field illumination, so a local moving mean was taken of the surrounding pixels in a 25 × 25 pixel square. The measurements mostly used monochromatic illumination at a wavelength of 500 nm, except for the wavelength sweep results of Fig. 5. Ten images were averaged for each measurement to reduce noise and dark images were subtracted from lit images.

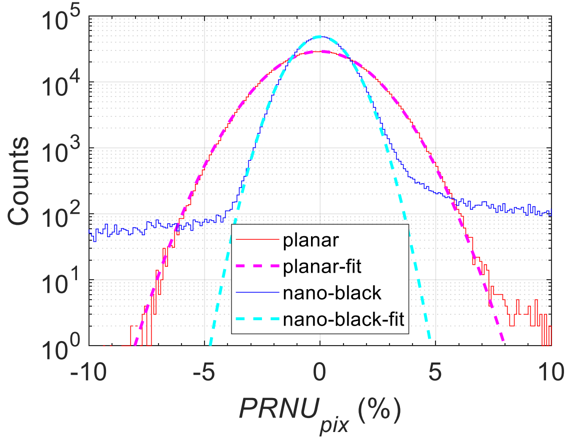

Figure 4. Histogram of $PRNU_{pix}$ for planar and nano-black regions of sensor with gaussian fits

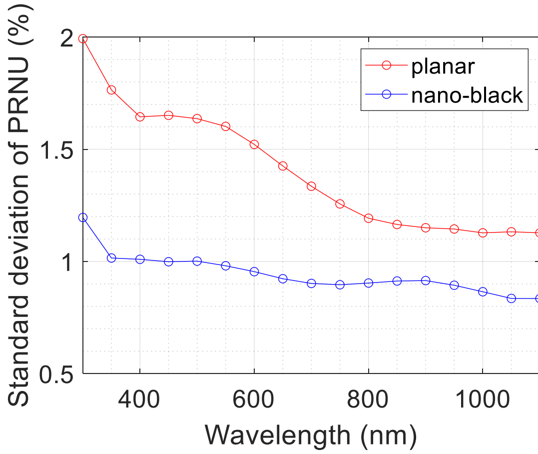

Figure 5. PRNU versus wavelength for sensor, showing comparison of the planar and nano-black regions.

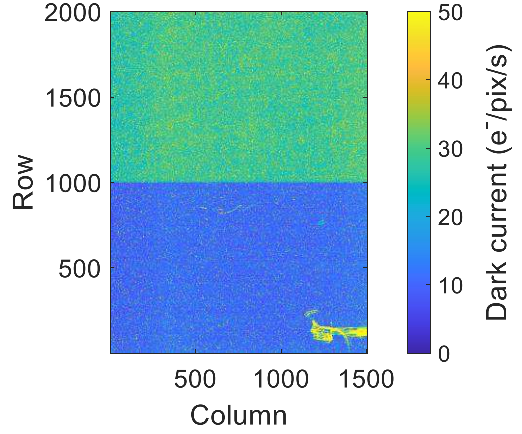

Figure 6. Dark current pixel map of sensor. Upper half: planar; lower half: nano-black

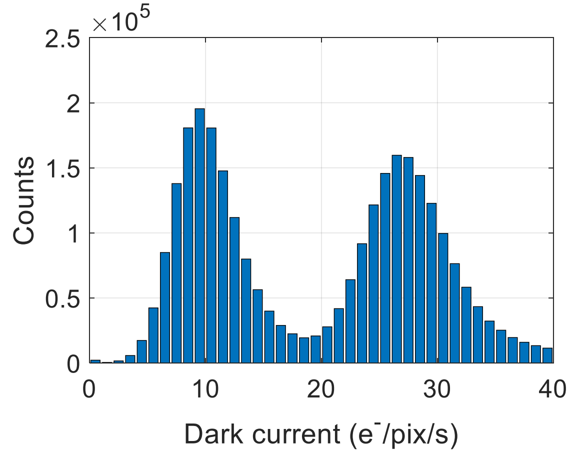

Figure 7. Dark current histogram at 20 ℃ of full pixel array, showing the nano-black region (left peak) and the planar region (right peak).

The $PRNU_{pix}$ contribution of each pixel was calculated according to [5] ignoring the first 4 rows and cols of the image area:

$$PRNU_{pix} = \frac{V_{si} - V_a}{V_a} \times 100\% \qquad (2)$$

where V_{si} = individual pixel signal and V_a = local mean signal. The sensor PRNU was calculated from the standard deviation of a Gaussian fit to the $PRNU_{pix}$ histogram, to reject the non-gaussian data of defective pixels. The lit images were taken in the linear range of operation, for an integration time of 0.7 s, corresponding to about 1/2 full well capacity.

Measurements were taken using a sensor divided into two regions, with a nano-black surface for one half and the planar control BSI passivation (without AR coating) for the other half of the chip. The $PRNU_{pix}$ for the two regions is shown using histograms in Fig. 4. The standard deviation of the Gaussian fits, giving the sensor PRNU were 1.0% for the nano-black region and 1.8% for the planar region. The nano-black histogram has higher shoulders (at a count of around 100) where the distribution becomes non-Gaussian because of a scratch in the surface causing more defective pixels (this scratch can be seen in the dark current pixel map of Fig. 6).

The sensor PRNU was also measured for varying wavelength as shown in Fig. 5. The PRNU is lower at all wavelengths for the nano-black region of the chip, compared to the planar region. PRNU is highest for both regions at the shortest wavelengths.

D. Dark Current

Ten images were taken for each of a set of integration times (between 0.1 s and 1 s), the first image was rejected to eliminate effects of lag and the median was taken of the other nine, the order of the varying integration time images was also randomised to reduce systematic errors. This process was repeated three times and further averaged to suppress noise. Using the X-ray calibration, the dark current for each pixel was converted to units of e^-/pix/s.

The dark current was measured at 20 °C using a sensor which had half of its surface with the nano-black process, the other half had a planar surface with the control BSI passivation consisting of a shallow boron implant and anneal, but no AR coating. Fig. 6 shows a pixel map of the dark current for the sensor. In Fig. 7, the histogram of pixel signals from the sensor has 2 peaks, at 9 and 27 e^-/pix/s for the nano-black and planar regions, respectively. These results show that the nano-black region clearly has lower dark current than the planar region.

III. Summary & Conclusions

When compared to the control CIS115s, with a conventional multilayer AR coating, the nano-black sensors

had higher QE for most of the wavelength range measured (300 nm to 1100 nm), but the greatest improvements were for UV (below 400 nm) and NIR (from 700 nm to 1100 nm) wavelengths.

The high QE at short wavelengths is consistent with results for discreet nano-black photodiodes [2] and is attributed to a combination of low reflectivity, good absorption and a quantum yield greater than one, i.e. more than one electron produced per photon. The control CIS115's AR coating was not UV optimised, which contributes to its sharp cut-off in QE below 400 nm. Also, its conventional back surface passivation is thicker than the nano-black's Al_2O_3 passivation, so the thin Al_2O_3 layer may in-part be responsible for the improved QE in the UV.

For high QE in the NIR, a relatively thick active silicon is required. The CIS115 is only 10 µm thick, which is approximately equal to the absorption length at 800 nm wavelength, and explains the drop-off in QE beyond 700 nm. The relative improvement in QE in the NIR for the nano-black sensor is despite the approximate 1 µm thinning of the silicon by the nano-black etching process, which would normally reduce the QE. However, some of this improvement may be attributed to increased light scattering, as indicated by the reduced PRNU.

Dark current and PRNU were reduced in nano-black sensors compared to a conventional planar BSI control. Dark current was 33% of that for the planar control. PRNU was 55% of that for the planar control.

We believe that the low PRNU of the nano-black surface compared to the planar surface is indicative of increased scattering of light, which smooths-out non-uniformities between pixels. The higher QE of the nano-black surface, particularly at longer wavelengths where the QE improvement is more modest, could also be related to the reduced PRNU because scattering could result in an increased probability of light transmission at the surface and may also be detrimental to spatial resolution.

In this work it was shown, for first time, that the nano-black process can be used in place of conventional AR coatings for CMOS image sensors, and can be performed as a final step after CMOS fabrication and back-thinning. The commercial viability of the nano-black process depends upon addressing concerns about the ability to clean a non-planar surface and difficulties in handling during packaging, but the improved QE and reduced dark current are good reasons to further pursue this technology.

Acknowledgment

The authors thank Simon Pyatt of The University of Birmingham, UK for wire-bonding of the image sensors.

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A customized 110nm CMOS process for large-area radiation detection and imaging

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ABSTRACT

This contribution presents a customized 110nm CMOS process tailored for the fabrication of pixel sensors on fully-depleted High-Resistivity (HR) substrates for radiation imaging applications. The test devices integrated in the first two fabrication runs, having three different values of active thickness, 48µm, 100µm and 200µm, are described, and the main results obtained from their electrical and functional characterization are summarized.

INTRODUCTION

Efficient charged-particle and X-ray direct detection require thick semiconductor sensors, and the mainstream solution for a wide range of applications are hybrid pixel detectors [1]. CMOS-integrated Monolithic Active Pixel Sensors provide a cost-effective alternative, but their efficient implementation requires a customization of the process and several trade-offs in detector performance [2-3]. Combining low-capacitance sensing node with thick active substrates and fast charge collection is a particularly challenging task, for which several approaches have been proposed so far [4-5]. This work presents a process specifically modified to tackle this problem, and discusses the main features of the proposed integrated sensors, summarizing the most significant results obtained so far.

PROCESS CUSTOMIZATION

The process was specifically developed for the detection of charged particles for biomedical (proton Computed Tomography), High-Energy Physics (HEP) and space applications, but its characteristics make it also suitable for the efficient detection of X-rays in the energy range from a few keV to 15keV.
Since the applications require large active pixel areas, typically ranging from 100s cm^2 to several m^2 in large HEP experiments, one of the drivers of this development was the cost-effectiveness of the technology. The approach presented here was developed starting from a commercial 110nm CMOS process with several customizations. A n-type high resistivity active volume, which can be fully depleted with a sufficiently high bias voltage applied at the backside, was used to enable fast charge collection and efficient radiation detection. A p+ region is present at the bottom of the active volume, and a deep pwell implantation at the front side is used to avoid the collection of signal electrons by the nwell hosting pMOS transistors. Figure 1 shows the simplified cross section of a pixel array implemented in this modified process.
Two engineering runs were fabricated in 2021 and 2022 in the framework of the ARCADIA project, funded by INFN, and wafers from a third run have been delivered by the foundry in the first months of 2023. In the reticles, several active pixel designs were included, together with passive test structures for the qualification of the process (Figure 2). To comply with different application needs, 3 different process splittings have been developed (Figure 3), and devices with 3 different active thicknesses, 48µm, 100µm and 200µm, have been produced using the same mask set. For the 48-µm thick devices, a p+ substrate with high-resistivity n-type epitaxial layer was used as starting material, while in the other two cases the starting material was a high-resistivity n-type wafer, that was backside processed after the completion of the front-side. A back-side p+ implantation followed by a laser annealing was used to create a shallow junction at the backside. In the 200 µm version, p+ regions surrounded by guard rings were lithographically defined.

SENSOR DESIGN

Several test devices, composed of arrays of pixels with different pitches (from 10µm to 50µm), with the pixel sensors connected in parallel, were included in the design in order to measure the electrical and functional characteristics of the sensors independently from the electronics. As a main demonstrator for the technology, a 512x512 active pixel array with 25µm pitch was developed (Figures 4 and 5). The demonstrator, designed for charged-particle tracking, features an event-driven readout architecture, and the pixels include the analog and digital circuitry needed to amplify, discriminate, store and transmit the address of the hit event. Several additional test designs, consisting in active pixel arrays with smaller area, microstrip arrays and electronic circuits test structures were also fabricated using the same reticle.

ELECTRICAL AND FUNCTIONAL CHARACTERIZATION

The passive pixel test structures were used for the electrical and electro-optical characterization of the sensors. Using a 1060-nm picosecond pulsed laser to excite the optical response from test pixels, an excellent correspondence between measurement results and TCAD simulations was obtained (Figure 6). The time needed for the complete collection of the photogenerated charge varies from a few ns for 10-µm pixels to 30-40ns for 50-µm pixels. The tail in the current signal is mainly due to charges generated at the corner of the pixels, where the lateral drift field is lower (Figure 7). Nevertheless, the charge collection is fast enough for the majority of applications and to ensure a good tolerance to non-ionizing radiation damage.
The cluster size distribution with Minimum Ionizing Particles has been studied using a combined TCAD-Monte Carlo approach, where the 3D electric field maps computed in TCAD are imported into a Monte Carlo simulation software, that computes the statistical interaction of charged particles with silicon (Figure 8). In pixels with 25µm pitch, the high electric field in the substrate is sufficient to limit the maximum cluster size to a group of 4 pixels in most cases, when particles with perpendicular incidence are considered (Figure 9).
A summary of the most relevant parameters for sensor operation, extracted from text structures, are shown in Tables 1 and 2. These results demonstrate that the proposed process can provide sensors with fast charge collection and small capacitance, with a dark current density suitable for most particle tracking and high-energy radiation imaging applications.

ACKNOWLEDGMENTS

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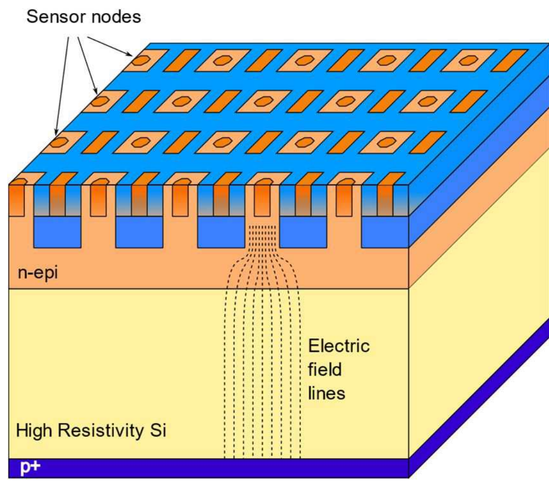


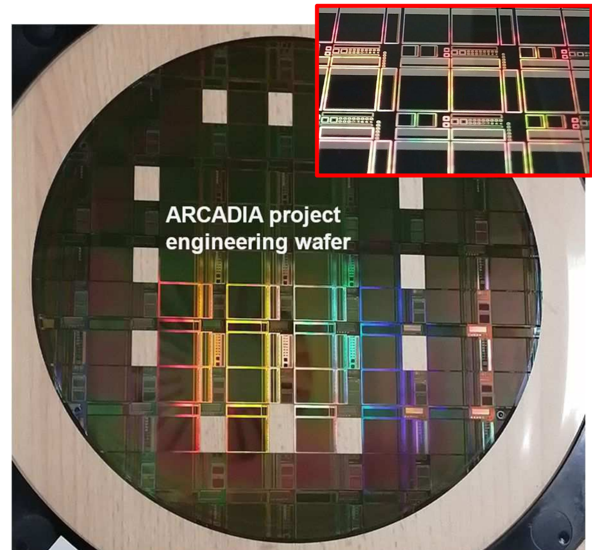


Figure 1. Schematic illustration of the pixel array, showing the sensor nodes, the surface pwell/deep-pwell regions (blue) and the isolated nwell regions (orange).

Figure 2. Image of a wafer produced in the ARCADIA project. Inset: detail of the backside of one of the wafers produced with double-sided processing.

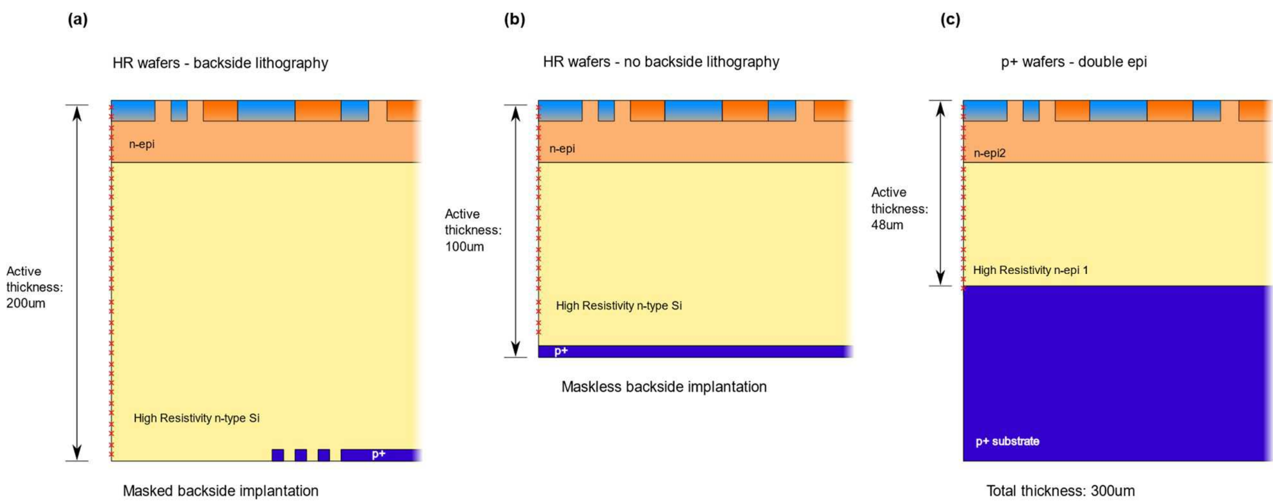
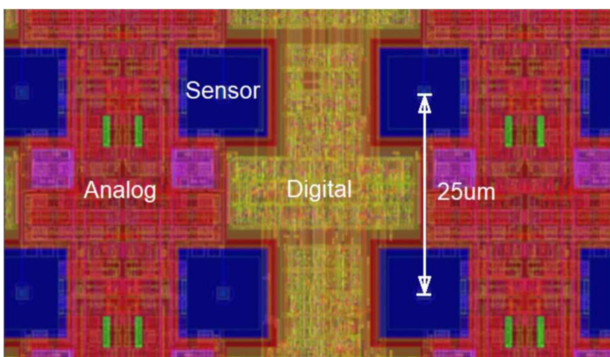


Figure 3. Cross section of the sensors produced with 3 different process splittings: a) 200µm sensors obtained with backside lithography; b) 100µm sensors with maskless p+ backside implantation; c) 48µm sensors with p+ substrate and HR epitaxial layer



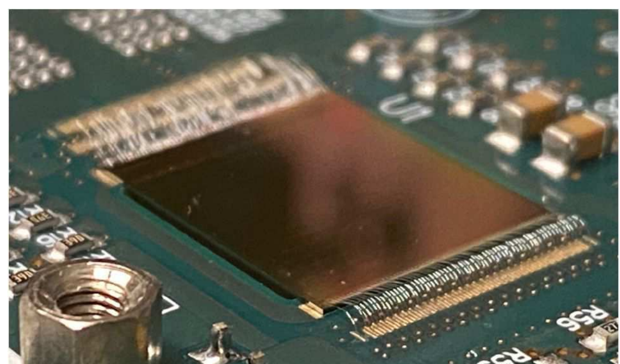


Figure 4. Detail of the layout of a group of pixels in the active 512x512 array, highlighting sensor area, analog and digital regions.

Figure 5. Image of the 512x512 active pixel array mounted on board

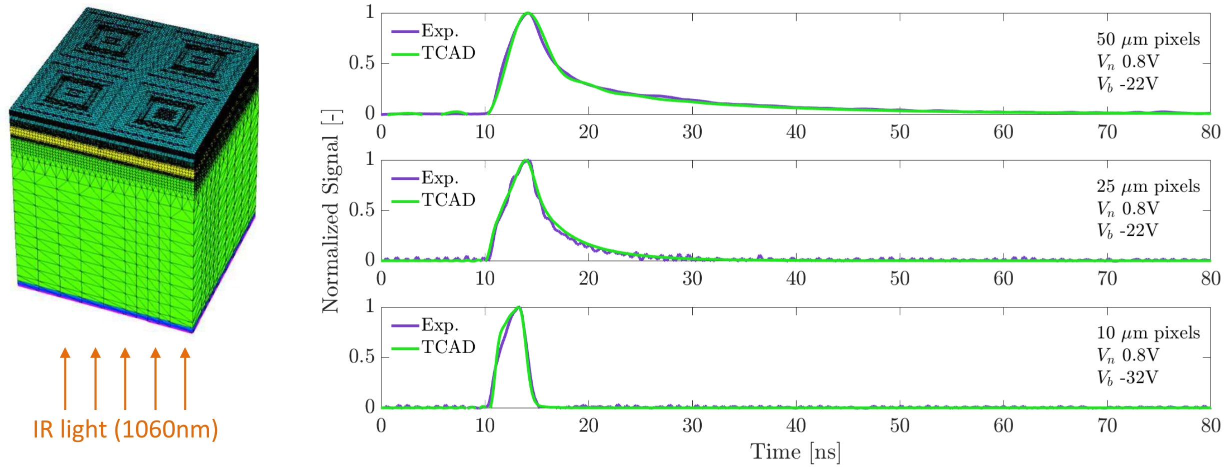


Figure 6. Optical transient response: simulated and measured on pixel test structures with fast pulsed IR laser (FWHM < 100ps, λ = 1060nm) incident uniformly on the sensor backside. In the measurements the test structures were connected to an external high-bandwidth amplifier and the simulated curves were filtered with a digital filter reproducing the characteristics of the amplifier. Measurements and simulations are shown on pixels with 3 different pitches and 100µm active thickness.

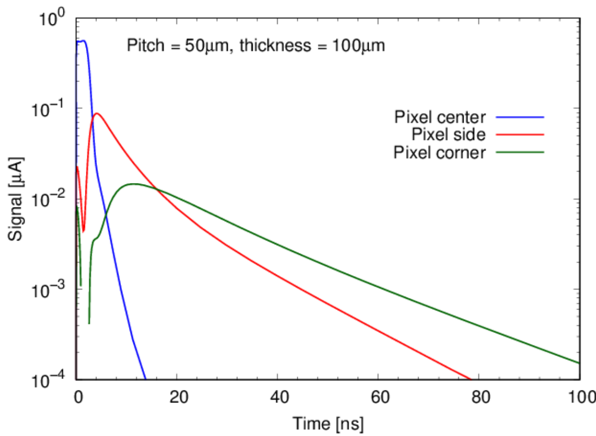


Figure 7. Simulated optical transient response with fast pulsed IR laser beam (FWHM < 100ps, λ = 1060nm) incident in different regions of the pixel.

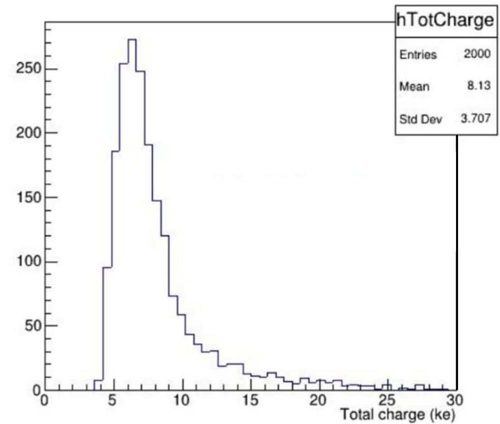


Figure 8. Simulated total charge distribution for 200-MeV muons incident on the array (100µm thickness)

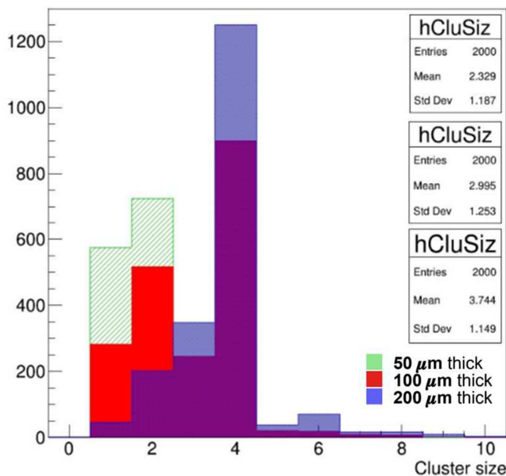


Figure 9. Simulated cluster size distribution of the 25µm-pitch sensor. In the simulations, the central pixel of a 5x5 matrix was uniformly hit by 200MeV muons with perpendicular incidence, and the threshold was set to 200e-.

Table 1. Sensor characteristics vs. wafer thickness. Ranges account for inter and intra-wafer variations

Active thickness (µm)	**48**	**100**	**200**
Sensor bias voltage (V)	25	20-35	60-100
Dark current density (pA/cm^2)	100-350	230 - 500	650 - 2000

Table 2. Sensor characteristics vs. pixel size (for 100µm active thickness)

Pixel pitch (µm)	**10**	**25**	**50**
Sensor area (% of pixel area)	36%	19%	16%
Sensor capacitance (fF)	1.9	3	12.7
Time for 90% charge collection with picosecond pulsed laser @ 1060 nm (ns)	4	10	31